FPGA

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IGLOO®2 FPGAs

The Industry's Lowest-Power FPGAs

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IGLOO®2 FPGAs Offer More Resources in Low-Density Devices With the Lowest Power, Proven Security and Exceptional Reliability

IGLOO2 FPGAs are ideal for general-purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, (I/O) expansion and conversion, video/image processing, system management and secure connectivity. FPGAs are used in communications, industrial, medical, defense and aviation markets.

IGLOO2 Features

More Resources in Low-Density Devices

- PCIe® Gen 2 support in 10K LE
- High-performance memory subsystem
- Highest I/O density

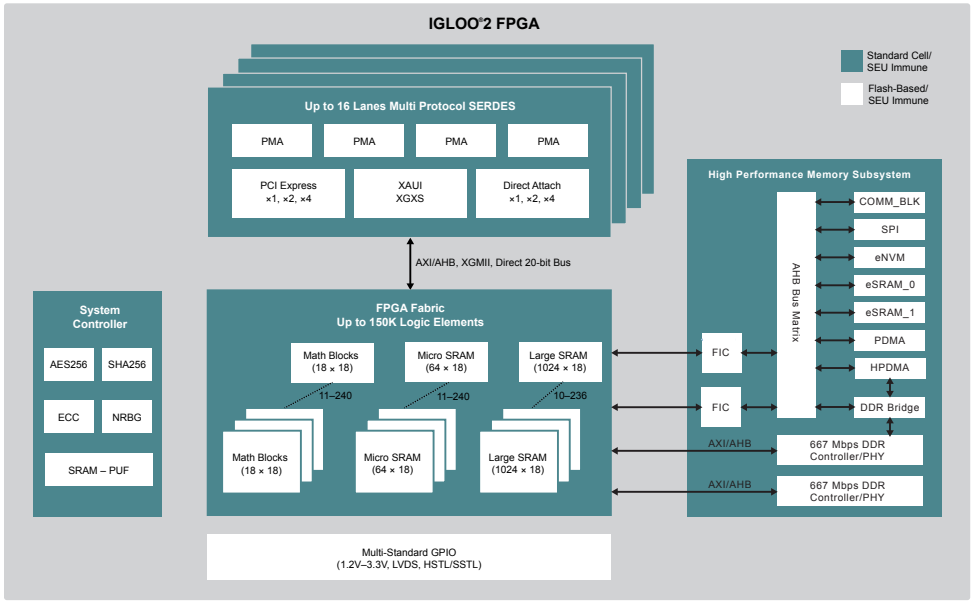
With Clear Advantages

- Lowest power
- Reduces total power by up to 50%
- 70 mW per 5G SERDES (PCIe Gen 2)
- Proven security
- Protection from overbuilding and cloning
- Secure boot for FPGA and processors
- Exceptional reliability
- SEU immune zero FIT Flash FPGA configuration
- Reliable safety-critical and mission-critical systems

IGLOO2 FPGA Architecture

IGLOO2 FPGAs offer 5K–150K LEs with a high-performance memory subsystem, up to 512 KB embedded Flash, 2 × 32 KB embedded SRAM, two Direct Memory Access (DMA) engines and two Double Data Rate (DDR) memory controllers. Architecture highlights include:

- Up to 16× transceiver lanes
  - PCIe Gen 2, XAUI/XGXS+, generic ePCS mode at 3.2G
- Up to 150K LEs, 5 Mbits SRAM, 4 Mbits eNVM
- Hard 667 Mbps DDR2/3 controllers
- Integrated DSP processing blocks
- Power as low as 7 mW standby, typical
- DPA-hardened, AES256, SHA256, on-demand NVM data integrity check
- SEU-protected/tolerant memories: eSRAMs, DDR bridges



PCI Express

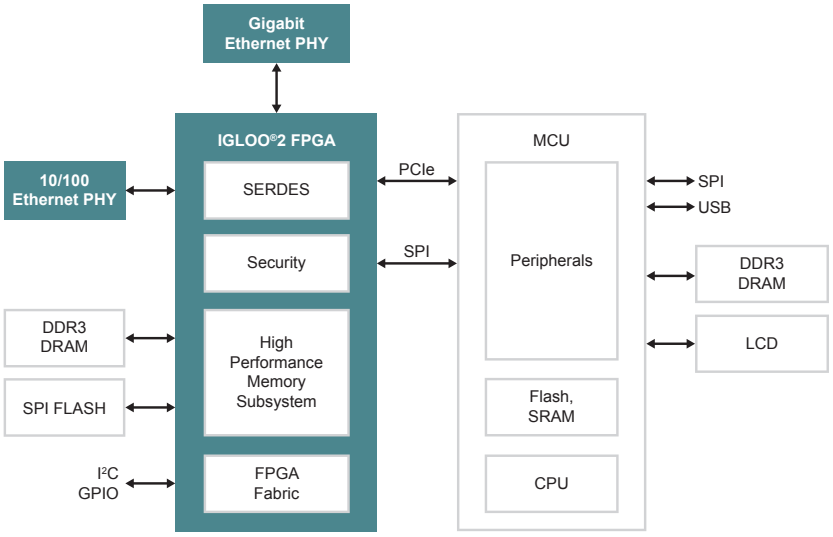
DDR3 Controller

Secure Flash

AES	Advanced Encryption Standard	**DDR**	Double Data Rate	**SHA**	Secure Hashing Algorithm
AHB	Advanced High-Performance Bus	**ECC**	Elliptical Curve Cryptography	**XAUI**	10 Gbps Attachment Unit Interface
APB	Advanced Peripheral Bus	**FIC**	Fabric Interface Controller	**XGMII**	10 Gigabit Media Independent Interface
AXI	Advanced eXtensible Interface	**HPMS**	High Performance Memory Subsystem	**XGXS**	XGMII Extended Sublayer

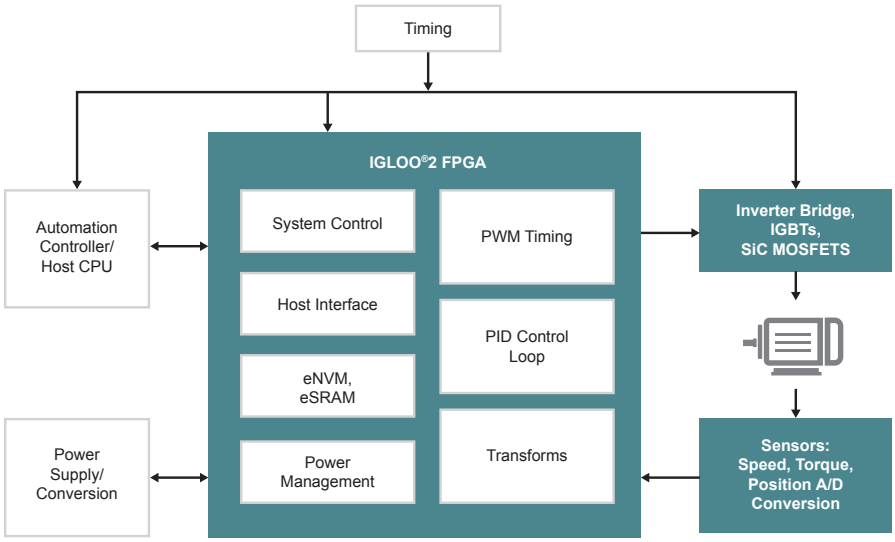
PCIe 1G Control Plane

- PCIe Gen 2 in 10K LE devices With I/O expansion



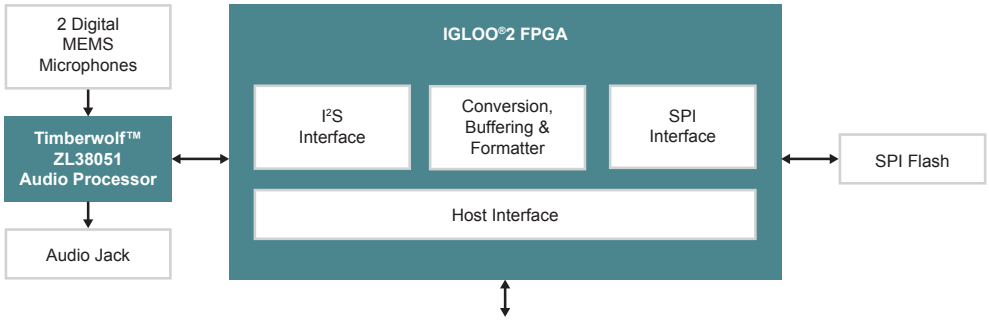
Multi-Axis Motor Control

- Deterministic and secure multi-axis/high-RPM solutions
- Motor control IP and development kit



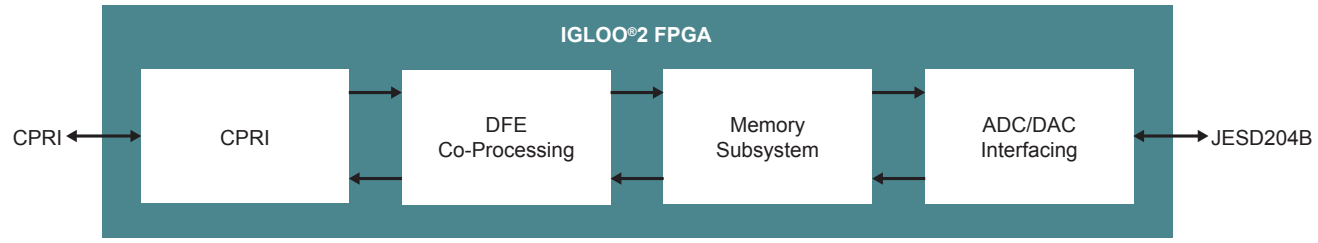
Audio Processing, Storage, and Retrieval

- I²S-to-SPI bridge allows multiple audio recordings and playbacks



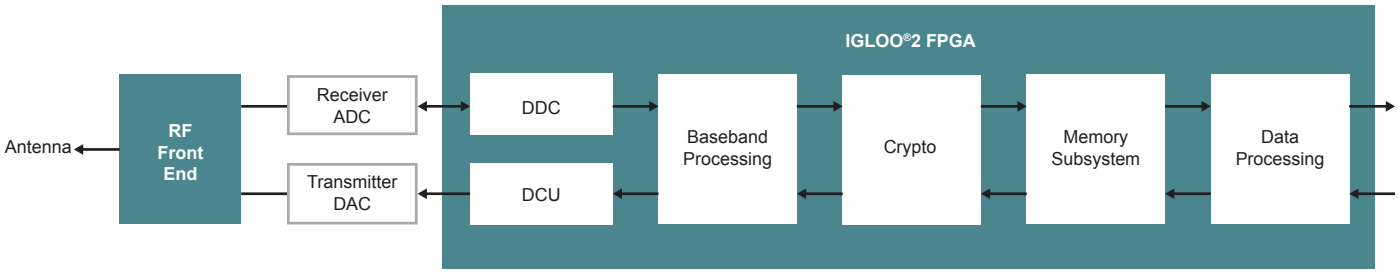
Bridging and Co-Processing

- SERDES to bridge CPRI, ADC/DAC



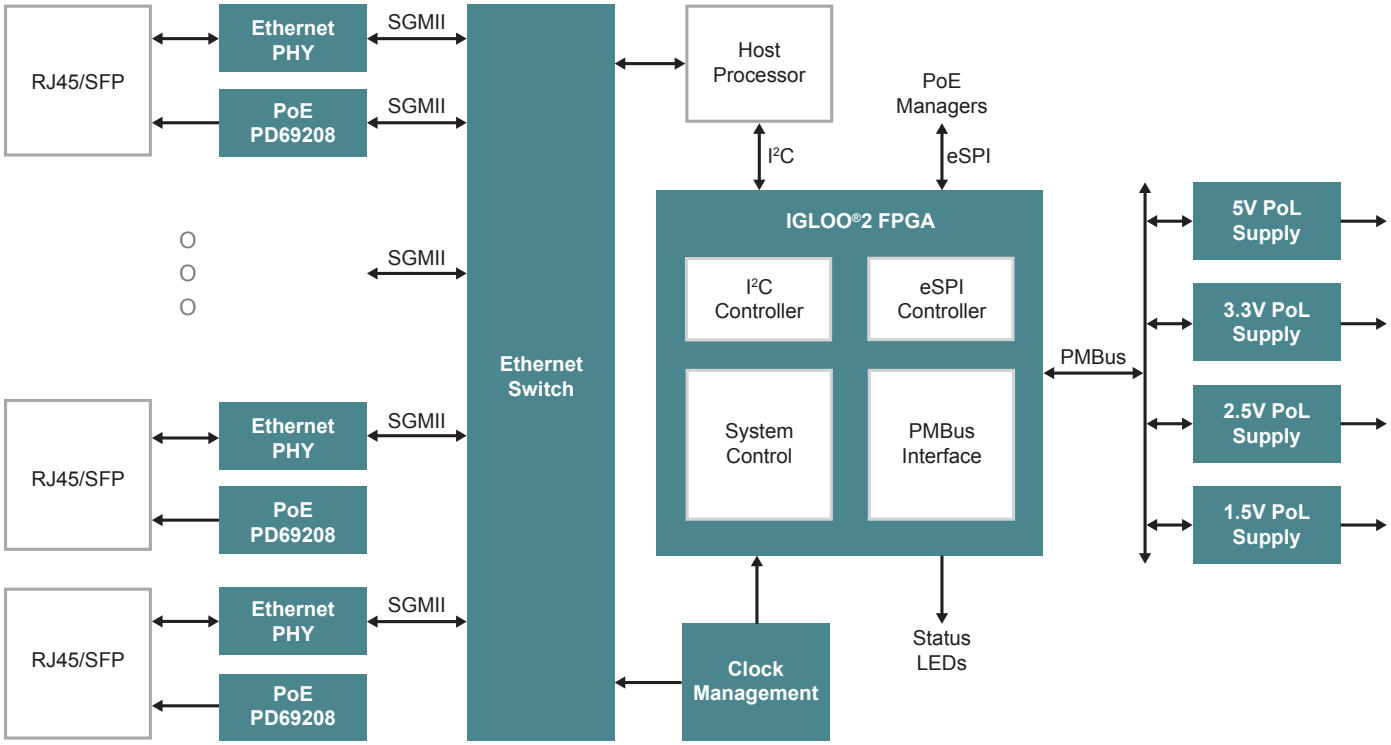
Secure Connectivity

- Best-in-class security data communications and anti-tamper
- Ultra-low static power for portability



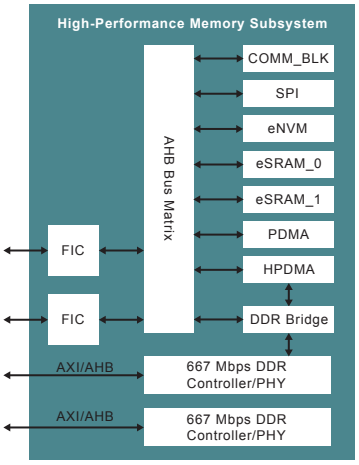
Board Initialization

- PMBus, instant-on



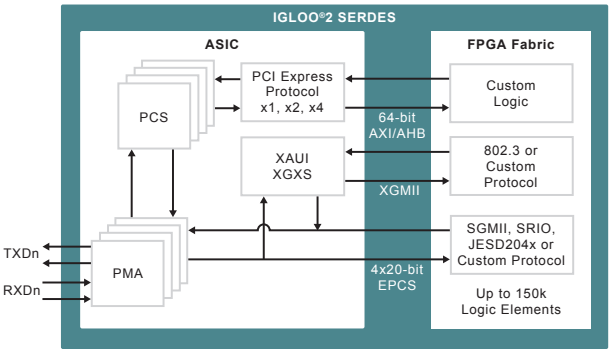
High-Performance Memory Subsystem

- 64 KB embedded SRAM (eSRAM)
- Up to 512 KB embedded nonvolatile memory (eNVM)
- One SPI/COMM_BLK
- DDR bridge (2 port) with 64-bit AXI interface
- Non-blocking, multi-layer AHB bus matrix allowing multi-master scheme supporting 4 masters and 8 slaves
- Two AHB/APB interfaces to FPGA fabric (master/slave capable)
- Two DMA controllers to offload data transactions
- 8-channel peripheral DMA (PDMA) for data transfer between soft peripherals in fabric and embedded eSRAMs, as well as support for memory-to-memory transfers
- eSRAM and external DDR memory for efficient data movement between embedded real-time memories



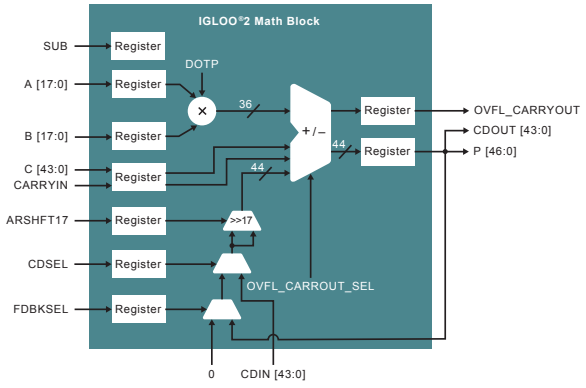
IGLOO2 FPGA SERDES

- Up to 16 lanes at up to 5 Gbps
- Dual-based reference clocks with single-lane rate granularity
- Tx and Rx PLLs programmable for each lane
- Reference clock is shared by groups of two lanes
- Transmitter features
- Programmable pre/post-emphasis
- Programmable impedance
- Programmable amplitude
- Receiver features
- Programmable termination
- Programmable linear equalization
- Built-in system debug features
- PRBS gen/chk
- Constant patterns
- Loopbacks



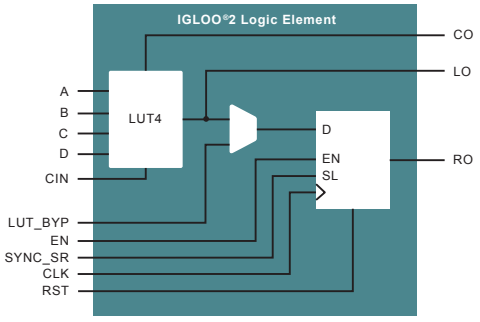
IGLOO2 FPGA Math Block

- High-performance and power-optimized multiplication operations
- Supports 18 × 18-signed multiplication (natively)
- Supports 17×17 unsigned multiplication
- Supports dot product: the multiplier computes (A[8:0] × B[17:9] + A[17:9] × B[8:0]) × 29 independent third input C with data width 44-bits completely registered
- Supports both registered and unregistered inputs and outputs
- Internal cascade signals (44-bit CDIN and CDOUT) enable cascading of the Math Blocks to support larger accumulator, adder, and subtractor without extra logic
- Supports loopback capability
- Adder support: (A×B) + C or (A×B) + D or (A×B) + C + D
- Clock-gated input and output registers for power optimizations



IGLOO2 FPGA Logic Element

- A fully permutable 4-input LUT
- A dedicated carry chain based on the carry look-ahead technique
- A separate flip-flop that can be used independently from the LUT
- Clock-gated input and output registers for power optimizations



Libero® SoC Design Software

Libero SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools that are used for designing with Microchip's power-efficient Flash-based IGLOO2 devices. The suite integrates industry-standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming and push button design flow.

This comprehensive suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adopt single-click synthesis to programming flow integrates industry-standard third-party tools, a rich IP library of DirectCores and Companion-Cores and supports complete reference designs and development kits.

https://www.microsemi.com/product-directory/design-resources/1750-libero-soc

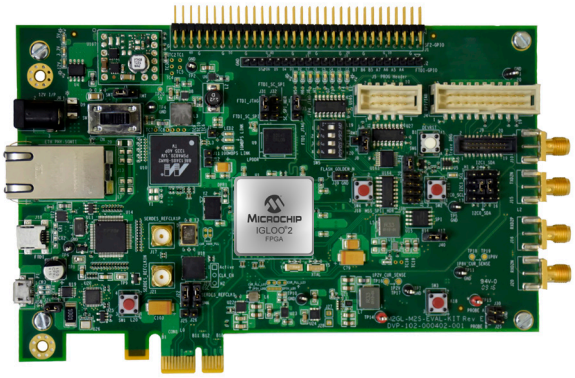
IGLOO2 Evaluation Kit

- Gives designers access to IGLOO2 FPGAs that offer leadership in I/O density, security, reliability and low power for mainstream applications
- Supports industry-standard interfaces including Gigabit Ethernet, USB 2.0 OTG, SPI, I²C and UART
- Can be powered by a 12V power supply or the PCIe connector and includes a FlashPro4 programmer

Board features

- IGLOO2 FPGA in the FGG484 package (M2GL010T-1FGG484)
- JTAG/SPI programming interface
- Gigabit Ethernet PHY and RJ45 connector
- USB 2.0 OTG interface connector
- 1 GB LPDDR, 64 MB SPI Flash
- Headers for I²C, UART, SPI, GPIOs
- ×1 Gen2 PCIe edge connector
- Tx/Rx/Clk SMP pairs

www.microsemi.com/existing-parts/parts/143976



Ordering Code	Supported Device
M2GL-EVAL-KIT	M2GL010T-1FGG484

Intellectual Property

Microchip enhances your design productivity by providing an extensive suite of proven and optimized IP cores for use with FPGAs. Our extensive suite of IP cores covers all key markets and applications. Our cores are organized as either Microchip-developed DirectCores or third-party-developed CompanionCores. Most DirectCores are available for free within our Libero tool suite and include common communications interfaces, peripherals, and processing elements.

Below are a few key DirectCores and CompanionCores. Click the below link for more details on IP Cores.
www.microsemi.com/product-directory/design-resources/5092-ip-cores

Functionality	DirectCore Examples
Connectivity	16550, 429, JESD204B, 1553BRM and 1553BRT
DSP	CIC, FFT, FIR, CORDIC, RS
Memory Controller	FIFO, DDR, QDR, SDR, MemCtrl, MMC
Processor	Mi-V RISC-V Soft CPUs
Ethernet	MII, RGMII, GMII, SGMII, TSE
Security	DES, 3DES, AES, SHA

Functionality	CompanionCores Examples
Connectivity	CAN, CANFD, PCIE, VME
DSP	FFT, JPEG, RS, DVBMOD
Memory Controller	SDRAMDDR, Flash, SD
Processor	80188, 80186, LEON3, 6809
Security	MD5, ARC4, RNG, ZUC, AES, SHA, 802.1ae (MACSec)

IGLOO2 FPGA Product Family

IGLOO®2 Devices	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL060	M2GL090	M2GL150
Logic/DSP	Maximum logic elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Math blocks (18x18)	11	22	34	72	72	84	240
	PLLs and CCCs	2		6				8
	SPI/HPDMA/PDMA	1 each						
	Fabric Interface Controllers (FICs)	1			2	1		2
	Data security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (KBytes)	128	256				512	
	LSRAM 18K Blocks	10	21	31	69		109	236
	uSRAM 1K Blocks	11	21	34	72		112	240
	eSRAM (KBytes)	64						
	Total RAM (Kbits)	703	912	1104	1826		2586	5000
High speed	DDR Controllers (count × width)	1 × 18			2 × 36	1 × 18		2 × 36
	SerDes lanes	0	4		8	4		16
	PCIe endpoints	0	1		2			4
User I/O	MSIO (3.3V)	115	123	157	139	271	309	292
	MSIOD (2.5V)	28	40		62	40		106
	DDRIO (2.5V)	66	70		176	76		176
	Total user I/Os	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M)	C, I	C, I, M					

*Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 Fabric UG for details.
*Feature availablility is package dependent.

I/Os per Package

	Package Options																			
Package type	FCS(G)325		VF(G)256		FCS(G)536		VF(G)400		FCV(G)484		TQ(G)144		FG(G)484		FG(G)676		FG(G)896		FC(G)1152	
Pitch (mm)	0.5		0.8		0.5		0.8				0.5		1.0		1.0		1.0		1.0	
Length x width (mm)	11 × 11		14 × 14		16 × 16		17 × 17		19 × 19		20 × 20		23 × 23		27 × 27		31 × 31		35 × 35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005 (S)			161				171				84		209							
M2GL010 (S/T/TS)			138	2			195	4			84		233	4						
M2GL025 (T/TS)	180	2	138	2			207	4					267	4						
M2GL050 (T/TS)	200	2					207	4					267	4			377	8		
M2GL060 (T/TS)	200	2					207	4					267	4	387	4				
M2GL090 (T/TS)	180	4											267	4	425	4				
M2GL150 (T/TS)					293	4			248	4									574	16

M2GL090 FCS325 is 11 × 13.5 package dim

Highlighted devices can migrate vertically in the same package

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If additional training interests you, Microchip offers several resources including in-depth technical training and reference material, self-paced tutorials and significant online resources.

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