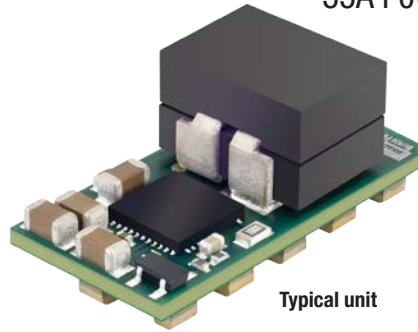


**Discontinued**



### FEATURES

- High efficiency (94%, 12Vin, 3.3Vout@25A)
- Power Block (35A, 7-13Vin, 0.8-3.6Vout, SMT)
- Small footprint (1" [25.4] x 0.5" [12.7] x 0.44" [11.1])
- No minimum load required
- Low Output Ripple
- -40°C to +85°C operating temperature
- Strong Thermal Performance
- Fast transient response
- Accurate DCR, ±5% tolerance
- High power density (384W/in<sup>3</sup>) in a compact footprint (1.0in. x 0.5in.)
- Accurate temperature sense

### PRODUCT OVERVIEW

Murata Power Solutions has developed the OKLP-X/35-W12-C, part of a new series of "Power Block" products to address the growing requirements for increased current/power densities while providing maximum flexibility for power system architectures. The OKLP-X/35-W12-C has incorporated all of the power handling components required for a 35A PoL design providing maximum

flexibility for the power systems engineer to design the power train using digital or analog controllers; however, the maximum benefits are achieved when coupled with ZMDI's ZSPM1035 single-phase digital PWM IC controller family. The OKLP-X/35-W12 series will deliver a high efficiency, thermally stable, high performance & cost effective solution for high power/current density system requirements.

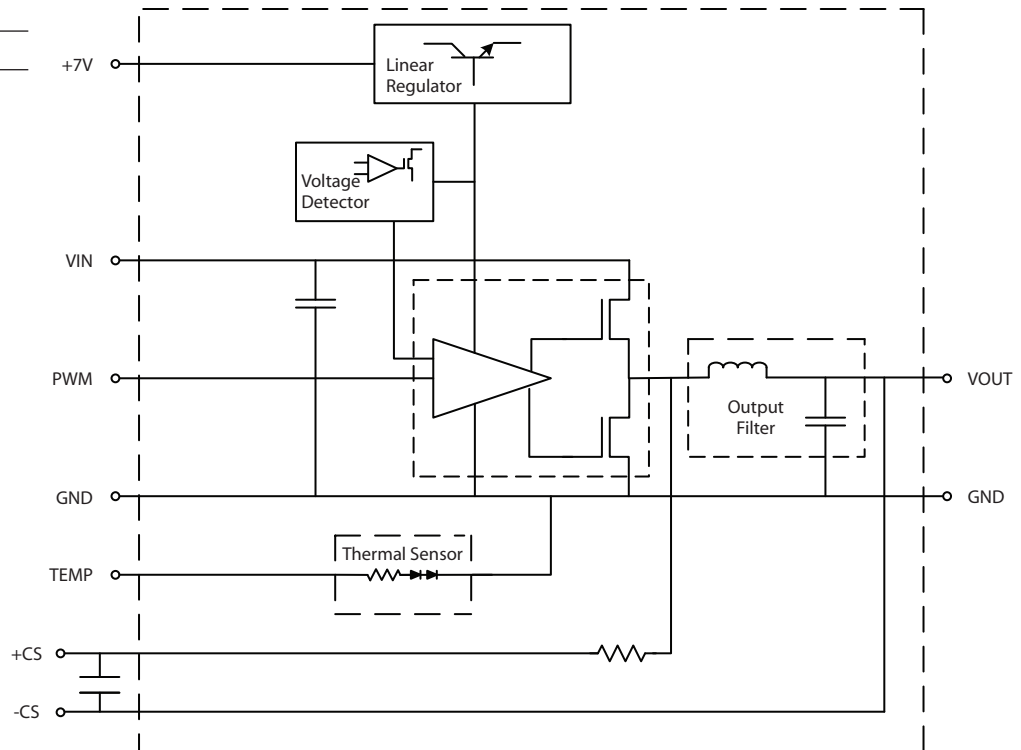


Figure 1. Block Diagram



For full details go to [www.murata-ps.com/rohs](http://www.murata-ps.com/rohs)



Discontinued

### PERFORMANCE SPECIFICATIONS SUMMARY AND ORDERING GUIDE ①

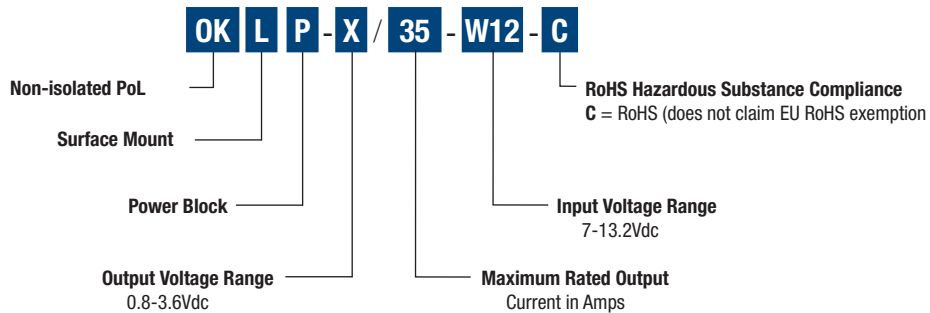
Root Model	Output			Input			Efficiency ③		Dimensions
	Vout (Volts)	Iout (Amps, max.)	Power (Watts)	Vin nom. (Volts)	Range (Volts)	Iin, full load (Amps) ②	Min.	Typ.	Inches (mm)
							91%	94.00%	
OKLP-X/35-W12-C	0.8-3.6	35	82.5	12	7-13.2	12.94			1 x 0.5 x 0.44 (25.4 x 12.7 x 11.1)

① Typical at Ta = +25°C

② @Vin = 7V, Vout = 3.3V, Iout = 25A

③ @Vin = 12V, Vout = 3.3V, Iout = 25A

### PART NUMBER STRUCTURE



ZMDI has an optimized digital controller for use with the OKLP-X/35-W12-C. See page 17 for ordering/additional information.

## 1. Input Requirements

### 1.1. Voltage:

Parameter	Notes	Min	Nom	Max	Units
Vin (Pin 6): Operating Absolute max		7	12	13.2 15.0	V
+7V (Pin 5): Operating Under-voltage lockout, rising Under-voltage lockout, falling Hysteresis		6.7 4.75 0.75	7 1.0	7.5 5.9	V
PWM (Pin 3): High Low Tri-state current	1, 2	2.5 -10		5.5 0.8 10	V μA

1. Sourcing or sinking current to/from PWM (Pin 3) within the specified range will result in both high and low-side MOSFETs to be held off by the gate-driver circuitry.

2. Before the PWM signal is applied to pin #3 (PWM), ensure that +7V is applied to the gate driver IC supply (pin 5). Otherwise, permanent damage may result to the unit.

### 1.2. Current:

Parameter	Notes	Min	Nom	Max	Units
Vin = 7V, Vout = 3.3V, Iout = 25A				12.94	A
Vin = 7V, Vout = 1.8V, Iout = 30A				8.77	A
Vin = 12V, Vout = 1.8V, Iout = 30A				5.1	A
+7V (Pin 5) (Switching at 500 KHz)				40	mA

## 2. Output Requirements

### 2.1. Voltage:

Parameter	Notes	Min	Nom	Max	Units
Operating Range		0.8		3.6	V

### 2.2. Current per Phase:

Parameter	Notes	Min	Nom	Max	Units
Operating Range					
1.0Vout	1	0		35	A
1.8Vout	1	0		30	A
3.3Vout	1	0		25	A

1. 7V to 12V input, switching at 500KHz.

## 2.3. Power/Efficiency

Parameter		Notes	Min	Nom	Max	Units
Output Power					82.5	W
Efficiency:	Vout = 3.3V, Iout = 25A, Vin = 12V	1, 2	91	94		%
	Vout = 3.3V, Iout = 25A, Vin = 7V		92	95		%
	Vout = 1.8V, Iout = 30A, Vin = 12V		89	92		%
	Vout = 1.8V, Iout = 30A, Vin = 7V		88	92		%
	Vout = 1V, Iout = 35A, Vin = 12V		86	88.8		%
	Vout = 1V, Iout = 35A, Vin = 7V		86	90		%

- 35A output, 7V to 12V input, switching at 400KHz, with 200 LFM at 55C
- Gate drive and controller losses are included. For the purpose of this calculation, controller loss is assumed to be 0.2W.

## 2.4. Capacitor

Parameter	Notes	Min	Nom	Max	Units
Input Capacitance	1, 3		52		μF
Output Capacitance	2, 3		20.1		μF

- 3 X 10μf, 25V, X7R; 1 X 22μf, 25V, X5R; 2 X 0.68μf, 25V, X8L
- 2x 10μF/0805/6.3V/X7R + 1x 0402/0.1μF/16V/X7R.
- Additional input and output capacitors are to be added externally as part of the buck regulator design.

## 2.5. Resistor

Parameter	Notes	Min	Nom	Max	Units
Output-to-GND Resistor	1		200		Ohm

- 0603 resistor.

## 2.6. Inductor

Parameter	Notes	Min	Nom	Max	Units
Inductance		337	375	413	nH
DCR (25C)	1	0.51	0.54	0.57	mOhm
Isat (125C)			40		A

- See Block Diagram for DCR sense requirements.

## 3. Temperature Sense

Parameter	Notes	Min	Nom	Max	Units
Bias current sourced from controller (into Pin 4)			495		uA
Voltage at 25C (Pin 4)		1.345	1.35	1.36	V
Temperature coefficient (0 to 130 C)			-4.4		mV / C

## 4. Mechanical

### 4.1. General

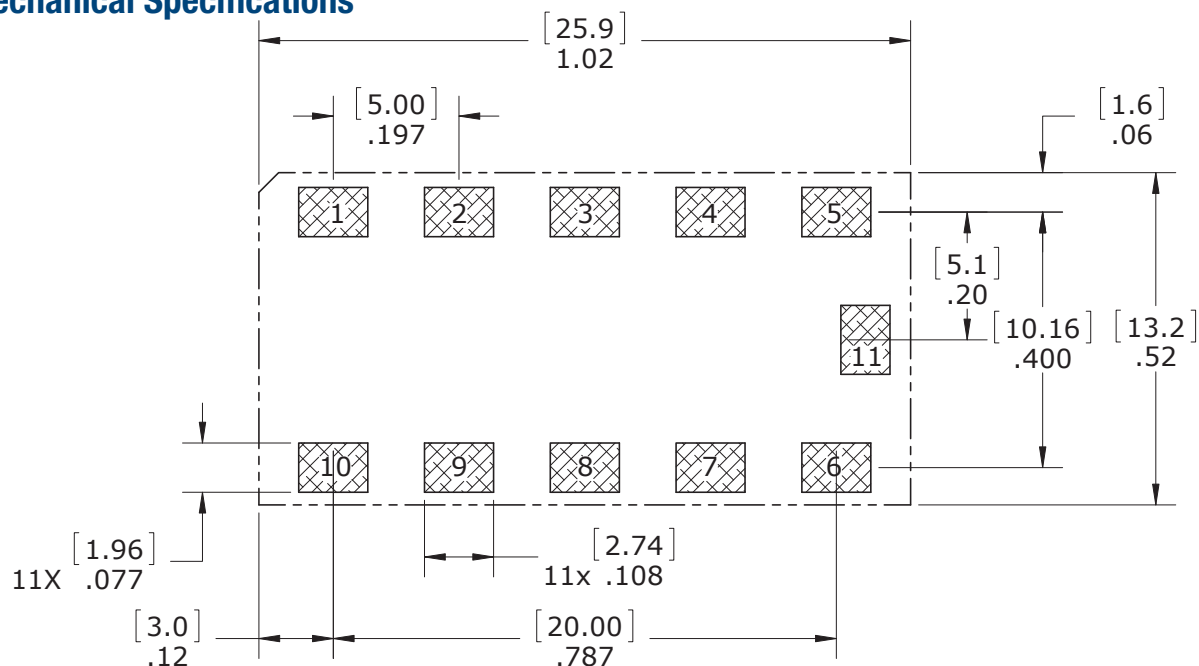
Single-board, designed for machine pick-N-place. Footprint is 0.5" x 1.0". Maximum height is 0.48".

Parameter	Notes	Nom	Units
Dimensions		1 x 0.5 x 0.44	inches
		25.4 x 12.7 x 11.1	mm
Weight		0.239	ounces
		6.8	grams

### 4.2. Pinout

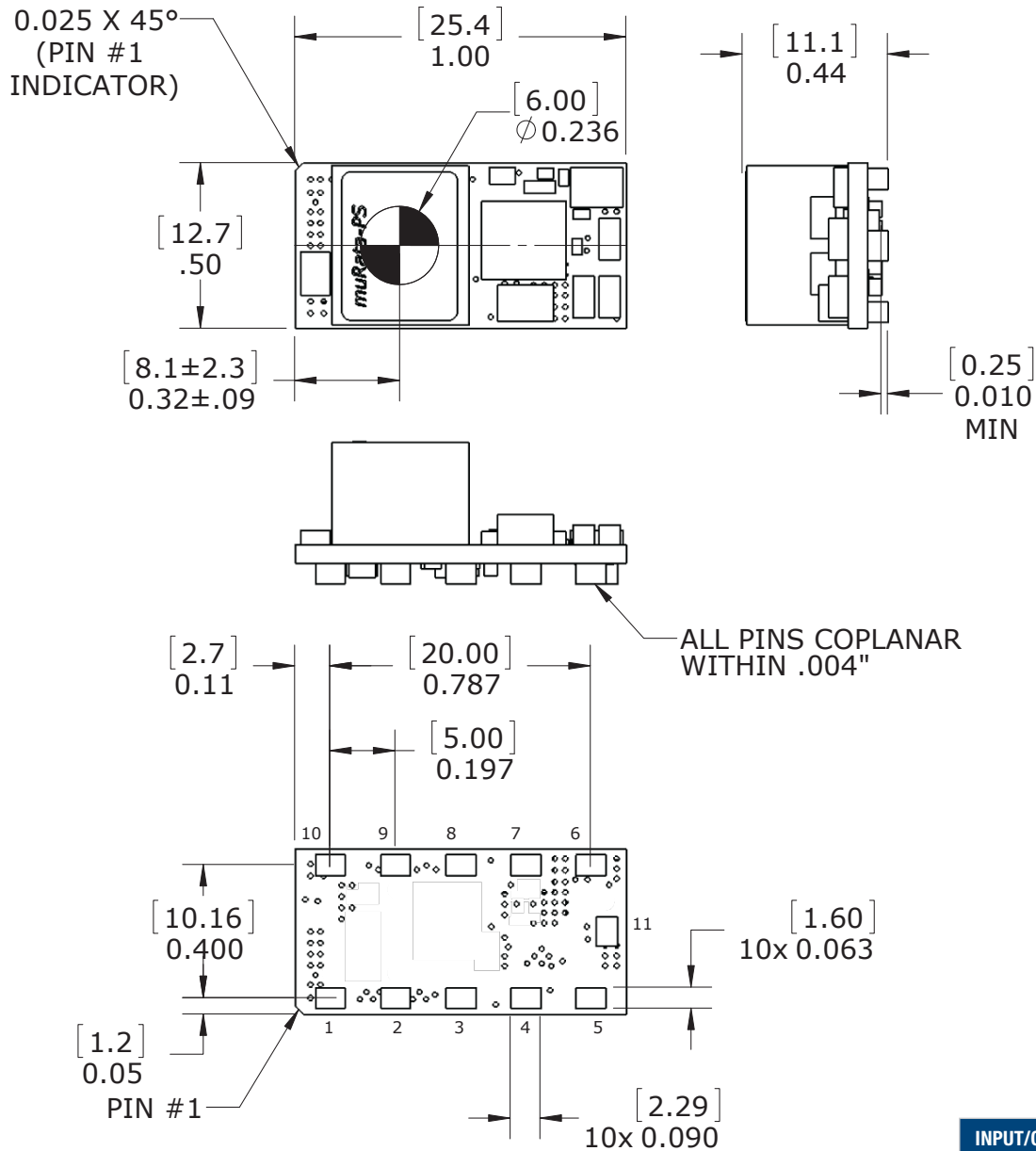
Pin #	Name	Function
1, 10	Vout	Output voltage
2, 9, 11	GND	Ground for both input and output
3	PWM	3.3V compliant PWM signal to the gate driver
4	Temperature	From temperature sense device on the power block for temperature sensing.
5	+7V	Input voltage for gate driver
6	Vin	Input voltage for the MOSFET
7	-Cs	Negative DCR sense
8	+Cs	Positive DCR sense

### 4.3. Mechanical Specifications



**RECOMMENDED FOOTPRINT  
(VIEWED THROUGH POWER BLOCK)**

Figure 2. Recommended Footprint



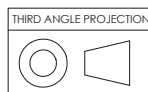
DIMENSIONS ARE IN INCHES [mm]

TOLERANCES:  
 2 PLACE ±.02      ANGLES: ±1°  
 3 PLACE ±.010

COMPONENTS SHOWN ARE FOR REFERENCE ONLY

MATERIAL:  
 PINS: COPPER ALLOY

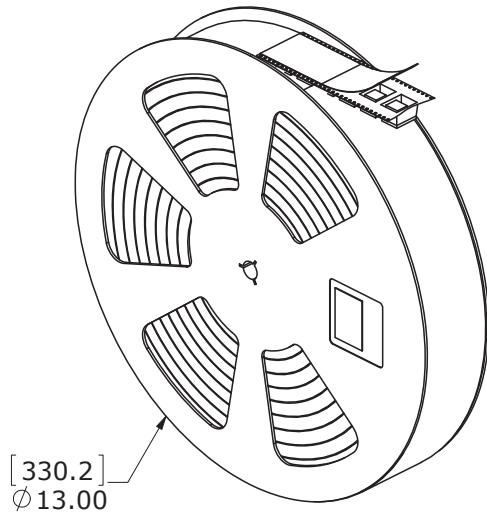
FINISH: (ALL PINS)  
 GOLD (5u"MIN) OVER NICKEL (50u" MIN)



INPUT/OUTPUT CONNECTIONS	
Pin	Function
1	Vout
2	Gnd
3	PWM
4	Temp
5	+7v
6	Vin
7	-CS
8	+CS
9	Gnd
10	Vout
11	Gnd

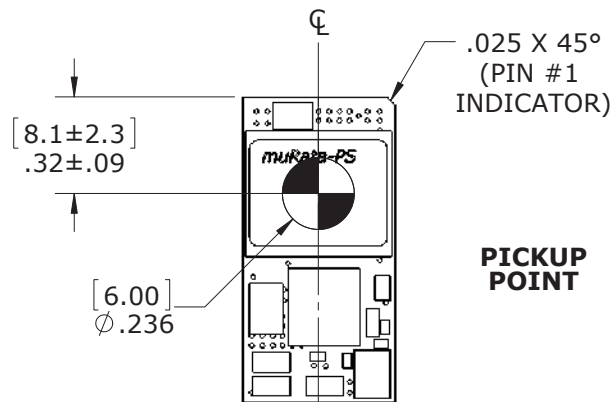
Figure 3. Mechanical Dimensions

**Tape and Reel Information (MSL Rating 2)**



**TAPE AND REEL**

7770234 SHIPPING KIT  
TAPE AND REEL WITH MSL2  
PACKAGING (NOT SHOWN)  
200 UNITS PER REEL



**FEED (UNWIND) DIRECTION**

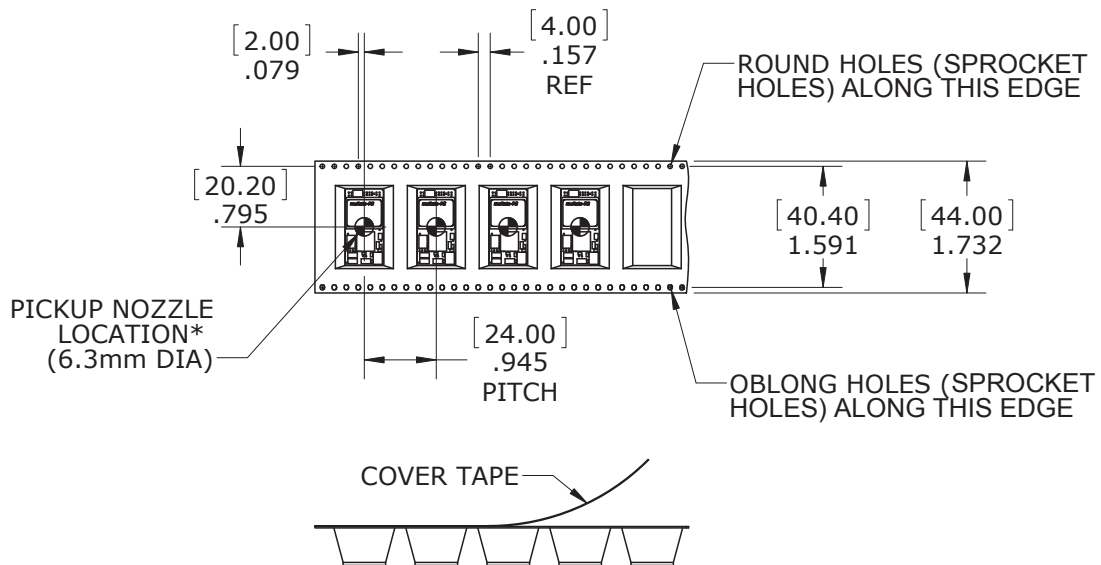


Figure 4. Tape and Reel

## 5. Block Diagram

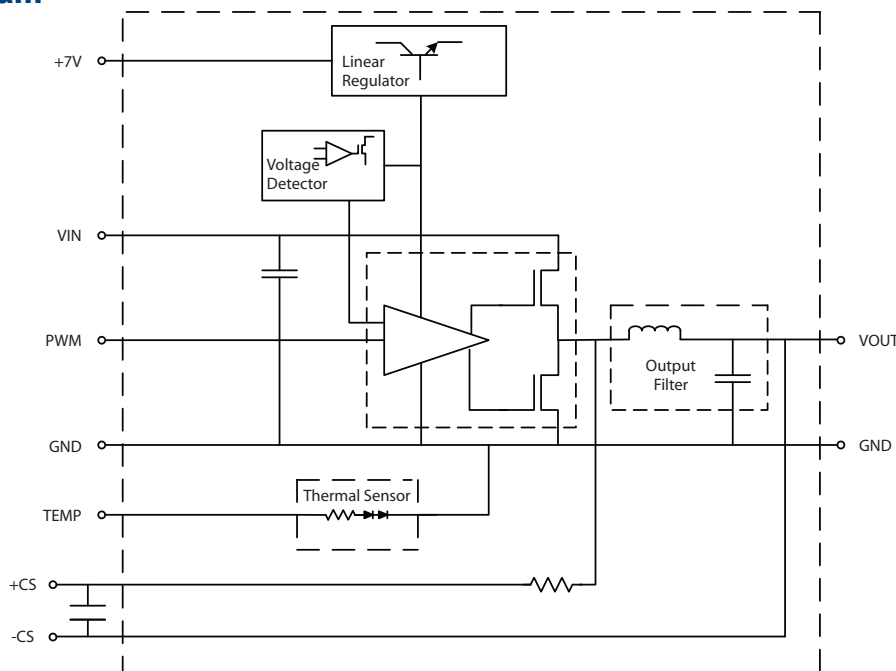


Figure 5. Block Diagram

For DCR sensing, there is a 2.37K $\Omega$  resistor on the power block (between CS+ and output inductor as shown) to work with an external 0.22 $\mu$ f capacitor (not supplied with the power block). The external C shown as across CS+ and CS- pins should be installed on the PCB near the controller. The R value in the RC network is the inductor DCR, used in the relation  $L/(DCR+PCB\ trace)=RC$ . (PCB trace equal 0.1m $\Omega$ .)

## 6. Miscellaneous

### 6.1. Environmental

Parameter	Notes	Min	Nom	Max	Units
Temperature, Operating		-40	-	85	$^{\circ}$ C
Temperature, Storage		-40	-	125	$^{\circ}$ C
Available airflow (along either long or short side)		200	-	-	LFM
Altitude, Operating	1	-500	-	10,000	Feet
Relative Humidity, Operating, Non-Condensing		10	-	90	%
MSL Rating 2					

1. Derate operating temperature 1 $^{\circ}$ C per 1000 Feet of altitude above sea-level.



**6.2. Reliability**

Parameter	Notes	Min	Nom	Max	Units
Calculated MTBF	1	3.0	-	-	MHrs
Service Life	2	7	-	-	Years

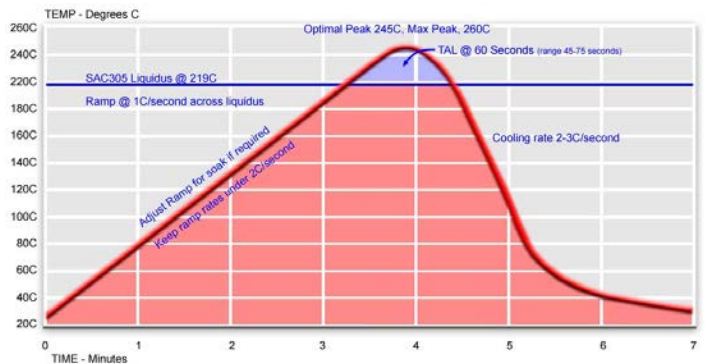
1. Calculated according to Bellcore or Telcordia TR-NTW-000332 at 40C full-load.
2. Calculated at 30°C.

**6.3. Parallel Operation**

2 or more units will be operated in parallel. Current sharing function will be performed by the external PWM controller.

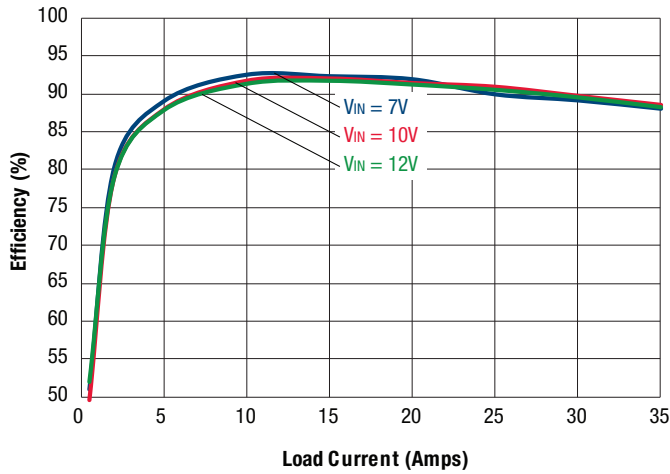
**6.4. SMT Reflow Soldering Guidelines**

The surface-mount reflow solder profile shown below is suitable for SAC305 type lead-free solders. This graph should be used only as a guideline. Many other factors influence the success of SMT reflow soldering. Since your production environment may differ, please thoroughly review these guidelines with your process engineers.

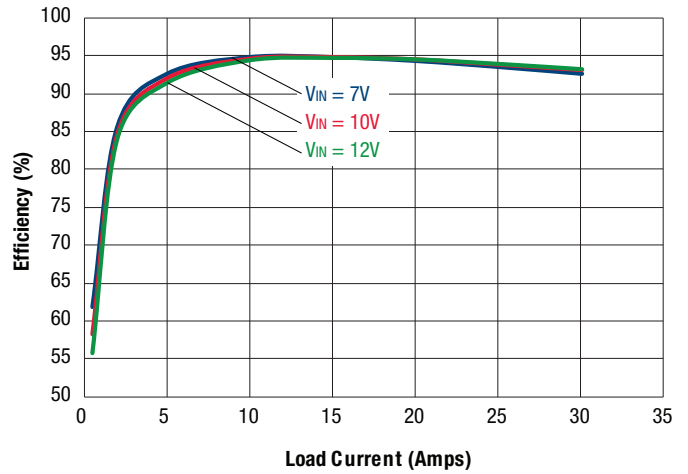


**TYPICAL PERFORMANCE DATA**

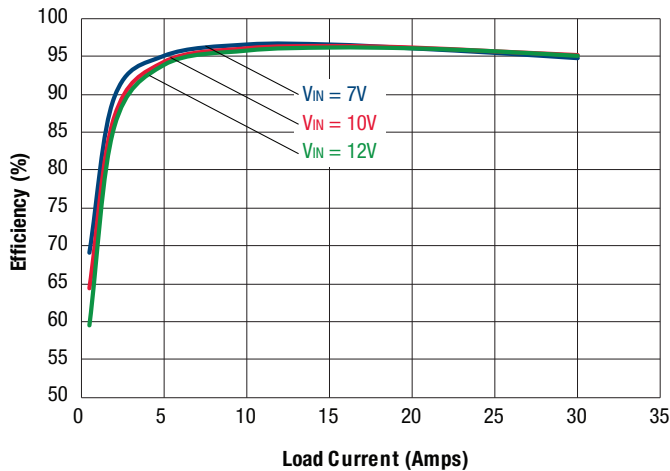
Efficiency vs. Line Voltage and Load Current @ +25°C. (Vout = 1.0V)



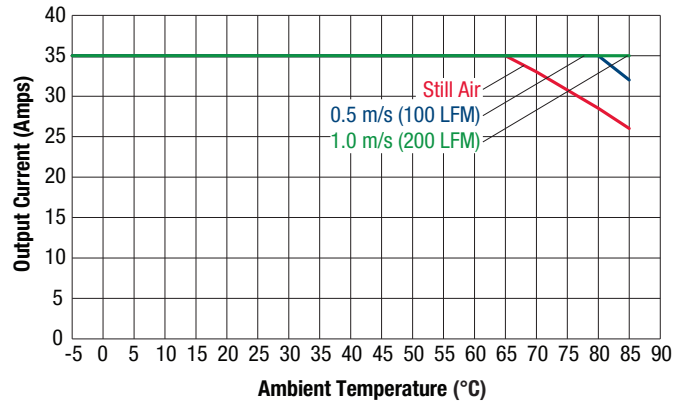
Efficiency vs. Line Voltage and Load Current @ +25°C. (Vout = 1.8V)



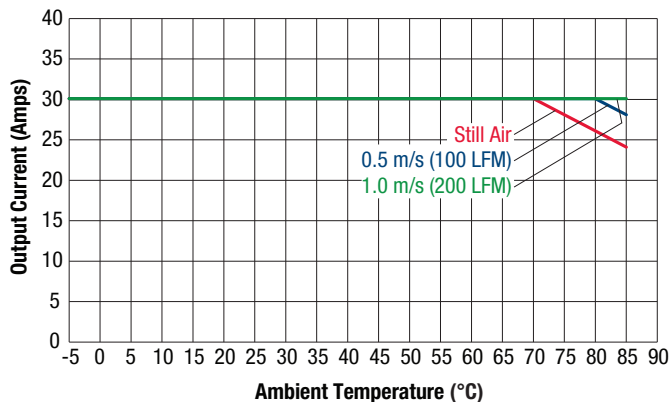
Efficiency vs. Line Voltage and Load Current @ +25°C. (Vout = 3.3V)



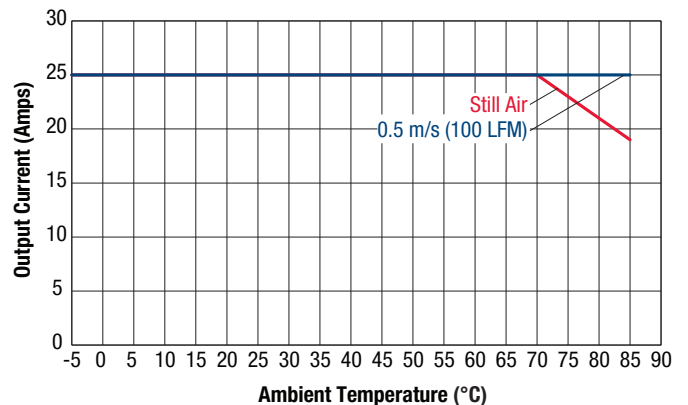
Maximum Current Temperature derating at Sea Level (Vout = 1V; Vin=7-13.2V)



Maximum Current Temperature derating at Sea Level (Vout = 1.8V; Vin=7-13.2V)

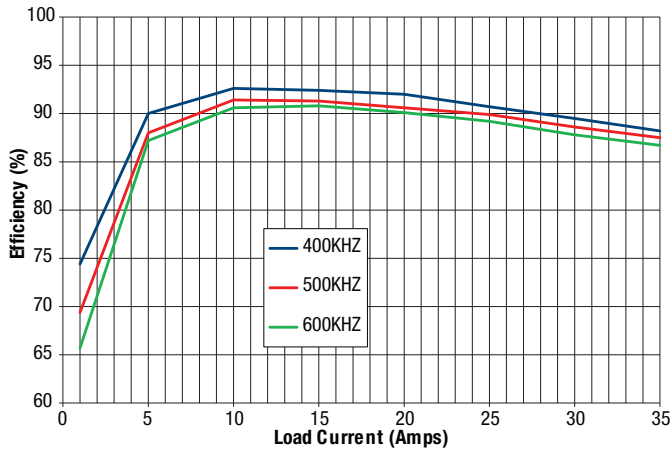


Maximum Current Temperature derating at Sea Level (Vout = 3.3V; Vin=7-13.2V)

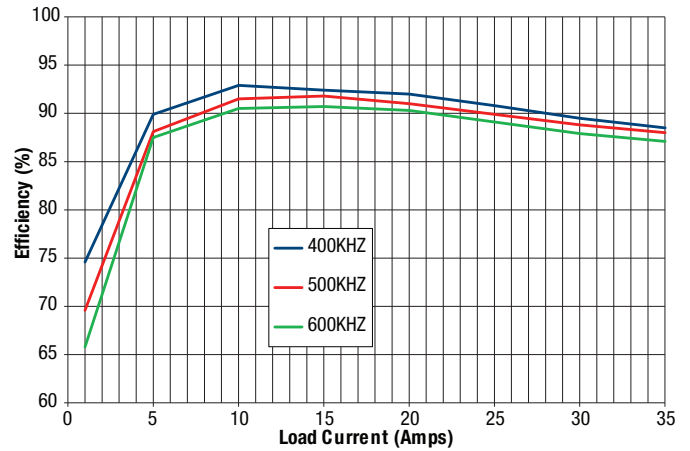


**TYPICAL PERFORMANCE DATA**

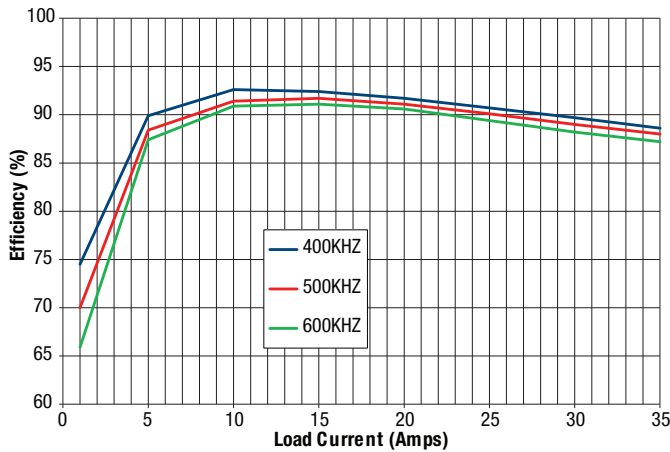
Efficiency vs. Load Current (Vo=1V, Vin=12Vin, 25°C, 0LFM)



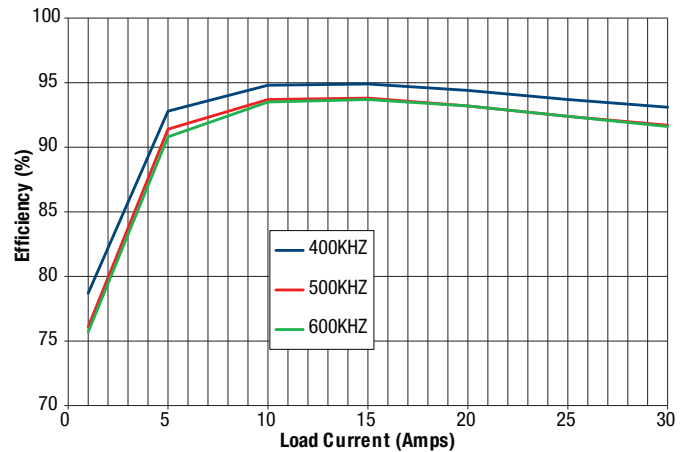
Efficiency vs. Load Current (Vo=1V, Vin=12Vin, 25°C, 100LFM)



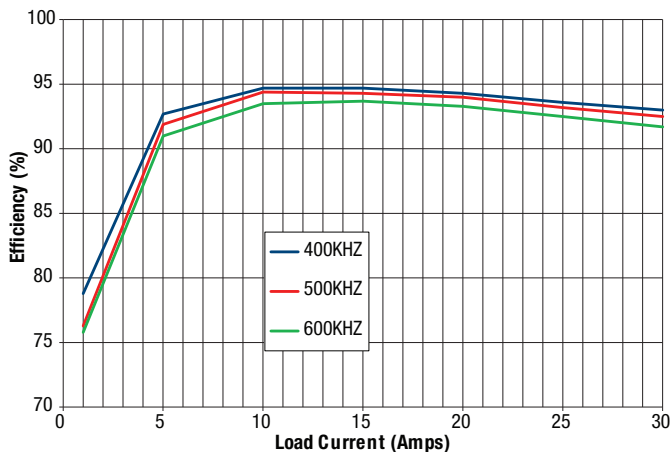
Efficiency vs. Load Current (Vo=1V, Vin=12Vin, 25°C, 200LFM)



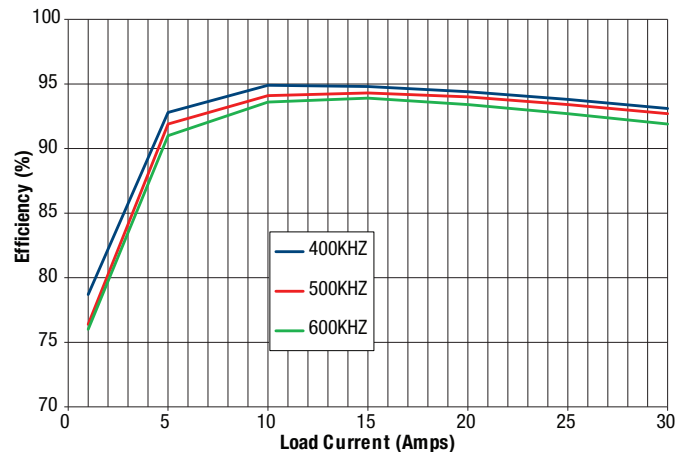
Efficiency vs. Load Current (Vo=1.8V, Vin=12Vin, 25°C, 0LFM)



Efficiency vs. Load Current (Vo=1.8V, Vin=12Vin, 25°C, 100LFM)

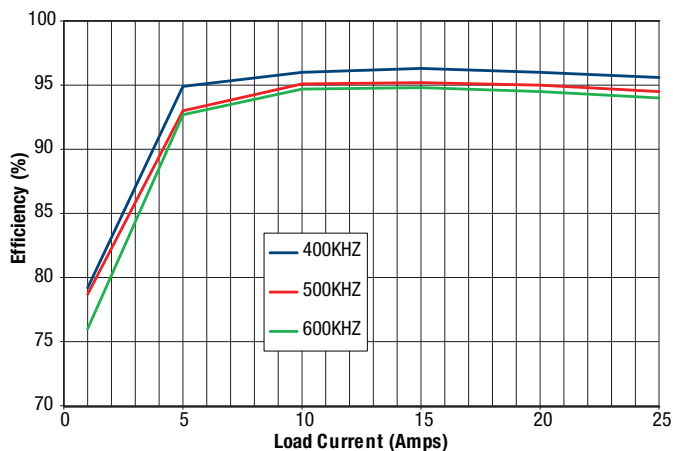


Efficiency vs. Load Current (Vo=1.8V, Vin=12Vin, 25°C, 200LFM)

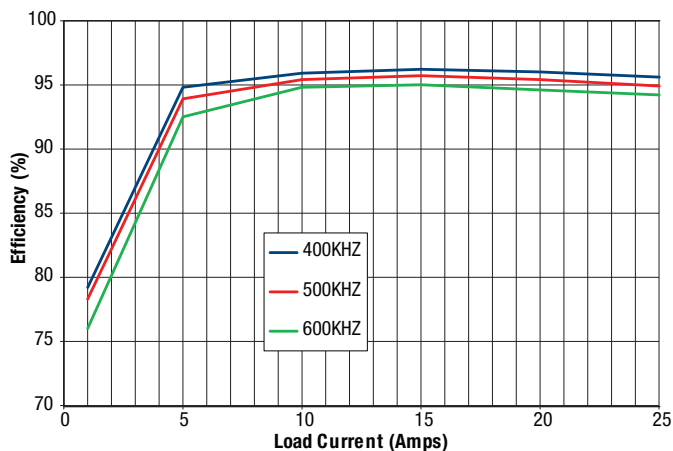


**TYPICAL PERFORMANCE DATA**

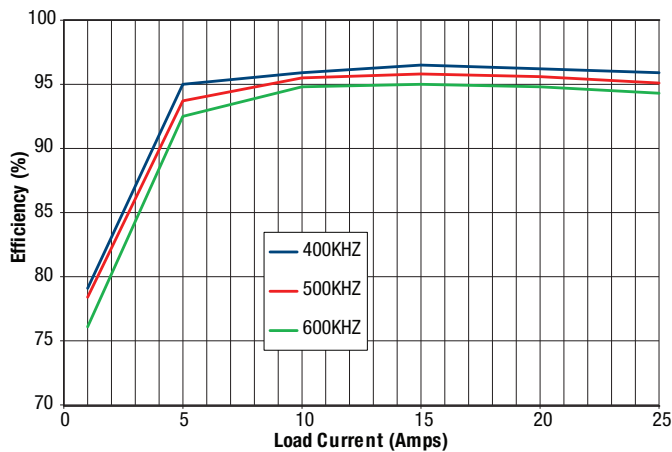
Efficiency vs. Load Current (Vo=3.3V, Vin=12Vin, 25°C, 0LFM)



Efficiency vs. Load Current (Vo=3.3V, Vin=12Vin, 25°C, 100LFM)



Efficiency vs. Load Current (Vo=3.3V, Vin=12Vin, 25°C, 200LFM)



**TECHNICAL NOTES**

**Overview**

Murata Power Solutions has developed the OKLP-X/35-W12-C, part of a new series of “Power Block” products to address the growing requirements for increased current/power densities while providing maximum flexibility for power system architectures. The OKLP-X/35-W12-C has incorporated all of the power handling components required for a 35A PoL design providing maximum flexibility for the power systems engineer to design the power train using digital or analog controllers; however, the maximum benefits are achieved when coupled with ZMDI’s ZSPM1035 single-phase digital PWM IC controller family. The OKLP-X/35-W12 series will deliver a higher efficiency, thermally stable, high performance & cost effective solution for high power/current density system requirements.

**Compelling advantages**

Murata Power Solutions’ Power Blocks offer compelling advantages to users seeking flexibility and ease-of-use, including the following:

- High efficiency, high power density (384 W/in<sup>3</sup>) in a compact footprint (1.0in. x 0.5in.)
- Accurate DCR, ±5 % tolerance
- Accurate temperature sense
- Ease of use; Simpler pcb layout; Noise/EMI contained within Power Block
- PMBus option (depending on PWM IC used)
- Current sharing options (depending on PWM IC used)
- Cost between down-solutions and integrated PoL modules
- PCB area/BOM reduction vs. fully discrete solutions
- Compatible with multiple PWM IC suppliers (e.g., IR, Linear Tech, Powervation, TI, ZMDI)

The ease-of-use aspect of the Power Blocks enables users to reduce the design cycle and improve the time-to-market. The Power Blocks are a high reliability solution with a calculated MTBF of 3 MH (min.) and Service Life of 6 years. Controlled variances and tight control over the inductor DCR, for example, ±5 % tolerance vs. ±10%, typically, enables more accurate current sense. In all these variables and features, “Knowing what you get” is important in realizing a successful and reliable design.

The OKLP-X/35 Power Block can be used with most analog or digital PWM controller IC. By simplifying the design task and providing for a high-density layout, including a reduced BOM (e.g., output capacitance), depending on transient performance vs. output capacitance, the OKLP-X/35 Power Block enables a robust design, reduced total cost of ownership and higher energy efficiency across all output load conditions. Basic information, including efficiency, thermal derating, etc., for the Power Block alone, not including controller losses, has been characterized.

Contact Murata Power Solutions for further information.

Each pin of the Power Block and related functional information for the controller (PWM) are described.

**Discussion**

The OKLP-X/35 Power Block is not a completely integrated point-of-load (PoL) solution. Power Blocks comprise the Power Stage\* of a non-isolated converter, integrating the power FETs, output inductor, current sense, temperature sense, and gate drive circuitry of a synchronous buck converter. This is the part of a PoL that performs the “heavy lifting” in the conversion process.

**\* The “Power Stage” of a Non-isolated PoL:**

- Does “the heavy lifting”—FETs, output inductor, gate drive circuitry
- Synchronous buck converter topology (evaluated at 400-600 KHz)
- Requires external parts for a complete POL solution (PWM, etc.)
- Can accommodate analog or digital controllers

In order to implement a complete POL solution, external circuitry must be added in the form of a PWM controller, gate drive voltage, as well as input and output capacitors. The Power Blocks are designed to accommodate either analog or digital PWM controllers, affording customers a wide range of performance features and functionality, according to their needs. For dense PCB circuit implementations, the PWM controller can be mounted on the underside the PCB, resulting in a very dense PCB layout.

**35A Power Block:**

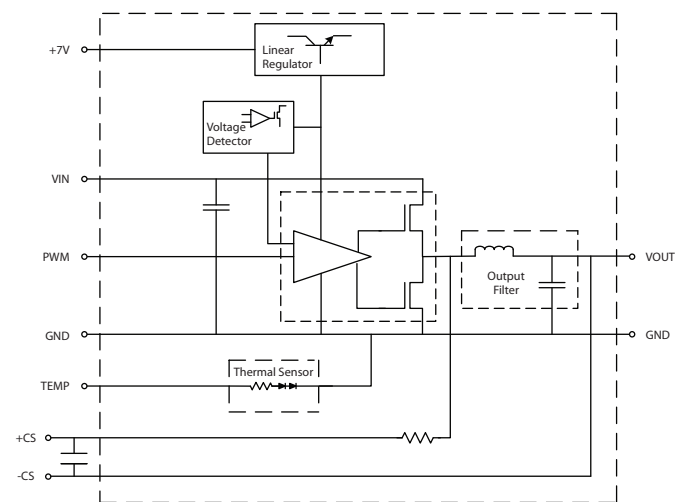


Figure 6. 35A Power Block

\* 0.22µf external capacitor must be used for accurate current sense

INPUT/OUTPUT CONNECTIONS		
Pin #	Name	Function
1, 10	Vout	Output voltage
2, 9, 11	GND	Ground for both input and output
3	PWM	3.3V compliant PWM signal to the gate driver
4	Temp	From temperature sense device on the power block for temperature sensing.
5	+7V	Input voltage for gate driver
6	Vin	Input voltage for the MOSFET
7	-Cs	Negative DCR sense
8	+Cs	Positive DCR sense

**PCB Design Guidelines**

Guidelines for proper conductor (surface and buried traces, vias, etc.) copper plating, pad sizes, trace widths, spacing, etc., can be found in IPC-2221A, "Generic Standard on Printed Circuit Board Design." Please consult this or similar standards when designing PCB layouts for the high-current output from the OLKP Power Blocks or any high-current power supply, taking into consideration, maximum currents, temperature rise and convection and/or conduction cooling of the end-user application.

**Powerblock Power Pins**

Placing large vias close to the power pins will improve thermal performance. Connecting each group of power and ground vias together on all inner layers where possible with a copper area will improve heat dissipation.

**Via Construction and Sizing**

- Via diameter and copper plating thickness affect current carrying capacity.
- Increasing outer layer copper thickness will allow thicker via plating thickness. MPS uses 3 Oz outer layers for 1 Oz via plating.
- Increased via plating thickness will prevent barrel cracking when board temperature changes to extremes, including reflow, resulting in improved reliability.

The following chart shows that larger diameter vias or thicker copper plating will improve the current carrying capacity.

$\Delta T$ $k$ $A = (\text{Diameter} * \text{Plating})$ $I = (k * (T \wedge 0.44)) * (A \wedge 0.725)$			
Via Diameter (mils)	Via wall plating thickness (oz)		
	1.00	0.50	0.25
10	1.54 A	0.93 A	0.56 A
15	2.06 A	1.25 A	0.75 A
20	2.54 A	1.54 A	0.93 A
25	2.99 A	1.81 A	1.09 A
30	3.41 A	2.06 A	1.25 A
35	3.81 A	2.31 A	1.40 A
40	4.20 A	2.54 A	1.54 A
50	4.94 A	2.99 A	1.81 A
60	5.63 A	3.41 A	2.06 A

$\Delta T$  = Max temperature rise above ambient (25°C)

$k$  = Derating constant (.024)

$A$  = Area in square mils

$I$  = Current in Amps

For optimum performance, heavy copper (2 Oz or greater) or use of multiple copper layers should be used for all power connections.

For higher currents, improved thermal performance and increased reliability of the power converter, the following suggestions are recommended:

- Multiple vias capable of carrying the current required should be used. Two adequately sized vias per amp. is not uncommon.
- Vias should be placed as close to power pins as permissible.
- Use of thermal reliefs for vias and power pads should be avoided.
- Unused inner layer via pads should not be removed. This annular ring reduces the resistance and increases the copper area of the via. Connecting these vias together on as many inner layers as possible using copper fills will also improve via performance.

- It is important to note that hole plating thickness and circumference must be used to determine the cross section when calculating the current carrying capacity of vias. Hole plating thickness will be much thinner than the copper weight of the printed circuit board.

**IPC-2221A Formula for Calculating Trace Width and Vias**

$I = k\Delta T^{0.44}A^{0.725}$

WHERE:

$I$  = current in amperes

$A$  = cross section in sq mils

$\Delta T$  = temperature rise in °C

$k$  is a derating constant such that:

$k = .048$  for outer layers

$k = .024$  for inner layers

**Input/Output Capacitor Selection**

The required amount of input and output capacitance will be determined on an application by application basis. However, there are guidelines common to every design which can be identified and following is a very brief overview.

For instance, ceramic capacitors with very low ESR (and ESL, if published) should be selected to reduce input and output ripple voltages. These should be placed as close to the power supply input as practical. External input bypass "bulk" capacitance should then be determined in order to stabilize the input voltage during large load transients and supply extra current to the load during a step load change. The maximum output capacitive loading specified in the datasheet should be observed. Consideration must also be given to ripple voltage and currents and the impact on capacitor lifetime and system reliability. Note that both input and output capacitors should be placed close to the load.

Also, as some systems are difficult to fully characterize analytically, some empirical testing may be necessary to assure successful operation.

**Input Capacitor Selection**

Reduce Input Ripple Voltage: The first step is to reduce ripple voltage amplitude at the input of the converter. For this purpose, ceramic capacitors with very low ESR should be selected; large, bulk capacitors do not reduce ripple voltage, as the ESR of aluminum electrolytics and most tantalums are too high to allow for effective ripple reduction. Therefore, to reduce the rms current in the bulk capacitors the ripple voltage amplitude must be reduced using ceramic capacitors. From the literature, "as a general rule of thumb, keeping the peak to peak ripple amplitude below 75 mV keeps the rms currents in the bulk capacitors within acceptable limits.

"Load current, duty cycle, and switching frequency are several factors which determine the magnitude of the input ripple voltage. The input ripple voltage amplitude is directly proportional to the output load current. The maximum input ripple amplitude occurs at maximum output load. Also, the amplitude of the voltage ripple varies with the duty cycle of the converter. For a single phase buck regulator, the duty cycle is approximately the ratio of output to input dc voltage. A single phase buck regulator reaches its maximum ripple at 50% duty cycle." Further detail can be found in the literature.

The following equation can be used to determine the amount of ceramic capacitance required to reduce the ripple voltage amplitude to acceptable levels:

$$C_{\text{MIN}} = (I_{\text{OUT}} \times \text{DC} \times (1 - \text{DC}) \times 1000) / (F_{\text{SW}} \times V_{\text{Pmax}}), \text{DC} = V_{\text{OUT}} / (V_{\text{IN}} \times \eta);$$

$$\eta = \text{Efficiency}$$

Where

$F_{\text{SW}}$  is the switching frequency in KHz

$I_{\text{OUT}}$  is the steady state output load current

$C_{\text{MIN}}$  is the minimum required ceramic input capacitance in  $\mu\text{F}$  ①

$V_{\text{P(MAX)}}$  is the maximum allowed peak-peak ripple voltage ②

### Example Ceramic Calculation

Given:

- $V_{\text{IN}} = 12 \text{ V}$
- $V_{\text{OUT}} = 3.3 \text{ V}$
- $I_{\text{OUT}} = 10 \text{ A}$
- $\eta = 90\%$
- $F_{\text{SW}} = 333 \text{ kHz}$
- $\text{DC} = 0.3$

The minimum ceramic capacitance required to reduce the ripple voltage to 75 mVpp is calculated to be:

$$C_{\text{MIN}} = (10 \text{ A} \times 0.3 \times (1 - 0.3) \times 1000) / (333 \times 75 \text{ mV}) = 84 \mu\text{F}$$

① The actual capacitance of a ceramic is less than the stated nominal value at a given DC voltage. Make sure the actual value is equal to or greater than the calculated value.

② 75 mVpp is recommended  $V_{\text{Pmax}}$ . This will yield approximately 22 mVrms of ripple voltage.

### Transients and Bulk Capacitors

Bulk capacitors control the voltage deviation at the input when the converter is responding to an output load transient. The higher the capacitance, the lower the deviation. Therefore, the size of the input bulk capacitor is determined by the size of the output current transient and the allowable input voltage deviation. The amplitude of the input voltage deviation during a transient is directly proportional to the load current change. If the magnitude of the transient load current is doubled, the input voltage disturbance is doubled also.

Lower input voltage means higher input currents. The input current scales directly by duty cycle. At lower input voltages the input transient currents will also be higher. To comply with output voltage deviation limits, more input capacitance is required.

Consider a 2.5V output regulator with a 10A transient load. With a 12V input, the ideal duty cycle is  $2.5/12 = 0.208$ . The 10 A load transient on the output transforms to a 2.08A transient on the input. With a 3.3 V input regulator, the duty cycle is now  $2.5/3.3 = 0.758$ . The 10 A load transient is now a 7.58A input transient. This will cause a larger voltage deviation on the lower voltage supply where the voltage limits are probably tighter.

During a transient, input inductance slows the current slew rate seen by the host supply. The use of a filter inductor places more demands on the input bulk capacitors since more of the initial current demand must come from the input capacitors rather than the host supply. The input voltage at the regulator input now sees a much higher voltage deviation. In the end, both the input and output capacitors have to be recharged, causing higher peak currents to be demanded from the host supply.

#### Bulk input capacitance calculation example

When designing a system consisting of a single POL module, **the first step** is to calculate the magnitude of the input transient current. This is done by calculating the reflected input transient for each POL module's output transient. When calculating, you must determine the worst case transient combination of all modules and proceed accordingly.

The magnitude of the input current transient is calculated from the following equation:

$$\Delta I_{\text{IN}} = V_{\text{OUT}} / (V_{\text{IN}} \times \eta) \times \Delta I_{\text{OUT}}, \text{ where}$$

- $\eta$  is efficiency
- $\Delta I_{\text{OUT}}$  is the output transient current
- $\Delta I_{\text{IN}}$  is the input transient current
- $V_{\text{OUT}}$  is the nominal output voltage
- $V_{\text{IN}}$  is the nominal input voltage

The efficiency value  $\eta$  is obtained from the regulator data sheet. Use a value from the efficiency curve for the particular output voltage and the highest expected output current.

**Next, determine the maximum allowable voltage deviation on the bulk capacitors.** This is the maximum allowable dip during the peak transient step that was calculated in step one. The smaller the voltage deviation, the higher the required amount of bulk capacitance.

The following equation calculates the minimum required bulk capacitance.

$$C = (1.21 \times \Delta I_{\text{IN}}^2 \times L) / \Delta V^2$$

Where:

$\Delta I_{\text{IN}}$  is the change in input current in response to the output step load transient

$L$  is stray inductance in the host supply path and/or any series inductor ③

$\Delta V$  is the allowable input voltage dip following the output step load transient

Note that this equation is an approximation. The value it produces should be considered to be an absolute minimum amount. The exact value will have to be determined through experimentation depending on how well regulated your host supply is.

#### Example

- Assume filter  $L = 560 \text{ nH}$
  - Assume allowable  $\Delta V$  is 100 mV
  - Assume input transient current ( $\Delta I_{\text{IN}}$ ) was calculated to be 2.774A
- $$C = (1.21 \times \Delta I_{\text{IN}}^2 \times L) / \Delta V^2 = (1.21 \times (2.774)^2 \times 560 \times 10^{-9}) / (-.100)^2 = 521 \mu\text{F}$$

According to the calculation, a minimum 521  $\mu\text{F}$  of bulk capacitance is needed. Use the nearest standard value of 560  $\mu\text{F}$ .

③ The user needs to decide if a series filter inductor is going to be used. If using an inductor, pick a value no greater than 560 nH. If not using one, use a value of 50 nH in the calculation to account for stray inductance in the host supply path and its finite bandwidth.

Detailed discussion of the use of an input inductor is beyond the scope of these guidelines, however; if reflected ripple is a concern, a small (560 nH or less) input inductor can be used. At lower currents, this input inductor can take the form of a power ferrite bead. This is an effective way to confine ripple currents to the local input bypass caps. An input inductor can reduce the reflected ripple current by an order of magnitude. During transient conditions, the use of an input inductor puts larger demands on input bulk capacitors. Take care when using input inductors as they will affect input capacitor selection.

### Output Capacitor Selection

There are numerous factors to consider when adding external capacitors to switched-mode power supplies (SMPS), including noise, startup, ESR, stability, pre-bias applications, Sense inputs, On/Off (remote enable) controls and other topics.

Most DC-DC applications require external bypass "bulk" capacitors as part of the output load. These capacitors supply extra current during a step load change. Lower DC voltages used in newer logic devices mean that the voltage margin difference between logic ZERO and logic ONE is reduced to hundreds or even tens of millivolts. Thus, since even modest power supply

noise can cause data errors by exceeding this threshold, these bypass caps are necessary to reduce this DC-DC noise.

In addition to the possibility of failed or delayed startup, increasing external capacitance can cause sluggish transient response, possible ringing and instability. The maximum output capacitive load specification is really an indication of acceptable and stable startup performance but with moderated transient response.

### Designing for Transient Performance

When designing for a load transient, the output bulk capacitors and high frequency bypass capacitors determine the response performance and voltage deviation of the regulator. The most important parameters are the magnitude of the load transient ( $\Delta I$ ) and the distributed bus impedance to the load. **The selection of the output capacitors is determined by the allowable peak voltage deviation ( $\Delta V$ ).** This limit should reflect the actual requirements, and should not be specified lower than needed.

The distribution bus impedance seen by the load is the parameter that determines the peak voltage deviation during a fast transient. The system requires a low impedance bus over all frequencies with adequate bypass capacitors to achieve fast slew rates. If the impedance of the network that supplies the load remains below a maximum impedance, the voltage deviation due to the transient will remain within allowable voltage deviation requirements. It is simply Ohm's Law:  $\Delta V = \Delta I \times Z$ . Keep the magnitude of  $Z$  below the maximum limit, and the transient voltage deviation will stay within its limits.

Divide  $\Delta V$  by the  $\Delta I$  to determine the maximum allowable impedance,  $Z_{max}$ . This is the impedance limit which must be maintained by the output capacitor network for frequencies above which the regulator is effective. To maintain low impedance from the regulator to the load, high frequency, low value ceramic capacitors must be placed very close to the load to minimize the effects of trace inductance while larger value ceramic capacitors can be placed closer to the regulator.

### Transient Design Example

Calculating the maximum allowable output impedance, given the following requirements:

- $V_O = 2.5\text{ V}$
- Output current step from 0.8 A to 12.5 A ( $\Delta I = 11.7\text{ A}$ )
- Maximum allowable voltage deviation ( $\Delta V$ ) is 100 mV
- 20 A/ $\mu\text{sec}$  slew rate.

$\Delta V/\Delta I =$  Maximum impedance

$\Delta V/\Delta I = 100\text{ mV}/11.7\text{ A} = 8.55\text{ m}\Omega$

Selecting four 330  $\mu\text{F}$  capacitors with an ESR of 25  $\text{m}\Omega$  would provide an effective ESR of 6.25  $\text{m}\Omega$  and 1320  $\mu\text{F}$  of total capacitance. Using these capacitors, the actual amplitude of the transient deviation would be about  $\pm 73\text{ mV}$  ( $11.7\text{ A} \times 6.25\text{ m}\Omega$ ). By maintaining the low impedance over the complete frequency range, any high slew rate transient will be achieved.

### Absolute Maximum Capacitor Limits

All regulators have an absolute maximum capacitance limit. MPS DC-DC converter modules incorporate output short-circuit protection. During startup, the regulator must charge the output capacitance in order to raise the output voltage to its set-point and this current flow is in addition to any load current that may be drawn by the application circuit. If there is too much output capacitance, the current demanded from the regulator trips its over-current

protection circuit. Furthermore, each over-current trip will be followed by further attempts by the regulator to restart. This can result in the regulator entering a perpetual cycle of over-current shutdown.

**Data sheet tables give the maximum allowable output capacitance for each module.** If external capacitance is required for stable operation, the minimum value will be listed in the datasheet. Recommended capacitance is also listed in the datasheet for improved transient performance. The recommended capacitance value will meet a typical  $\Delta V$  spec at a 50% transient load step.

Detailed analysis has been performed to allow capacitor limits to be accurately defined. By following the capacitor recommendations in the data sheet and selecting capacitors based on your actual operating conditions, a reliable, low-cost power system can be designed.

Additional explanation can be found at the Murata Power Solutions web page at [www.murata-ps.com/data/apnotes/dcan-58.pdf](http://www.murata-ps.com/data/apnotes/dcan-58.pdf), Application Note D-CAN-58, Output Capacitive Load Considerations.

### Power Block Performance

The OKLP-X/35 Power Block modules have been tested using controller (PWM) IC's under various transient load conditions. Contact Murata Power Solutions for further details.

### Power Block Pin Functional Descriptions

#### Pin #2, 9, 11 (Gnd)

#### Pin #3 (PWM):

This is a 3.3V logic level tri-state PWM input and 5V tolerant. "High" turns the control MOSFET on, and "Low" turns the synchronous MOSFET on. "Tri-state" turns both MOSFETs off. In diode emulation mode, "Tri-state" activates internal diode emulation control.

#### Pin #4 (Temperature): Temperature Measurement

The OKLP-X/35 includes a Thermal Sensor in the module for temperature sensing of the inductor. This element is used by the controller for temperature compensation, measuring the inductor temperature. This information can be used to adapt the gain of the current sense path to compensate for the increase in actual DCR.

**Pin #5 (+7V):** Supply to the gate driver IC (6.7V to 7.5V). This can be supplied via another +5V power rail, or a linear regulator or an LDO (e.g., LM317 or LP2992).

#### Pin #6 (Vin):

Input supply pin, with a range of 7 – 13.2Vin (see 1.1).

**Pin #8 (+Cs), Positive DCR (current) sense and Pin #7 (-Cs), Negative DCR (current) sense:** For additional information, please reference the relevant applications notes ([www.zmdi.com/zspm1000](http://www.zmdi.com/zspm1000)) for the specific controller (PWM) IC to be used. Contact Murata Power Solutions for further information. A brief description of using current sense with the Power Block follows.

### Current Sensing

Many controller (PWM) IC's implement average current sensing to provide accurate current information over the switching period. A generated schematic of the required current sensing circuitry is shown in figure 7 for the widely used DCR current-sensing method, which uses the parasitic resistance of the inductor to acquire the current information. The principle is based on a matched time-constant (i.e.,  $RC=L/R$  (DCR) between the



inductor and the low-pass filter built from the 2.15KΩ resistor and an external capacitor (not supplied with the OKLP-X/35 Power Block) across +Cs and -Cs (220µf), where the inductor L and DCR (+5%) values are used.

**Pin #1, 10 (Vout):** Output voltage supplied to the load. Note: There is minimal input/output capacitance incorporated in the Power Block. Approximately 600µf output capacitance is “typical” at 35A output current level, depending on the application. Refer to 2.4. Capacitor (OKLP-X/35 datasheet). The user needs to determine the appropriate amount of external capacitance for energy storage, ripple voltage requirements, etc.

**Power Block Design Process**

The design process begins with selecting a PWM controller for use with the OKLP-X/35-W12 Power Block. As each controller (PWM) IC differs in configuration and performance, the user needs to ensure that adequate technical support is available from the supplier of choice (e.g., datasheets, application notes and configuration tools). For details concerning usage with a Power Block (i.e., the “power stage”) to implement a point-of-load solution, including regulation, transient performance, protection and sequencing, please consult the supplier’s web page. Contact Murata-PS Technical Support ([www.murata-ps.com/support](http://www.murata-ps.com/support)), as well as the websites below, for further information.

[www.zmdi.com/Murata\\_Power\\_Block](http://www.zmdi.com/Murata_Power_Block)

[www.powervation.com/products/single-phase-controllers](http://www.powervation.com/products/single-phase-controllers)

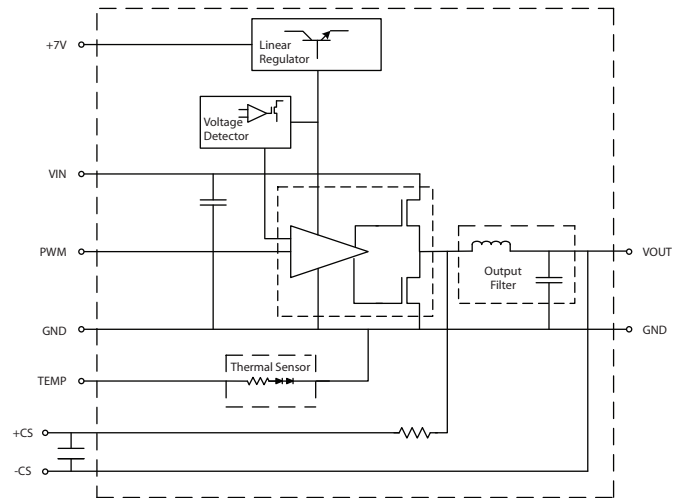


Figure 7. Inductor Current Sensing Using the DCR Method

**DEDICATED CONTROLLER P/N TO SUPPORT MURATA POWER BLOCKS**

ZMDI P/N	Murata Power Solutions P/N	Iout	Vout	Voltage Divider Setting	Output Capacitor	Release Date
ZSPM1035AA1R	OKLP-X/35-W12-C	35A	0.35V-3.6V	Programmable	4 fixed different ranges	December 2013
ZSPM1035CA1R			0.6V-1.2V	No voltage divider	4 fixed different ranges selectable by pin-strap option	
ZSPM1035DA1R			1.2V-3.4V	With voltage divider		

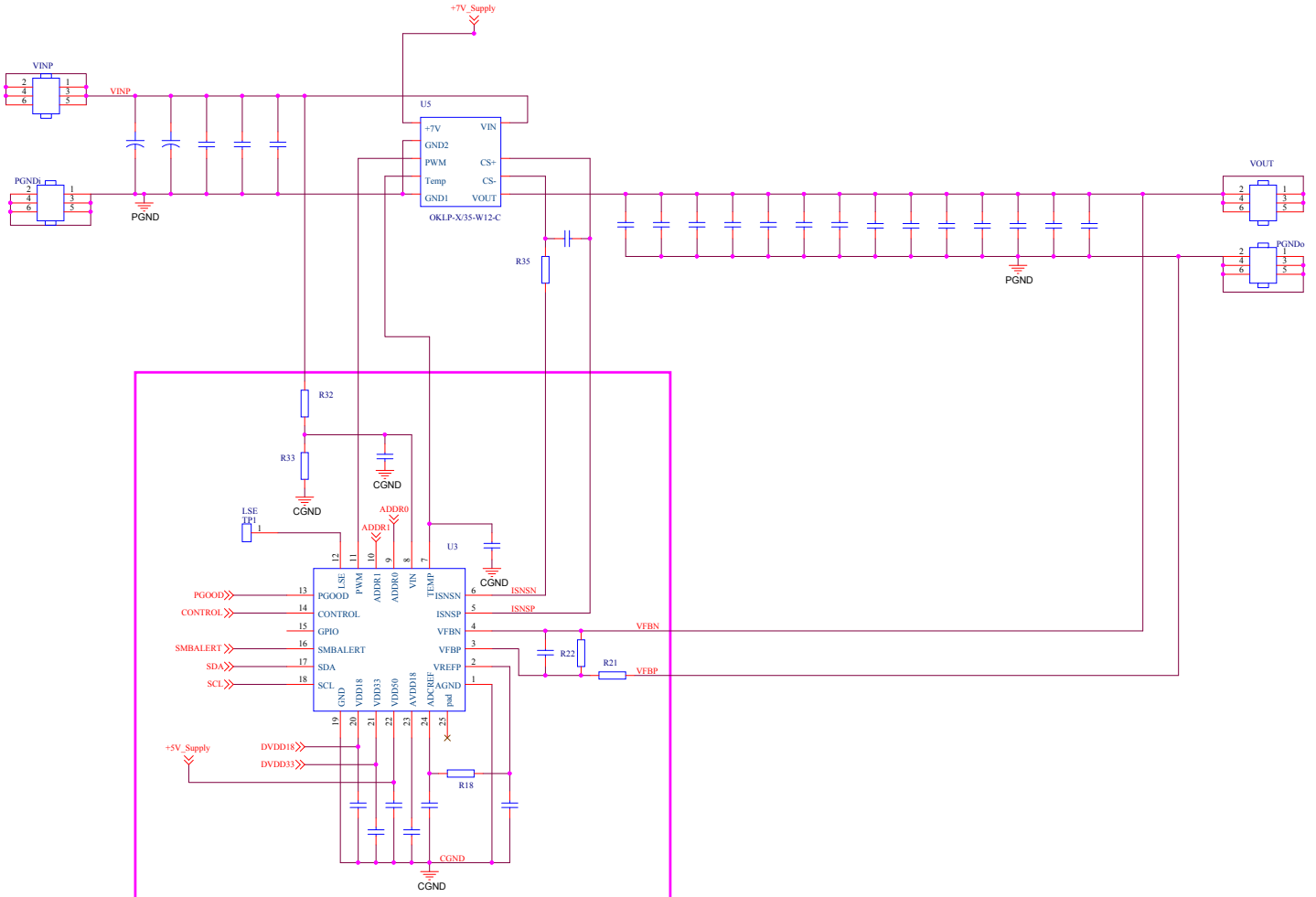


Figure 8. Typical OKLP-X/35-W12 - controller implementation

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 ISO 9001 and 14001 REGISTERED



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 Refer to: <http://www.murata-ps.com/requirements/>

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