NCV8667

150 mA LDO Regulator with Enable, Reset and Early Warning

The NCV8667 is 150 mA LDO regulator with integrated enable, reset and early warning functions dedicated for microprocessor applications. Its robustness allows NCV8667 to be used in severe automotive environments. The NCV8667 utilizes precise 1 MΩ internal resistor divider for Early Warning function which significantly reduces overall application quiescent current and number of external components. Very low quiescent current as low as 28 μA (Adjustable Early Warning Thresholds) or 42 μA (Preset Early Warning Thresholds) typical for NCV8667 makes it suitable for applications permanently connected to battery requiring very low quiescent current with or without load. The Enable function can be used for further decrease of quiescent current down to 1 μA. The NCV8667 contains protection functions as current limit, thermal shutdown and reverse output current protection.

Features

- Output Voltage Options: 5 V
- Output Voltage Accuracy: ± 2%
- Output Current up to 150 mA
- Very Low Quiescent Current:
  - typ 28 μA for Adjustable Early Warning Threshold Option
  - typ 42 μA for Preset Early Warning Threshold Option
- Very Low Dropout Voltage
- Early Warning Threshold Accuracy: ±10% Over Temperature Range (using R_{SI_ext} external resistor with ±1%, 100 ppm/°C)
- Enable Function (1 μA Max Quiescent Current when Disabled)
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Power−on Delay
  - Early Warning
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Output Current
- These are Pb−Free Devices

Typical Applications

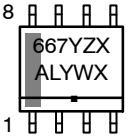
- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

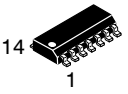
ON Semiconductor®

http://onsemi.com

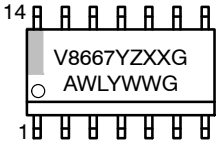
MARKING DIAGRAMS

SO−8
D SUFFIX
CASE 751





SO−14
D SUFFIX
CASE 751A



Y	= Timing and Reset Threshold Option*
Z	= Early Warning Option*
XX, X	= Voltage Option 5.0 V (XX = 50, X = 5)
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

*See Application Information Section.

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 18 of this data sheet.

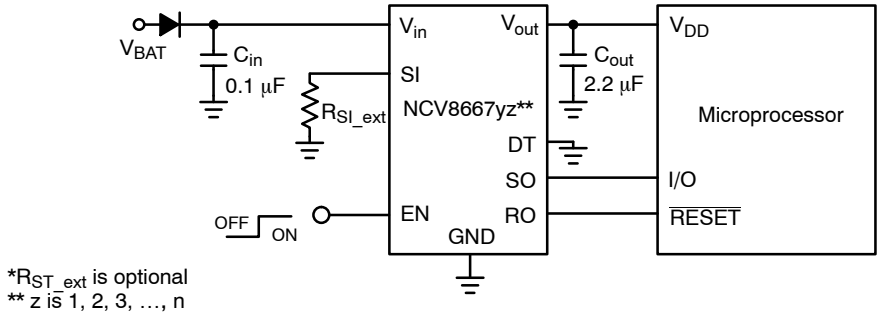


Figure 1. Application Circuit (Preset Early Warning Thresholds)

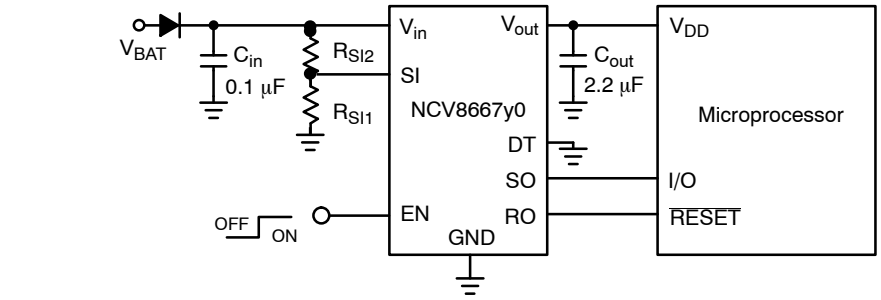
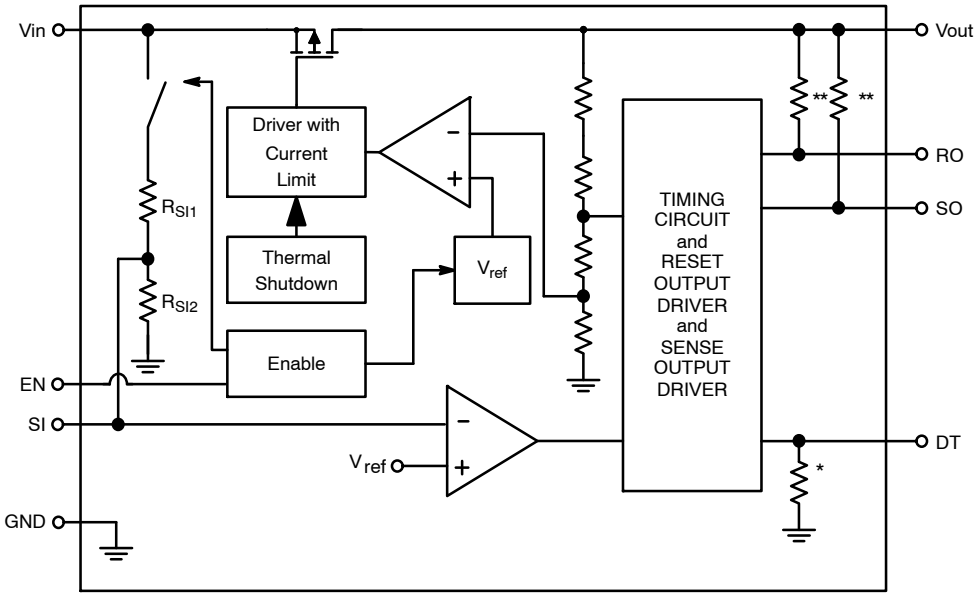
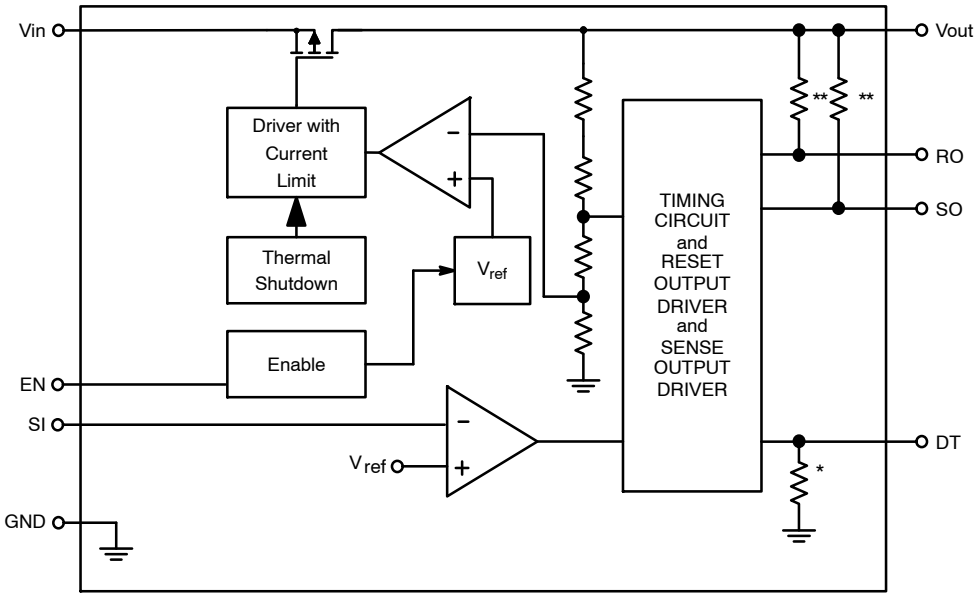


Figure 2. Application Circuit (Adjustable Early Warning Thresholds)



*Pull−down Resistor (~150 kΩ) active only in Reset State.
** 5 V option only.

Figure 3. Simplified Block Diagram of NCV8667yz (z is 1, 2, 3, … , n) (Preset Early Warning Threshold options)



*Pull−down Resistor (~150 kΩ) active only in Reset State.
** 5 V option only.

Figure 4. Simplified Block Diagram of NCV8667y0 (Adjustable Early Warning Threshold options)

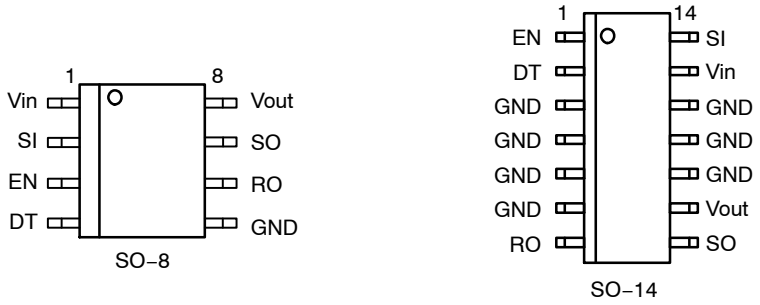


Figure 5. Pin Connections
(Top View)

PIN FUNCTION DESCRIPTION

Pin No. SO−8	Pin No. SO−14	Pin Name	Description
3	1	EN	Enable Input; low level disables the IC.
4	2	DT	Reset Delay Time Select. Short to GND or connect to V_{out} to select time.
5	3, 4, 5, 6, 10, 11, 12	GND	Power Supply Ground.
6	7	RO	Reset Output. 30 kΩ internal Pull−Up resistor connected to V_{out}. RO goes Low when V_{out} drops by more than 7% (typ.) from its nominal value
7	8	SO	Early Warning Output. 30 kΩ internal Pull−Up resistor connected to V_{out}. It can be used to provide early warning of an impending reset condition. Leave open if not used.
8	9	V_{out}	Regulated Output Voltage. Connect 2.2 μF capacitor with ESR < 100 Ω to ground.
1	13	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
2	14	SI	Adjustable Early Warning Threshold: Sense Input; If not used, connect to V_{out}. Preset Early Warning Threshold: Early Warning Adjust Input; connect R_{SI_ext} against GND to adjust Input Voltage Early Warning Threshold or leave unconnected. See Electrical Characteristics Table and Application Information sections for more information.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC (Note 1)	V_{in}	−0.3	40	V
Input Voltage Transient (Note 1)	V_{in}	–	45	V
Input Current	I_{in}	−5	–	mA
Output Voltage (Note 2)	V_{out}	−0.3	5.5	V
Output Current	I_{out}	−3	Current Limited	mA
Enable Input Voltage DC	V_{EN}	−0.3	40	V
Enable Input Voltage Transient	V_{EN}	–	45	V
Enable Input Current Range	I_{EN}	−1	1	mA
DT (Reset Delay Time Select) Voltage	V_{DT}	−0.3	5.5	V
DT (Reset Delay Time Select) Current	I_{DT}	−1	1	mA
Reset Output Voltage	V_{RO}	−0.3	5.5	V
Reset Output Current	I_{RO}	−3	3	mA
Sense Input Voltage DC	V_{SI}	−0.3	40	V
Sense Input Voltage Transient	V_{SI}	–	45	V
Sense Input Current	I_{SI}	−1	1	mA
Sense Output Voltage	V_{SO}	−0.3	5.5	V
Sense Output Current	I_{SO}	−3	3	mA
Maximum Junction Temperature	$T_{J(max)}$	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	−2	2	kV
ESD Capability, Machine Model (Note 3)	ESD_{MM}	−200	200	V
Lead Temperature Soldering Reflow (SMD Styles Only) (Note 4)	T_{SLD}	–	265 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. 5.5 or (V_{in} + 0.3 V), whichever is lower
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SO−8 (Note 5) Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Pin4 (Note 6)	 $R_{\theta JA}$ $\Psi_{\psi JP4}$	 132 49	°C/W
Thermal Characteristics, SO−14 (Note 5) Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Pin4 (Note 6)	 $R_{\theta JA}$ $\Psi_{\psi JP4}$	 94 18	°C/W

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 7)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 8)	V_{in}	5.5	40	V
Junction Temperature	T_J	−40	150	°C

7. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
8. Minimum V_{in} = 5.5 V or (V_{out} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS V_{in} = 13.2 V, V_{EN} = 3 V, V_{DT} = GND, V_{SI} = V_{out} (NCV8667y0 only), R_{SI1}, R_{SI2}, R_{SI_ext} not used, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40 °C to 150°C; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %)	V_{in} = 5.6 V to 40 V, I_{out} = 0.1 mA to 100 mA V_{in} = 5.8 V to 16 V, I_{out} = 0.1 mA to 150 mA	V_{out}	4.9 4.9 (−2 %)	5.0 5.0	5.1 5.1 (+2%)	V
Output Voltage (Accuracy %)	T_J = −40°C to 125°C V_{in} = 5.8 V to 28 V, I_{out} = 0 mA to 150 mA	V_{out}	4.9 (−2 %)	5.0	5.1 (+2%)	V
Line Regulation	V_{in} = 6 V to 28 V, I_{out} = 5 mA	Reg_{line}	−20	0	20	mV
Load Regulation	I_{out} = 0.1 mA to 150 mA	Reg_{load}	−40	10	40	mV
Dropout Voltage (Note 11) 5.0 V 	 I_{out} = 100 mA I_{out} = 150 mA	V_{DO}	 − −	 225 300	 450 600	mV
Output Capacitor for Stability (Note 12)	I_{out} = 0 mA to 150 mA	 C_{out} ESR	 2.2 0.01	 − −	 100 100	 μF Ω
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V,T_J < 85°C	I_{DIS}	−	−	1	μA
Quiescent Current, I_q = I_{in} − I_{out} (Note 13) Adjustable EW Threshold Option: Preset EW Threshold Options: 	 I_{out} = 0.1 mA, T_J = 25°C I_{out} = 0.1 mA to 150 mA, T_J ≤ 125°C I_{out} = 0.1 mA, T_J = 25°C I_{out} = 0.1 mA to 150 mA, T_J ≤ 125°C	I_q	 − − − −	 28 − 42 	 35 37 49 50	μA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	205	−	525	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	205	−	525	mA

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V.
12. Values based on design and/or characterization.
13. I_q for Preset EW Threshold Options is measured when R_{SI_ext} is not used. For typical values of I_q vs R_{SI_ext} see Figure 27.
14. See APPLICATION INFORMATION section for Reset Threshold and Reset Delay Time Options

ELECTRICAL CHARACTERISTICS V_{in} = 13.2 V, V_{EN} = 3 V, V_{DT} = GND, V_{SI} = V_{out} (NCV8667y0 only), R_{SI1}, R_{SI2}, R_{SI_ext} not used, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40 °C to 150°C; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REVERSE OUTPUT CURRENT PROTECTION						
Reverse Output Current Protection	V_{EN} = 0 V, I_{out} = −1 mA	V_{out_rev}	–	2	5.5	V
PSRR						
Power Supply Ripple Rejection (Note 12)	f = 100 Hz, 0.5 V_{pp}	PSRR	–	60	–	dB
ENABLE						
Enable Input Threshold Voltage Logic Low Logic High		$V_{th(EN)}$	 – 2.5	 – –	 0.8 –	V
Enable Input Current Logic High Logic Low	 V_{EN} = 5 V V_{EN} = 0 V, T_J < 85 °C	 I_{EN_ON} I_{EN_OFF}	 – –	 3 0.5	 5 1	μA
DT (Reset Delay Time Select)						
DT Threshold Voltage Logic Low Logic High		$V_{th(DT)}$	 – 2	 – –	 0.8 –	V
DT Input Current	V_{DT} = 5 V	I_{DT}	–	–	1	μA
RESET OUTPUT RO						
Output Voltage Reset Threshold (Note 14)	V_{out} decreasing V_{in} > 5.5 V	V_{RT}	90	93	96	%V_{out}
Reset Hysteresis		V_{RH}	–	2.0	–	%V_{out}
Maximum Reset Sink Current	V_{out} = 4.5 V, V_{RO} = 0.25 V	I_{ROmax}	1.75	–	–	mA
Reset Output Low Voltage	V_{out} > 1 V, I_{RO} < 200 μA	V_{ROL}	–	0.15	0.25	V
Reset Output High Voltage		V_{ROH}	4.5	–	–	V
Integrated Reset Pull Up Resistor		R_{RO}	15	30	50	kΩ
Reset Delay Time (Note 14)	Min time available, DT connected to GND Max time available, DT connected to V_{out}	t_{RD}	6.4 102.4 (−20 %)	8 128	9.6 153.6 (+20 %)	ms
Reset Reaction Time (see Figure 29)		t_{RR}	16	25	38	μs
EARLY WARNING (SI and SO)						
Sense Input Threshold (NCV8667y0) (Adjustable EW Threshold Option) High Low		$V_{SI(th)}$	 1.25 1.20	 1.33 1.25	 1.40 1.33	V
Early Warning Input Voltage Threshold (Preset EW Threshold Values) NCV8667y2 High Low	R_{SI1} = 480 kΩ, R_{SI2} = 520 kΩ (internal resistor divider values, see Figure 3) R_{SI_ext} = 150 kΩ (±1%, ±100 ppm/°C) (external resistor value, see Figure 26)	$V_{in\_EW(th)}$	 5.67 5.30	 6.30 5.89	 6.92 6.47	V
Sense Input Current (NCV8667y0) (Adjustable EW Threshold Option)	 V_{SI} = 5 V	I_{SI}	 −1	 0.1	 1	μA

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V.
12. Values based on design and/or characterization.
13. I_q for Preset EW Threshold Options is measured when R_{SI_ext} is not used. For typical values of I_q vs R_{SI_ext} see Figure 27.
14. See APPLICATION INFORMATION section for Reset Threshold and Reset Delay Time Options

ELECTRICAL CHARACTERISTICS V_{in} = 13.2 V, V_{EN} = 3 V, V_{DT} = GND, V_{SI} = V_{out} (NCV8667y0 only), R_{SI1}, R_{SI2}, R_{SI_ext} not used, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40 °C to 150°C; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
EARLY WARNING (SI and SO)						
Integrated Sense Output Pull Up Resistor		R_{SO}	15	30	50	kΩ
Sense Output Low Voltage	V_{SI} < 1.2 V, I_{SO} < 200 μA, V_{out} > 1 V	V_{SOL}	–	0.15	0.25	V
Sense Output High Voltage		V_{SOH}	4.5	–	–	V
Maximum Sense Output Sink Current	V_{out} = 4.5 V, V_{SI} < 1.2 V, V_{SO} = 0.25 V	I_{SOmax}	1.75	–	–	mA
SI High to SO High Reaction Time (Adjustable EW Threshold Option NCV8667y0)	V_{SI} increasing	t_{PSOLH}	–	7	12	μs
SI Low to SO Low Reaction Time (Adjustable EW Threshold Option NCV8667y0)	V_{SI} decreasing	t_{PSOHL}	–	3.8	5.0	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 11)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 11)		T_{SH}	–	25	–	°C

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V.
12. Values based on design and/or characterization.
13. I_q for Preset EW Threshold Options is measured when R_{SI_ext} is not used. For typical values of I_q vs R_{SI_ext} see Figure 27.
14. See APPLICATION INFORMATION section for Reset Threshold and Reset Delay Time Options

TYPICAL CHARACTERISTICS

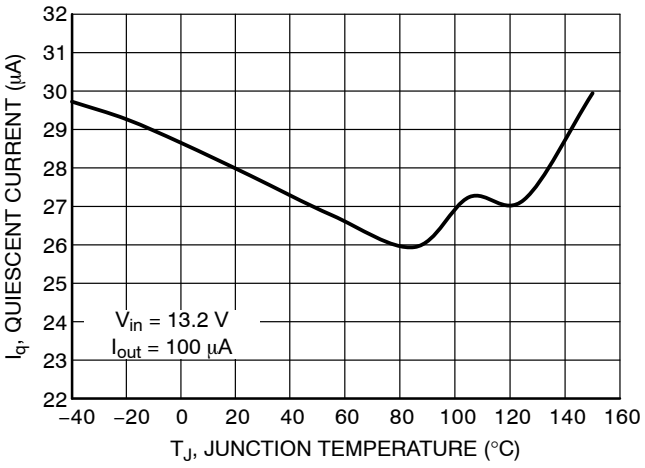


Figure 6. Quiescent Current vs. Temperature (NCV8667y0)

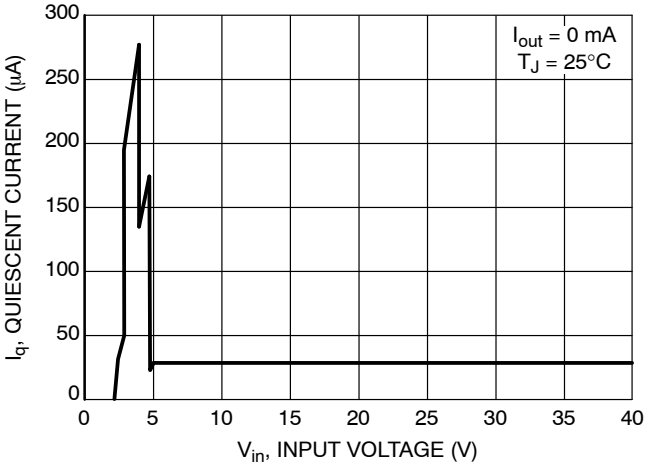


Figure 7. Quiescent Current vs. Input Voltage (NCV8667y0)

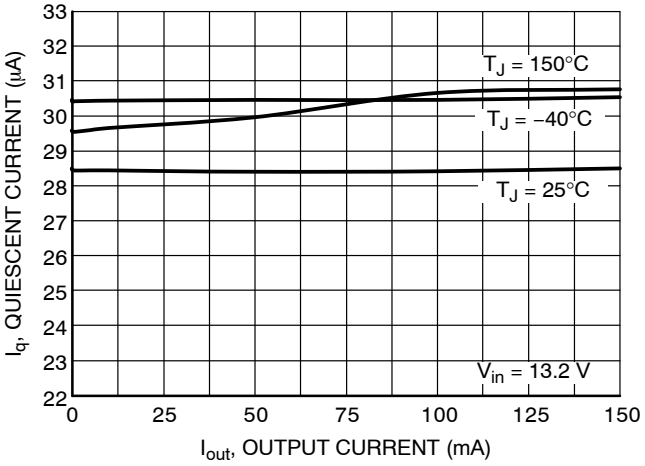


Figure 8. Quiescent Current vs. Output Current (NCV8667y0)

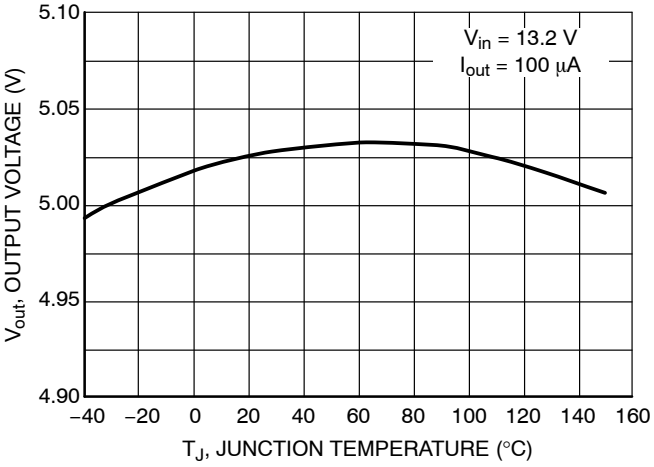


Figure 9. Output Voltage vs. Temperature

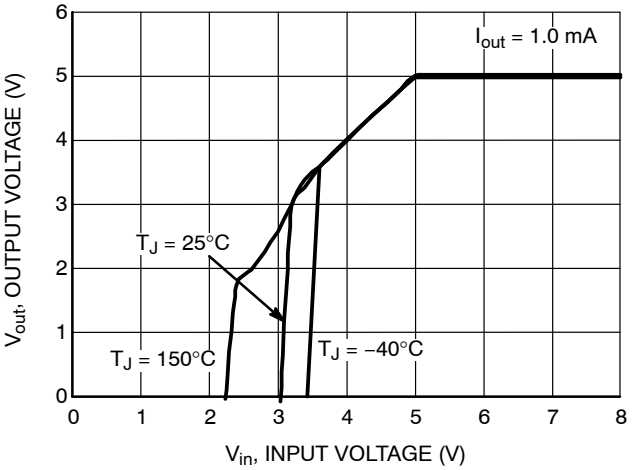


Figure 10. Output Voltage vs. Input Voltage

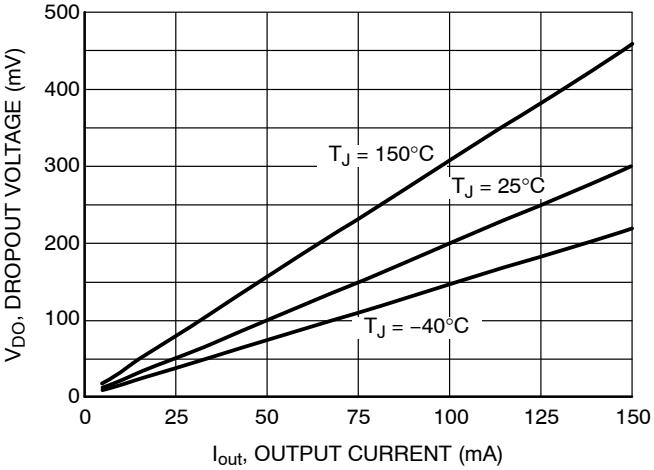


Figure 11. Dropout vs. Output Current

TYPICAL CHARACTERISTICS

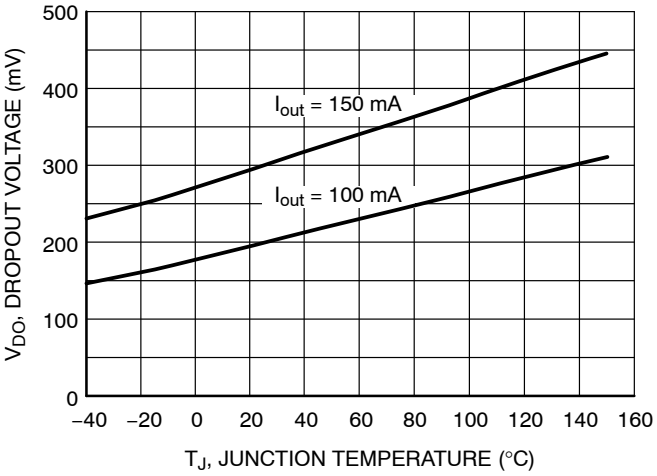


Figure 12. Dropout vs. Temperature

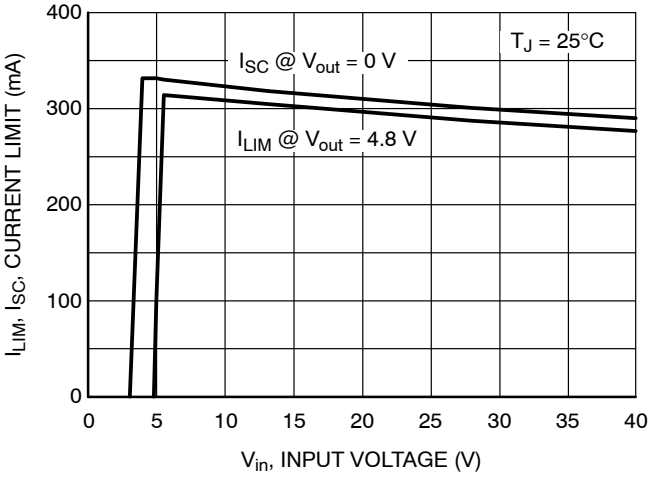


Figure 13. Output Current Limit vs. Input Voltage

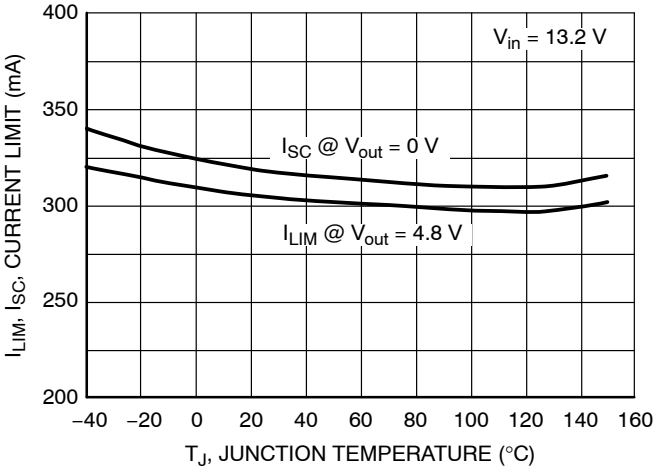


Figure 14. Output Current Limit vs. Temperature

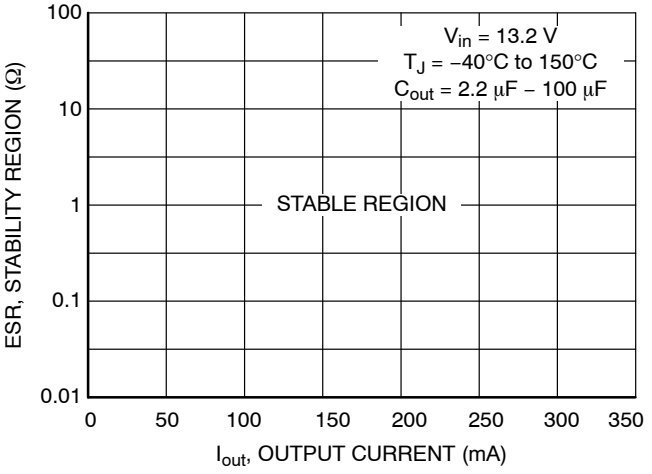


Figure 15. C_{out} ESR Stability vs. Output Current

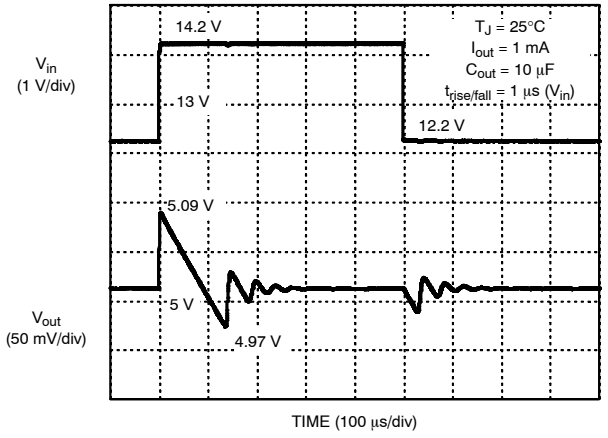


Figure 16. Line Transients

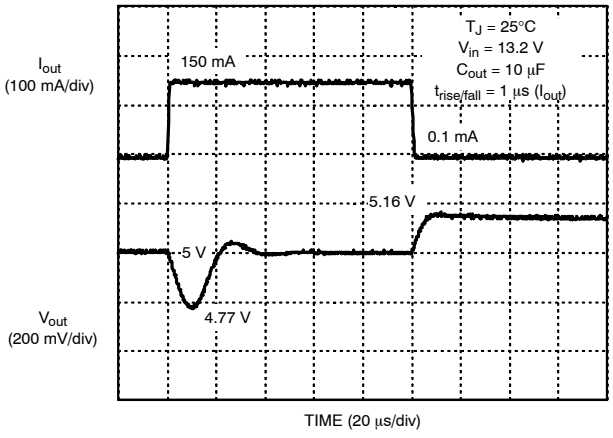


Figure 17. Load Transients

TYPICAL CHARACTERISTICS

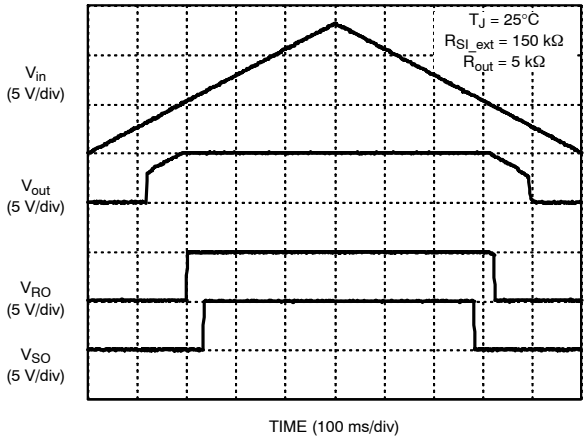


Figure 18. Power Up and Down Transient

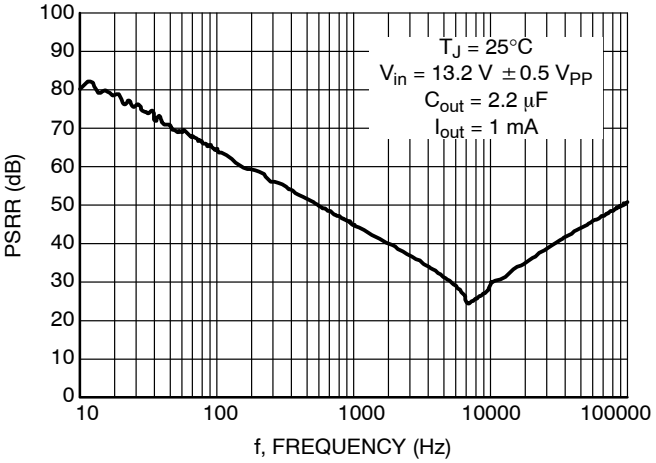


Figure 19. PSRR vs. Frequency

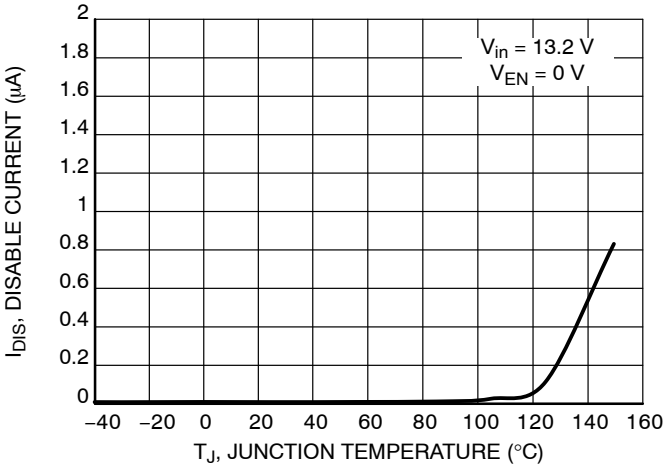


Figure 20. Disable Current vs. Temperature

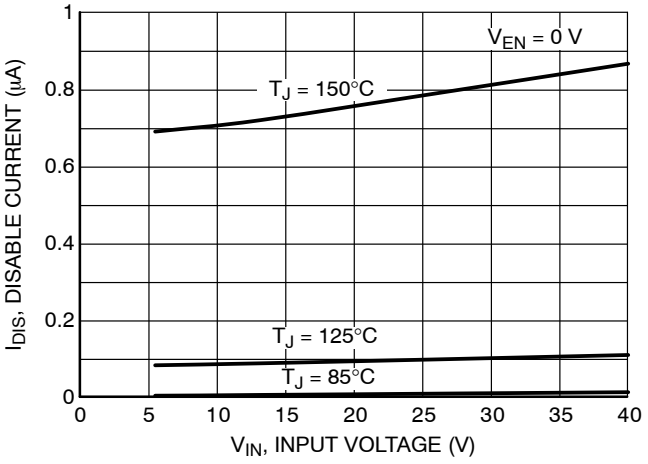


Figure 21. Disable Current vs. Input Voltage

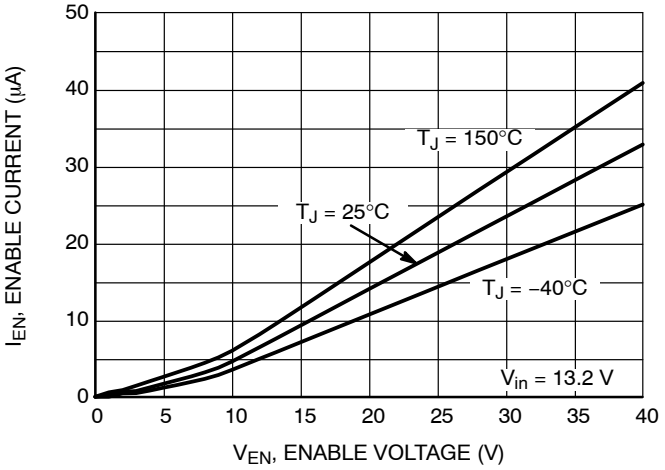


Figure 22. Enable Current vs. Enable Voltage

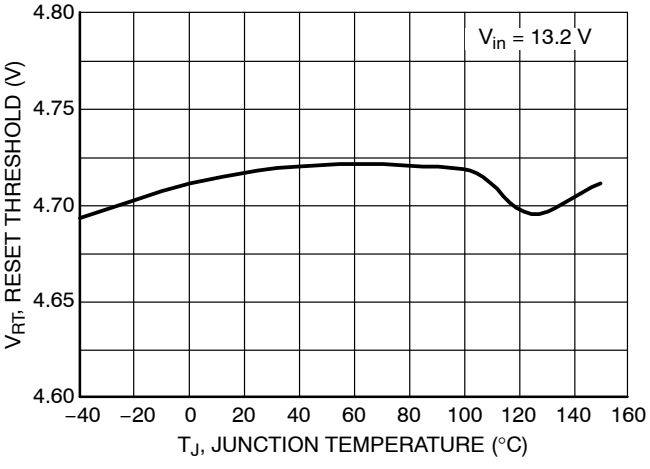


Figure 23. Reset Threshold vs. Temperature

TYPICAL CHARACTERISTICS

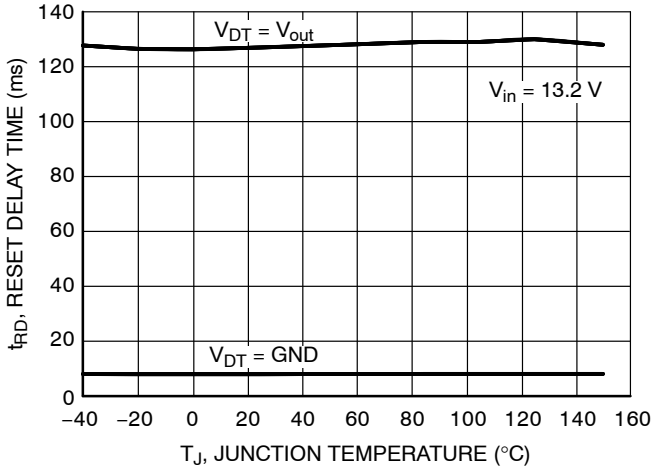


Figure 24. Reset Time vs. Temperature (NCV86671z)

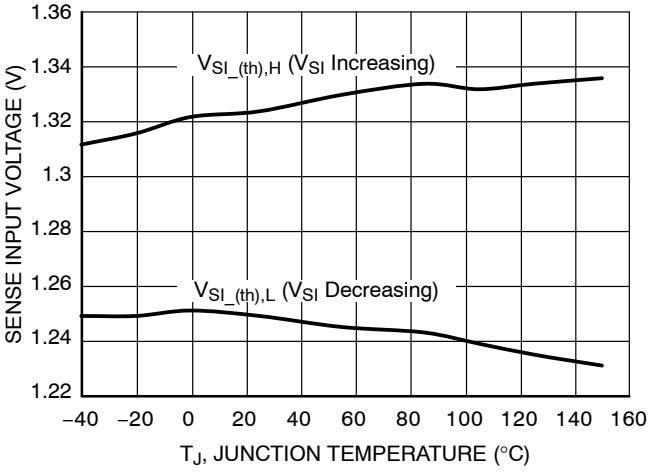


Figure 25. SI Threshold vs. Temperature (NCV8667y0)

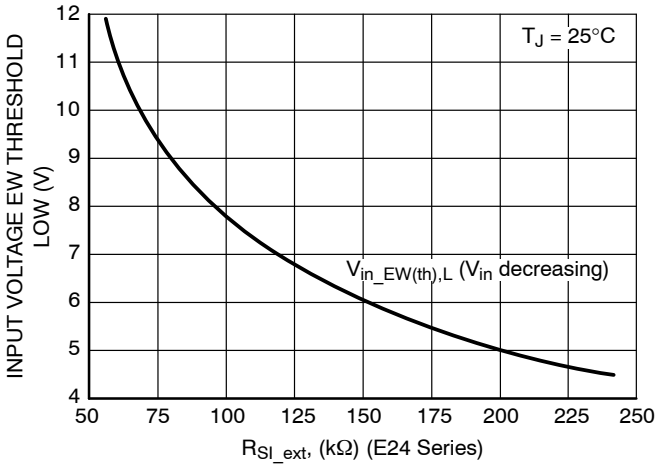


Figure 26. Input Voltage EW Threshold Low vs. R_{SI_ext} (Calculated Using E24 Series)

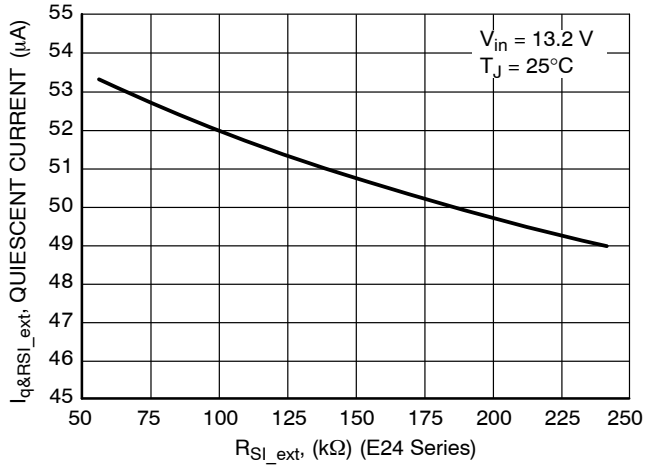


Figure 27. Quiescent Current vs. R_{SI_ext} (Including I_{RSI_ext}, Calculated Using E24 Series)

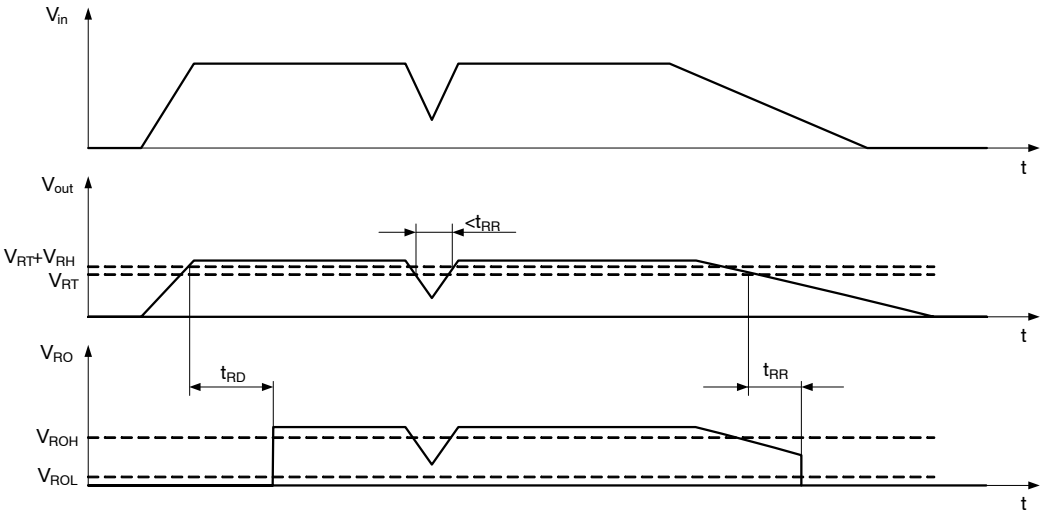


Figure 28. Reset Function and Timing Diagram

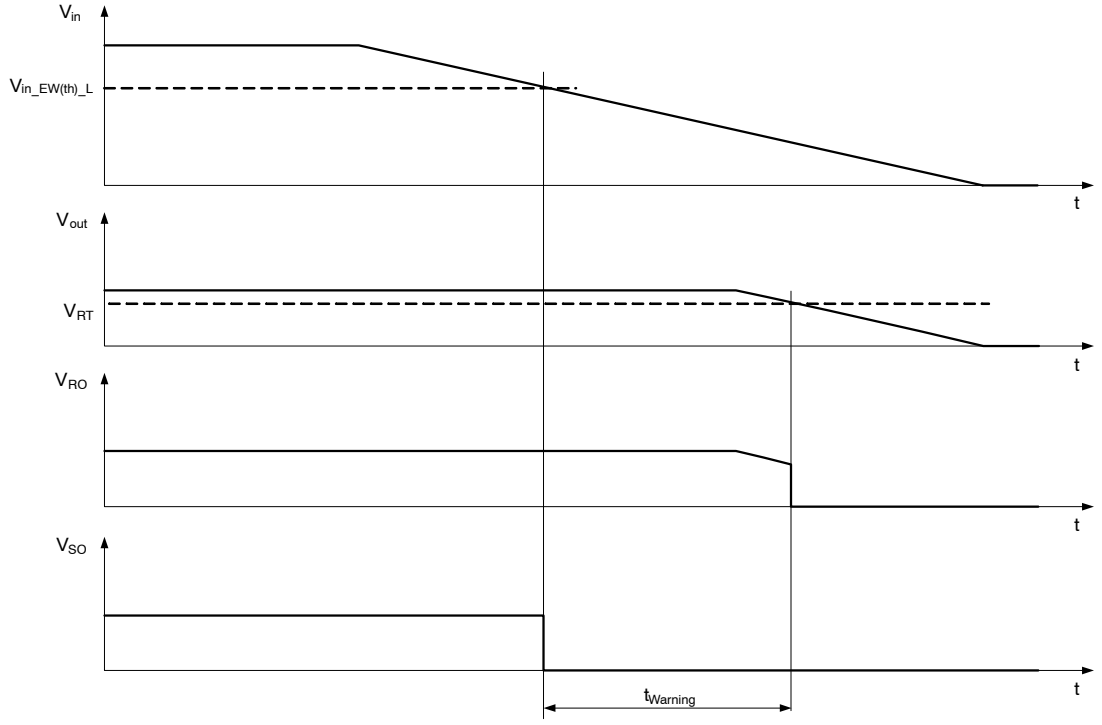


Figure 29. Input Voltage Early Warning Function Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Current

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current.

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. It means that the device is capable to supply minimum 200 mA without sending Reset signal to microprocessor.

Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8667 regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 6 to 29.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8667 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8667 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs. Output Current is shown in Figure 15. The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load transient response.

Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet.

Reset Delay Time Select

Selection of the NCV8667yz devices and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or OUT, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability. The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 28. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{out} = 1.0 V. The Reset Output (RO) circuitry includes internal pull−up connected to the output (V_{out}) No external pull−up is necessary.

RESET DELAY AND RESET THRESHOLD OPTIONS

Part Number	DT = GND Reset Time	DT = V_{out} Reset Time	Reset Threshold
NCV86671z	8 ms	128 ms	93%
NCV86675z	16 ms	32 ms	93%

NOTE: The timing values can be selected from following list: 8, 16, 32, 64, 128 ms. The reset threshold values can be selected from the following list: 90% and 93%. Contact factory for other timing combinations not included in the table.

Sense Input (SI) / Sense Output (SO) Voltage Monitor

An on−chip comparator is available to provide early warning to the microprocessor of a possible reset signal (Figure 29). The Sense Output is from an open drain driver with an internal 30 kΩ pull up resistor to output V_{out}. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time ($t_{Warning}$) to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point of input voltage is programmed by internal resistor divider and external resistor R_{SI_ext}. If R_{SI_ext} is not used following Preset Early Warning Threshold would apply:

EARLY WARNING PRESET OPTIONS

Part Number	R_{SI1} (internal)	R_{SI2} (internal)	Input Voltage Early Warning Threshold Low (Typ) (R_{SI_ext} not used)
NCV8667y2	480 kΩ	520 kΩ	2.37 V

Practically only preset options above 4.5 V can be used without R_{SI_ext} due to minimum operating input voltage value limitation. For other preset options the trip point has to be adjusted externally using R_{SI_ext} resistor connected between input monitor SI and GND (see Figure 1). For other preset options R_{SI_ext} has to be used to achieve $V_{in\_EW(th)}$ > 5.5 V (minimum operating input voltage value) . The value for R_{SI_ext} is recommended to be selected in range from 50 kΩ to 250 kΩ and the trip point can be shifted according to Figure 26. In case of R_{SI_ext} values higher than 200 kΩ two resistors in series could be used in order to eliminate leakage current of the resistor and hence ensure precision of its resistance value. The higher is R_{SI_ext} the lower is overall Quiescent Current of the application (see Figure 27). General formulas for calculation of $V_{in\_EW(th)Low}$ or R_{SI_ext}

for selected preset Early Warning options are described by Equations 1 and 2.

$$V_{in\_EW(th)\_Low} = 1.1\left(1 + \frac{R_{SI1} \times \left(R_{SI2} + R_{SI\_ext}\right)}{R_{SI2} \times R_{SI\_ext}}\right) + 0.25 \quad \text{(eq. 1)}$$

$$R_{SI\_ext} = 1.1\left(\frac{R_{SI1} \times R_{SI2}}{R_{SI2} \times \left(V_{in\_EW(th)\_Low} - 0.25\right) - 1.1 \times 10^6}\right) \quad \text{(eq. 2)}$$

Where:
R_{SI1},R_{SI2} − internal EW divider resistors (see Figure 3) (select values from Early Warning Preset Options table)
R_{SI-ext} − external resistor connected between SI and GND (recommended to be selected from 50 kΩ to 250 Ω)

If Adjustable Early Warning Threshold option (NCV8667y0) is used EW threshold is adjusted by external resistor divider. (See Figure 2) The values for R_{SI1} and R_{SI2} are selected for a typical threshold of 1.2 V on the SI pin according to Equations 3 and 4, where $V_{in\_EW(th)}$ is demanded value of input voltage at which Early Warning signal has to be generated. R_{SI2} is recommended to be selected in range of 100 kΩ to 1 MΩ. The higher are values of resistors R_{SI1} and R_{SI2} the lower is current flowing through the resistor divider, however this also increases a delay between Input voltage and SI input voltage caused by charging SI input capacitance with higher RC constant. The delay can be lowered by decreasing the resistors values with consequence of resistor divider current is increased.

$$V_{in\_EW(th)} = 1.25\left(1 + \frac{R_{SI1}}{R_{SI2}}\right) \quad \text{(eq. 3)}$$

$$R_{SI1} = R_{SI2}\left(\frac{V_{in\_EW(th)}}{1.2} - 1\right) \quad \text{(eq. 4)}$$

Sense Output

The Sense Output is from an open drain driver with an internal 30 kΩ pull up resistor to V_{out}. Figure 26 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 1. If the input voltage decreases the output voltage decreases as well. If the SI input low threshold voltage is crossed it causes the voltage on the SO output goes low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal.

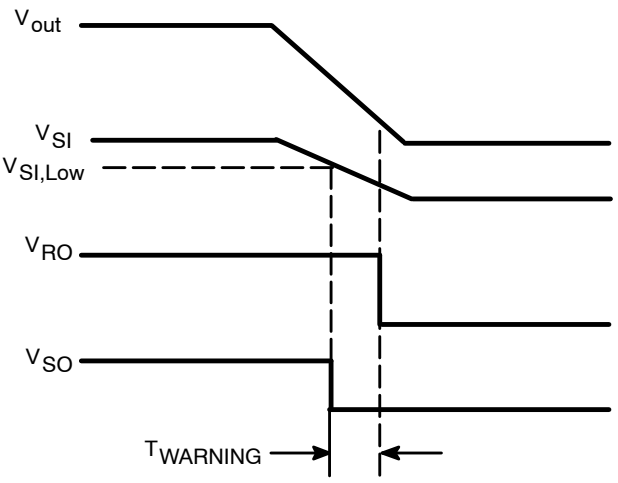


Figure 30. SO Warning Timing Diagram

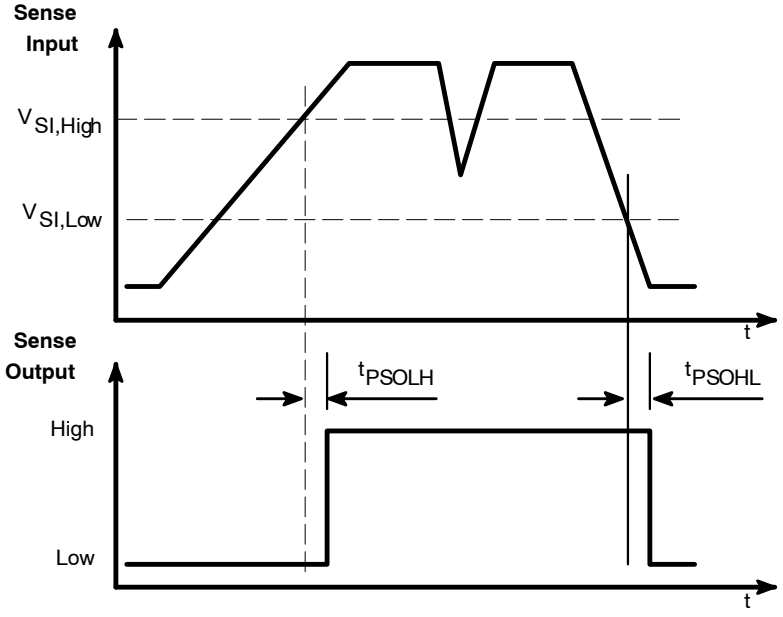


Figure 31. Sense Input to Sense Output Timing Diagram

Thermal Considerations

As power in the NCV8667 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8667 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8667 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 5)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8667 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.33 W when the ambient temperature (T_A) is 25°C. See Figure 29 for R_{thJA} versus PCB area. The power dissipated by the NCV8667 can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 6)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 7)}$$

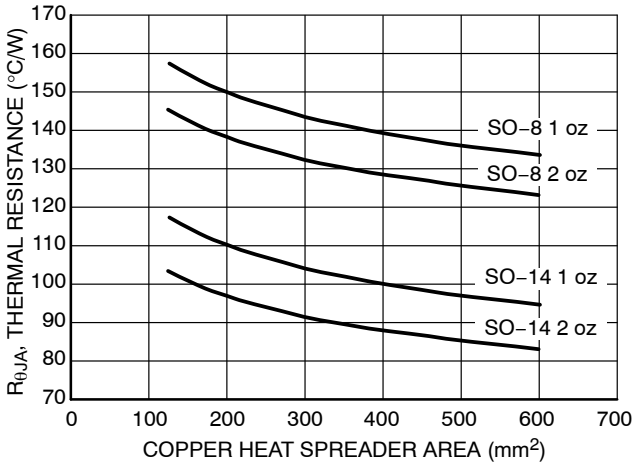


Figure 32. Thermal Resistance vs. PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8667 and make traces as short as possible.

ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time DT = GND/V_{out}	Reset Threshold (Typ)	Input Voltage Early Warning Threshold Low (Typ) R_{SI_ext} = 150 kΩ	Marking	Package	Shipping†
NCV866710D150R2G	5.0 V	8/128 ms	93 %	N/A	667105	SO−8 (Pb−Free)	2500 / Tape & Reel
NCV866710D250R2G	5.0 V	8/128 ms	93 %	N/A	V86671050G	SO−14 (Pb−Free)	2500 / Tape & Reel
NCV866752D250R2G	5.0 V	16/32 ms	93 %	5.89 V	V86675250G	SO−14 (Pb−Free)	2500 / Tape & Reel

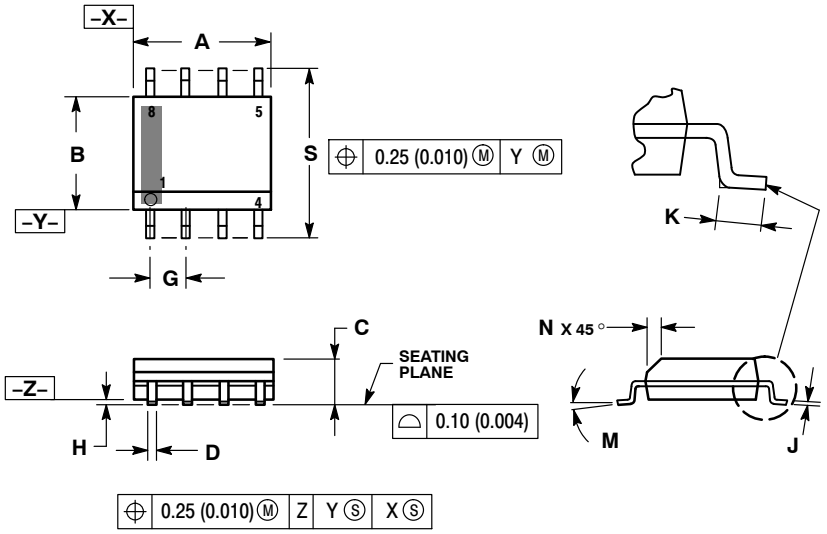
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

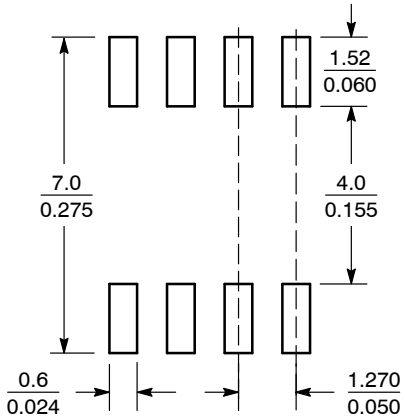
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

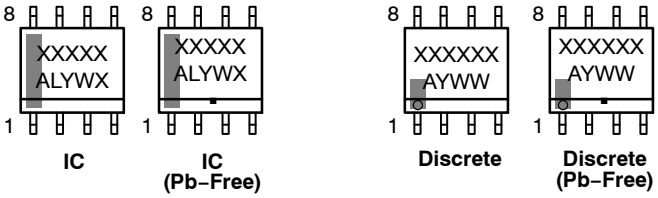
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

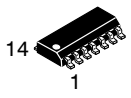
STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

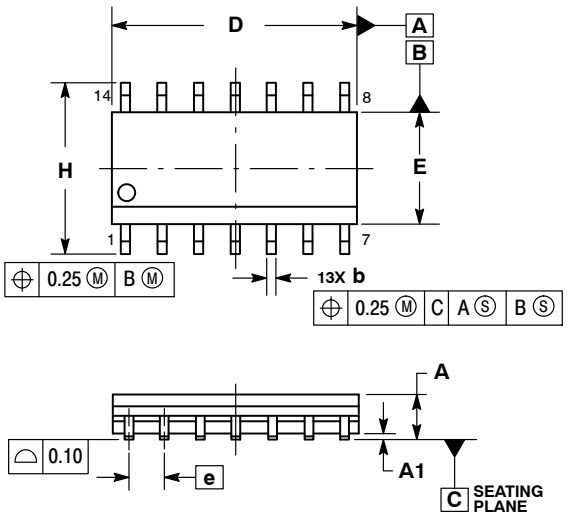
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

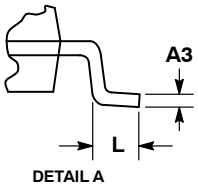


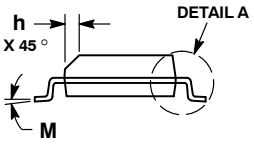
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



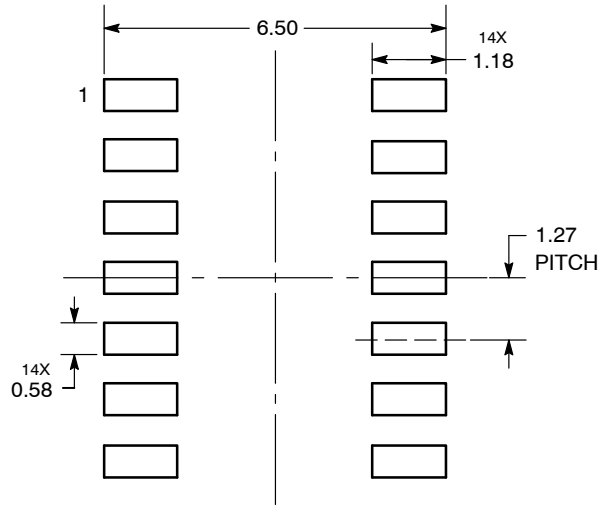




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

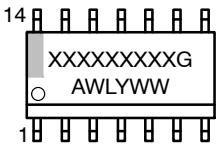
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊