Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **N1710-01** Date: November 8, 2017
Product Affected: 8V49NS0312NLGI(8)

Date Effective: February 8, 2018

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ☐ Product Mark
- ☐ Back Mark
- ☐ Date Code
- ■ Other Datasheet change only

Contact: TSD Clock Team
E-mail: clocks@idt.com

Attachment: ■ Yes ☐ No
Samples: Samples are available now.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ☐ Other

This notice is to advise our customers that the QD fractional output divider's max. frequency is updated to 138MHz to meet period jitter compliance.

There is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in Table 28.

In the event frequency is higher than 138MHz , output clock will have higher period jitter. As such, IDT would like to recommend customer to use 8V49NS0412 if they need to run above 138MHz since the two devices are drop in compatible.

RELIABILITY/QUALIFICATION SUMMARY:

There is no change in die technology/process.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT 1 - PCN #: N1710-01

PCN Type: Datasheet Revision Change

Data Sheet Change: Yes

Detail of Change: This notice is to advise our customers that the QD fractional output divider's max. frequency is updated to 138MHz to meet period jitter compliance.

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Datasheet Changes: Table 28

From:

AC Electrical Characteristics

Table 28: AC Characteristics,[a] V_{CC_X}[b] = V_{CCOX}[c] = 3.3V+5%, T_A = -40°C to +85°C, V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency			2400		2500	MHz
f_{PFD}	Phase / Frequency Detector Frequency			5		200	MHz
f_{OUT}	Output Frequency	QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1]		10.91		2500	MHz
		QD0, nQD0	Integer Divider Selected	10.91		2500	MHz
			Fractional Divider Selected	20		250	MHz
		QD1	Integer Divider Selected	10.91		250	MHz
			Fractional Divider Selected	20		250	MHz
*t*sk(b)	Bank Skew[d, e, f]	Bank A	Same Frequency and Output Type Only valid for skew between outputs in the same bank			45	ps
		Bank B				45	
		Bank C				20	

To:

AC Electrical Characteristics

Table 28: AC Characteristics,[a] V_{CC_X}[b] = V_{CCOX}[c] = 3.3V+5%, T_A = -40°C to +85°C, V_{EE} = 0V

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f_{OUT}	Output Frequency	QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1]		10.91		2500	MHz
		QD0, nQD0	Integer Divider Selected	10.91		2500	MHz
			Fractional Divider Selected	20		138	MHz
		QD1	Integer Divider Selected	10.91		250	MHz
			Fractional Divider Selected	20		138	MHz
*t*sk(b)	Bank Skew[d, e, f]	Bank A	Same Frequency and Output Type Only valid for skew between outputs in the same bank			45	ps
		Bank B				45	
		Bank C				20	