

LMX8410L High-Performance Mixer With Integrated Synthesizer

1 Features

- Wideband RF Input: 4 to 10 GHz
- Large IF Bandwidth: DC to 1350 MHz
- Input IP3: 28 dBm at 5-GHz RF Input
- Noise Figure: 15 dB at 5-GHz RF Input
- High Voltage Conversion Gain: 11 dB at 5-GHz RF Input
- Integrated Wideband RF Input Balun
- Automatic Offline DC Offset Correction to ± 2 mV
- Programmable IMRR Calibration
- SYNC Feature for Multiple Devices
- High-Performance Integrated LO Synthesizer: 56.5-dBc DSB Integrated Noise at 5-GHz carrier
- External LO mode: Integrated LO Synthesizer can be Bypassed; Support External LO Injection
- Integrated Low-Noise LDOs
- 7-mm \times 7-mm 48-pin QFN Package

2 Applications

- Test and Measurement Equipment
- Wireless Infrastructure
- Phased Array Radar
- Microwave Backhaul
- Satellite Communications
- Software-Defined Radio

3 Description

The LMX8410L is a high-performance wideband (RF frequency input from 4 to 10 GHz) I/Q demodulator with an integrated LO and IF amplifier. With IIP3 of 28 dBm and NF of 15 dB (both at 5GHz), it provides excellent dynamic range for high performance applications. The device offers large complex bandwidth of 2.7 GHz for high data-rate applications.

The LMX8410L offers an automatic DC offset correction algorithm that reduces the offset to less than ± 2 mV. Fine control of gain and phase of I and Q channels is enabled using SPI interface to achieve high image rejection.

The LMX8410L has a high level of integration providing high performance while saving board space and complexity. It integrates a wideband RF input balun, eliminating the need for external baluns. It integrates a high-performance PLL and VCO, eliminating the need for external LO and LO driver. The device also integrates an IF amplifier and several low noise LDOs, further simplifying the board.

The LMX8410L integrates a very low-noise synthesizer, with a PLL FOM of -236 dBc/Hz, providing up to 56.5-dBc DSB integrated noise at 5 GHz carrier. The LO allows for phase synchronization across multiple devices. The high-performance synthesizer output can be brought out to drive another stage or a data converter. The integrated LO can be bypassed for applications that share a common external LO.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------------|
| LMX8410L | VQFN (48) | 7.00 mm \times 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

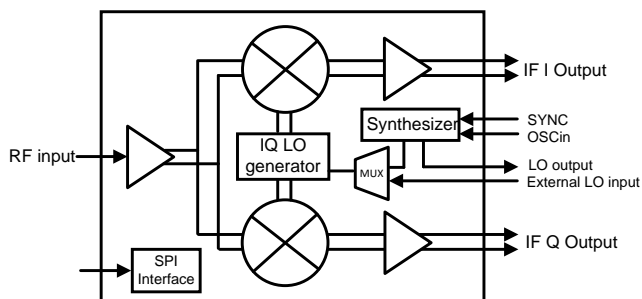


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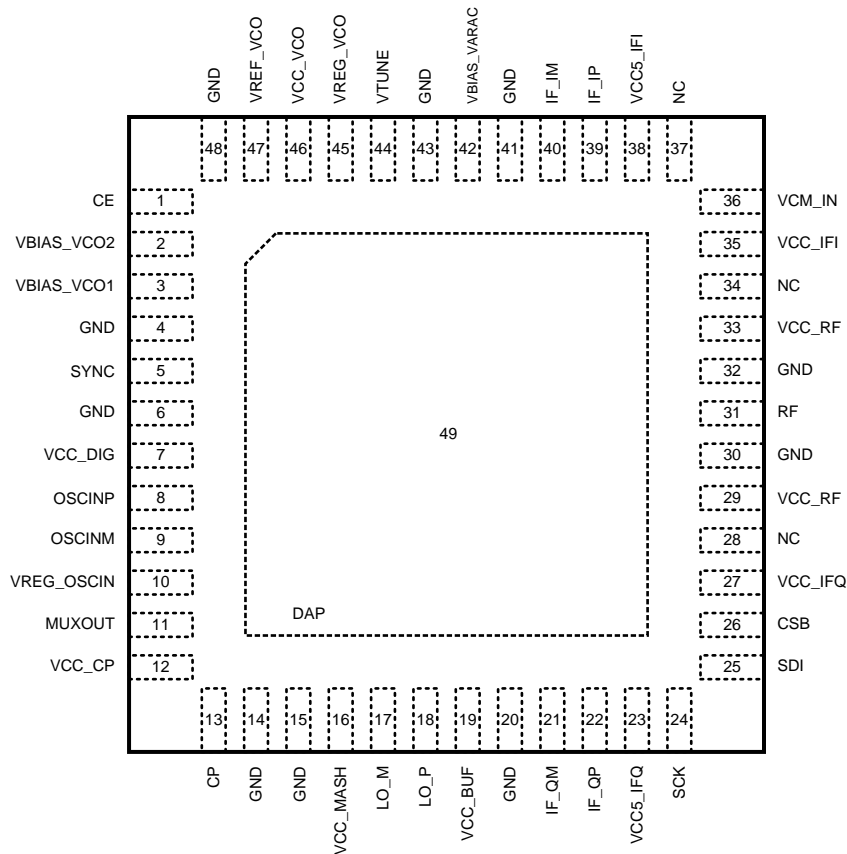
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (March 2018) to Revision A | Page |
|--|-------------|
| • First release of production-data data sheet | 1 |
| • Changed many numbers in electrical specifications table. | 6 |
| • Added typical performance characteristics section. | 14 |
| • Changed and added significant details in detailed descriptions sections. Added sections, changed several portions of the register map..... | 22 |

5 Pin Configuration and Functions

**RGZ Package
48-Pin QFN
Top View**



Pin Functions

| PIN | | I/O | DESCRIPTION |
|------|------------|--------|--|
| NAME | NAME | | |
| 1 | CE | Input | Chip Enable input. Active HIGH powers on the device. 1.8V to 3.3V logic. |
| 2 | VBIAS_VCO2 | Bypass | VCO bias. Requires connecting 10- μ F capacitor to VCO ground. Place close to pin. If using external LO, this pin should either be floated or configured the same way as internal LO mode. |
| 3 | VBIAS_VCO1 | Bypass | VCO bias. Requires connecting 10- μ F capacitor to VCO ground. Place close to pin. If using external LO, this pin should either be floated or configured the same way as internal LO mode. |
| 4 | GND | Ground | VCO ground. VBIAS pin capacitors must bypass to this point. |
| 5 | SYNC | Input | Trigger pin for synchronizing multiple devices. If using external LO, tie this pin to GND. |
| 6 | GND | Ground | Digital ground. VCC_DIG bypass capacitors must bypass to this point. |
| 7 | VCC_DIG | Supply | Digital supply. TI recommends connecting 0.1- μ F capacitor to digital ground. |
| 8 | OSCINP | Input | Reference input clock (+). High input impedance. Requires connecting series capacitor (0.1 μ F recommended). If using external LO, tie this pin to GND. |
| 9 | OSCINM | Input | Reference input clock (-). High input impedance. Requires connecting series capacitor (0.1 μ F recommended). If using external LO, tie this pin to GND. |
| 10 | VREG_OSCIN | Bypass | Internal LDO output. Requires connecting 1- μ F capacitor to digital ground. Place close to pin. If using external LO, this pin should either be floated or configured the same way as internal LO mode. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|------|-------------|--------------|--|
| NAME | NAME | | |
| 11 | MUXOUT | Output | Readback or lock detect output. Pin mode configured by internal register settings. |
| 12 | VCC_CP | Supply | Charge pump supply. TI recommends connecting 0.1 μ F and 100 pF to charge pump ground. Place close to pin. This pin must be connected to VCC, even if using external LO. |
| 13 | CP | Output | Charge pump output. TI recommends connecting C1 of loop filter close to pin. If using external LO, this pin should either be floated or configured the same way as internal LO mode. |
| 14 | GND | Ground | Charge pump ground. VCC_CP bypass capacitors must bypass to this point. |
| 15 | GND | Ground | MASH engine ground. VCC_MASH bypass capacitors must bypass to this point. |
| 16 | VCC_MASH | Supply | MASH engine supply. TI recommends connecting 0.1 μ F and 100 pF to MASH engine ground. Place close to pin. This pin must be connected to VCC, even if using external LO. |
| 17 | LO_M | Input/Output | Internal LO differential output (–) or external LO differential input (–). In differential output mode, requires connecting 50- Ω resistor pullup to VCC as close as possible to pin. In differential input mode, remove the pull up resistors or inductors. The input should be capacitively coupled with internal biasing. See LO Interface for more information. |
| 18 | LO_P | Input/Output | Internal LO differential output (+) or external LO differential input (+). In differential output mode, requires connecting 50- Ω resistor pullup to VCC as close as possible to pin. In differential input mode, remove the pull up resistors or inductors. The input should be capacitively coupled with internal biasing. See LO Interface for more information. |
| 19 | VCC_BUF | Supply | LO buffer supply. TI recommends connecting 0.1 μ F and 100 pF to VCO ground. This pin must be connected to VCC, even if using external LO. |
| 20 | GND | Ground | IF amplifier Q-channel ground. Q-channel VCC5 bypass capacitors must bypass to this point. |
| 21 | IF_QM | Output | IF amplifier Q-channel differential output (–). TI recommends connecting series 50- Ω resistor close to pin. |
| 22 | IF_QP | Output | IF amplifier Q-channel differential output (+). TI recommends connecting series 50- Ω resistor close to pin. |
| 23 | VCC5_IFQ | Supply | IF amplifier Q-channel 5-V supply. TI recommends connecting 0.1 μ F and 100 pF to IF amplifier Q-channel ground. Place close to pin. |
| 24 | SCK | Input | SPI clock signal. High impedance CMOS input. 1.8-V to 3.3-V logic. |
| 25 | SDI | Input | SPI data signal. High impedance CMOS input. 1.8-V to 3.3-V logic. |
| 26 | CSB | Input | SPI chip select signal. High impedance CMOS input. 1.8-V to 3.3-V logic. |
| 27 | VCC_IFQ | Supply | IF mixer Q-channel supply. TI recommends connecting 0.1 μ F and 100 pF to digital ground. |
| 28 | NC | N/A | No connect. Pin is not internally connected and may be floated or shorted to other nodes. |
| 29 | VCC_RFQ | Supply | RF Q-channel supply. TI recommends connecting 0.1 μ F and 100 pF to digital ground. |
| 32 | GND | Ground | RF input path ground. |
| 31 | RF | Input | RF input. Single-ended. Must be AC coupled. |
| 32 | GND | Ground | RF input path ground. |
| 33 | VCC_RFI | Supply | RF I-channel supply. TI recommends connecting 0.1 μ F and 100 pF to digital ground. |
| 34 | GND | Ground | Should be connected IF ground. |
| 35 | VCC_IFI | Supply | IF mixer I-channel supply. TI recommends connecting 0.1 μ F and 100 pF to digital ground. |
| 36 | VCM_IN | Input | Common-mode voltage input. When the VCM_CONFIG register is set to external (0xF), the voltage on this pin sets the common-mode voltage of the IF amplifiers. |
| 37 | NC | Ground | Connect this pin to IF ground. |
| 38 | VCC5_IFI | Supply | IF amplifier I-channel 5-V supply. TI recommends connecting 0.1 μ F and 100 pF to IF amplifier I-channel ground. Place close to pin. |
| 39 | IF_IP | Output | IF amplifier I-channel differential output (+). TI recommends connecting series 50- Ω resistor close to pin. |
| 40 | IF_IM | Output | IF amplifier I-channel differential output (–). TI recommends connecting series 50- Ω resistor close to pin. |
| 41 | GND | Ground | IF amplifier I-channel ground. I-channel VCC5 bypass capacitors should bypass to this point. |
| 42 | VBIAS_VARAC | Bypass | VCO varactor bias. Requires connecting 10 μ F capacitor to VCO ground. If using external LO, this pin should either be floated or configured the same way as internal LO mode. |
| 43 | GND | Ground | VCO ground. Varactor bias bypass capacitor should bypass to this point. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|------|----------|--------|---|
| NAME | NAME | | |
| 44 | VTUNE | Input | VCO tuning voltage input. If using internal LO, connect the output of the loop filter to this point. If using external LO, tie this pin to GND. |
| 45 | VREG_VCO | Bypass | VCO LDO output node. Requires connecting 10- μ F capacitor to VCO ground. Place close to pin. This capacitor must be present even if used in external LO mode. |
| 46 | VCC_VCO | Supply | VCO supply. TI recommends connecting 0.1- μ F and 100-pF capacitors to VCO ground. This pin must be connected to VCC, even if using external LO. |
| 47 | VREF_VCO | Bypass | VCO LDO reference node. Requires connecting 1- μ F capacitor to VCO ground. If using external LO, this pin should either be floated or configured the same way as internal LO mode. |
| 48 | GND | Ground | VCO ground. VCO LDO, LDO reference, and supply bypass capacitors must bypass to this point. |
| 49 | PAD | Ground | Die attach pad. Internally connected to ground. TI recommends shorting ground pins to this pad on the same plane, if possible. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------|----------------------------------|------|-----|------|
| V_{CC} | Power supply voltage, 3.3-V rail | -0.3 | 3.6 | V |
| V_{CC5} | Power supply voltage, 5-V rail | -0.3 | 5.3 | V |
| P_D | Power dissipation | | 5 | W |
| T_J | Junction temperature | -40 | 150 | °C |
| T_{stg} | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|---|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins | 2500 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins | 500 |

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------|---------------------------------|------|-----|------|------|
| V_{CC} | Power supply voltage, 3.3V rail | 3.15 | 3.3 | 3.45 | V |
| V_{CC5} | Power supply voltage, 5V rail | 4.75 | 5 | 5.25 | V |
| T_A | Ambient temperature | -40 | 25 | 85 | °C |
| T_J | Junction temperature | | | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ (2) | | LMX8410L | UNIT |
|-----------------------------------|--|------------|------|
| | | RGZ (VQFN) | |
| | | 48 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 21.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 9.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 5.6 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 0.1 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 5.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.4 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Thermal model based on JEDEC standard coupon, 50.8 mm × 50.8 mm × 1.6 mm, six-layer Cu, 0.5 oz top layer, 2 oz else. 6 × 6 thermal vias in DAP, 0.2 mm diameter.

6.5 Electrical Characteristics

Measurements are done at 25 degree C. Parameters are measured at IF = 65MHz with high side injection, unless otherwise noted. Measurements are done with external VCM = 1.7V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|-----------------|------|------|-------|------|
| POWER SUPPLY | | | | | | |
| V _{CC} | Power supply voltage, 3.3-V rail | | 3.15 | 3.3 | 3.45 | V |
| I _{CC} | Power supply current, 3.3-V rail | Internal LO | | 650 | | mA |
| | | External LO | | 330 | | |
| V _{CC5} | Power supply voltage, 5-V rail | | 4.75 | 5 | 5.25 | V |
| I _{CC5} | Power supply current both channels I and Q, 5-V rail | | | 130 | | mA |
| FREQUENCY RANGES | | | | | | |
| F _{RF} | RF port frequency range | | 4000 | | 10000 | MHz |
| F _{LO} | LO port frequency range | | 4000 | | 10000 | MHz |
| F _{IF} | IF port frequency range (3dB bandwidth) | | DC | | 1350 | MHz |
| DYNAMIC PERFORMANCE | | | | | | |
| NF | Noise figure | RF = 4 GHz | | 15 | | dB |
| | | RF = 5 GHz | | 15 | | |
| | | RF = 6 GHz | | 16 | | |
| | | RF = 7 GHz | | 17 | | |
| | | RF = 8 GHz | | 18 | | |
| | | RF = 9 GHz | | 19 | | |
| | | RF = 10 GHz | | 19 | | |
| G | Voltage gain ⁽¹⁾ | RF = 4 GHz | | 11 | | dB |
| | | RF = 5 GHz | | 11 | | |
| | | RF = 6 GHz | | 10.5 | | |
| | | RF = 7 GHz | | 9.5 | | |
| | | RF = 8 GHz | | 9 | | |
| | | RF = 10 GHz | | 7 | | |
| IIP3 | Input intercept point, 3rd order ⁽²⁾ | RF = 4 GHz | | 28 | | dBm |
| | | RF = 5 GHz | | 28 | | |
| | | RF = 6 GHz | | 26.5 | | |
| | | RF = 7 GHz | | 27 | | |
| | | RF = 8 GHz | | 26.5 | | |
| | | RF = 10 GHz | | 27 | | |
| IIP2 | Input intercept point, 2nd order (uncalibrated) | RF = 4 GHz | | 48 | | dBm |
| | | RF = 5 GHz | | 48 | | |
| | | RF = 6 GHz | | 46 | | |
| | | RF = 7 GHz | | 44 | | |
| | | RF = 8 GHz | | 45 | | |
| | | RF = 10 GHz | | 42 | | |

(1) For measurements that require RF input, RF input power is -10dBm unless otherwise specified.

(2) For two-tone measurements, tone separation is 17MHz.

Electrical Characteristics (continued)

Measurements are done at 25 degree C. Parameters are measured at IF = 65MHz with high side injection, unless otherwise noted. Measurements are done with external VCM = 1.7V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------------|-----------------|-----|-----|-----|------|
| SP _{2x2} | 2x2 spur [RF input power at -10 dBm] | RF = 4 GHz | | -58 | | dBc |
| | | RF = 5 GHz | | -58 | | |
| | | RF = 6 GHz | | -58 | | |
| | | RF = 7 GHz | | -54 | | |
| | | RF = 8 GHz | | -52 | | |
| | | RF = 9 GHz | | -50 | | |
| | | RF = 10 GHz | | -48 | | |
| SP _{3x3} | 3x3 spur [RF input power at -10 dBm] | RF = 4 GHz | | -75 | | dBc |
| | | RF = 5 GHz | | -75 | | |
| | | RF = 6 GHz | | -75 | | |
| | | RF = 7 GHz | | -75 | | |
| | | RF = 8 GHz | | -75 | | |
| | | RF = 9 GHz | | -75 | | |
| | | RF = 10 GHz | | -75 | | |
| OP _{1dB} | Output 1-dB compression point | RF = 4 GHz | | 12 | | dBm |
| | | RF = 5 GHz | | 12 | | |
| | | RF = 6 GHz | | 12 | | |
| | | RF = 7 GHz | | 12 | | |
| | | RF = 8 GHz | | 12 | | |
| | | RF = 9 GHz | | 12 | | |
| | | RF = 10 GHz | | 12 | | |
| IRR | Image rejection ratio [calibrated] | RF = 4 GHz | | 43 | | dB |
| | | RF = 5 GHz | | 43 | | |
| | | RF = 6 GHz | | 44 | | |
| | | RF = 7 GHz | | 44 | | |
| | | RF = 8 GHz | | 43 | | |
| | | RF = 9 GHz | | 42 | | |
| | | RF = 10 GHz | | 36 | | |
| ISO _{RFxIF} | RF to IF isolation | RF = 4 GHz | | 40 | | dB |
| | | RF = 5 GHz | | 40 | | |
| | | RF = 6 GHz | | 40 | | |
| | | RF = 7 GHz | | 40 | | |
| | | RF = 8 GHz | | 40 | | |
| | | RF = 9 GHz | | 40 | | |
| | | RF = 10 GHz | | 40 | | |
| LEAK _{RFxIF} | LO to IF leakage | LO = 4 GHz | | -35 | | dBm |
| | | LO = 5 GHz | | -35 | | |
| | | LO = 6 GHz | | -35 | | |
| | | LO = 7 GHz | | -35 | | |
| | | LO = 8 GHz | | -35 | | |
| | | LO = 9 GHz | | -35 | | |
| | | LO = 10 GHz | | -35 | | |

Electrical Characteristics (continued)

Measurements are done at 25 degree C. Parameters are measured at IF = 65MHz with high side injection, unless otherwise noted. Measurements are done with external VCM = 1.7V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-----|-------|------|-----------------|
| LEAK _{LOxRF} | LO to RF leakage (internal Lo mode) | LO = 4 GHz | | -60 | | dBm |
| | | LO = 5 GHz | | -60 | | |
| | | LO = 6 GHz | | -52 | | |
| | | LO = 7 GHz | | -50 | | |
| | | LO = 8 GHz | | -50 | | |
| | | LO = 9 GHz | | -45 | | |
| | | LO = 10 GHz | | -40 | | |
| PERFORMANCE TUNING | | | | | | |
| G _{IQ_CAL} | I/Q gain calibration range | IMRR_GCAL register full range | | ±0.5 | | dB |
| G _{IQ_STEP} | I/Q gain calibration step size | | | 0.05 | | dB |
| PH _{IQ_CAL} | I/Q phase calibration range | IMRR_PCAL register full range | | ±20 | | Deg |
| PH _{IQ_STEP} | I/Q phase calibration step size | Step size can be made reduced to 0.25 deg in fine accuracy mode | | 0.45 | | Deg |
| V _{DCOC} | calibrated differential DC offset | | | +/- 2 | | mV |
| PORTS | | | | | | |
| S _{11RF} | RF return loss | RF = 4 GHz | | 8 | | dB |
| | | RF = 5 GHz | | 19 | | dB |
| | | RF = 6 GHz | | 21 | | dB |
| | | RF = 7 GHz | | 16 | | dB |
| | | RF = 8 GHz | | 10 | | dB |
| | | RF = 9 GHz | | 9 | | dB |
| | | RF = 10 GHz | | 9 | | dB |
| S _{11LO} | LO return loss (differential measurement) | RF = 4 GHz | | 15 | | dB |
| | | RF = 5 GHz | | 15 | | dB |
| | | RF = 6 GHz | | 20 | | dB |
| | | RF = 7 GHz | | 17 | | dB |
| | | RF = 8 GHz | | 18 | | dB |
| | | RF = 9 GHz | | 17 | | dB |
| | | RF = 10 GHz | | 12 | | dB |
| P _{LO_IN} | External LO input power | 8 GHz RF _{IN} | | 6 | | dBm |
| P _{LO_OUT} | External LO output power ⁽³⁾ | <7 GHz RF _{out} | | 2 | | dBm |
| | | <10 GHz RF _{out} | | -1 | | dBm |
| V _{IF_RANGE} | IF output voltage swing (differential) | | | 2 | | V _{PP} |
| V _{CM} | IF common mode voltage, internal or external source | | 1.2 | 1.7 | 2 | V |
| P _{inRF} | RF input power | | | | 5 | dBm |
| LO SYNTHESIZER INPUT SIGNAL PATH | | | | | | |
| F _{OSCIN} | Reference oscillator port frequency range | OSC_2X = 0 | | 5 | 1400 | MHz |
| | | OSC_2X = 1 | | 5 | 200 | |
| V _{OSCIN} | Reference input voltage | AC-coupled required ⁽⁴⁾ | | 0.2 | 2 | V _{pp} |
| F _{MULT} | Multiplier frequency (when multiplier enabled) | Input range | | 30 | 70 | MHz |
| | | Output range | | 180 | 250 | |

(3) Output power, spurs, and harmonics can vary based on board layout and components.

(4) For lower VCO frequencies, the N divider minimum value can limit the phase detector frequency.

Electrical Characteristics (continued)

Measurements are done at 25 degree C. Parameters are measured at IF = 65MHz with high side injection, unless otherwise noted. Measurements are done with external VCM = 1.7V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-------|------|--------|
| LO SYNTHESIZER PHASE DETECTOR AND CHARGE PUMP | | | | | |
| F _{PD} | Phase detector frequency | Integer Mode (FRAC_ORDER = 0) | 0.125 | 400 | MHz |
| | | Fractional Mode (FRAC_ORDER = 1,2,3) | 5 | 300 | |
| | | Fractional Mode (FRAC_ORDER = 4) | 5 | 240 | |
| I _{CPOUT} | Charge pump leakage current | CPG = 0 | 15 | | nA |
| | Effective charge pump current (sum of up and down currents) | CPG = 4 | 3 | | mA |
| | | CPG = 1 | 6 | | |
| | | CPG = 5 | 9 | | |
| | | CPG = 3 | 12 | | |
| | | CPG = 7 | 15 | | |
| PN _{1/F} | Normalized PLL flicker noise | F _{PD} = 100 MHz, F _{VCO} = 12 GHz ⁽⁵⁾ | | -129 | dBc/Hz |
| PN _{FLAT} | Normalized PLL thermal noise floor | | | -236 | dBc/Hz |

- (5) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. $PLL_{FLAT} = PLL_{FOM} + 20\log(F_{VCO} / F_{PD}) + 10\log(F_{PD} / 1\text{Hz})$. $PLL_{FLICKER}(\text{offset}) = PLL_{FLICKER_NORM} + 20\log(F_{VCO} / 1\text{GHz}) - 10\log(\text{offset frequency} / 10\text{kHz})$. Once these two components are found, the total PLL noise can be calculated as $PLL_{NOISE} = 10\log(10^{PLL_{FLAT} / 10} + 10^{PLL_{FLICKER} / 10})$.

Electrical Characteristics (continued)

Measurements are done at 25 degree C. Parameters are measured at IF = 65MHz with high side injection, unless otherwise noted. Measurements are done with external VCM = 1.7V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|------------------------------|-----|------|-----|--------|
| LO SYNTHESIZER VCO | | | | | | |
| PN _{vco} | Open loop VCO phase noise | 8 GHz VCO, 10 kHz offset | | -80 | | dBc/Hz |
| | | 8 GHz VCO, 100 kHz offset | | -107 | | |
| | | 8 GHz VCO, 1 MHz offset | | -128 | | |
| | | 8 GHz VCO, 10 MHz offset | | -148 | | |
| | | 8 GHz VCO, 90 MHz offset | | -157 | | |
| | | 9.2 GHz VCO, 10 kHz offset | | -79 | | |
| | | 9.2 GHz VCO, 100 kHz offset | | -105 | | |
| | | 9.2 GHz VCO, 1 MHz offset | | -127 | | |
| | | 9.2 GHz VCO, 10 MHz offset | | -147 | | |
| | | 9.2 GHz VCO, 90 MHz offset | | -157 | | |
| | | 10.3 GHz VCO, 10 kHz offset | | -77 | | |
| | | 10.3 GHz VCO, 100 kHz offset | | -104 | | |
| | | 10.3 GHz VCO, 1 MHz offset | | -126 | | |
| | | 10.3 GHz VCO, 10 MHz offset | | -147 | | |
| | | 10.3 GHz VCO, 90 MHz offset | | -157 | | |
| | | 11.3 GHz VCO, 10 kHz offset | | -76 | | |
| | | 11.3 GHz VCO, 100 kHz offset | | -103 | | |
| | | 11.3 GHz VCO, 1 MHz offset | | -125 | | |
| | | 11.3 GHz VCO, 10 MHz offset | | -145 | | |
| | | 11.3 GHz VCO, 90 MHz offset | | -158 | | |
| | | 12.5 GHz VCO, 10 kHz offset | | -74 | | |
| | | 12.5 GHz VCO, 100 kHz offset | | -100 | | |
| | | 12.5 GHz VCO, 1 MHz offset | | -123 | | |
| | | 12.5 GHz VCO, 10 MHz offset | | -144 | | |
| | | 12.5 GHz VCO, 90 MHz offset | | -157 | | |
| | | 13.3 GHz VCO, 10 kHz offset | | -73 | | |
| | | 13.3 GHz VCO, 100 kHz offset | | -100 | | |
| | | 13.3 GHz VCO, 1 MHz offset | | -122 | | |
| 13.3 GHz VCO, 10 MHz offset | | -143 | | | | |
| 13.3 GHz VCO, 90 MHz offset | | -155 | | | | |
| 14.5 GHz VCO, 10 kHz offset | | -73 | | | | |
| 14.5 GHz VCO, 100 kHz offset | | -99 | | | | |
| 14.5 GHz VCO, 1 MHz offset | | -121 | | | | |
| 14.5 GHz VCO, 10 MHz offset | | -143 | | | | |
| 14.5 GHz VCO, 90 MHz offset | | -152 | | | | |
| t _{VCO_CAL} | VCO calibration speed, switch across the entire frequency band, F _{OSC} = 200 MHz, F _{PD} = 100 MHz ⁽⁶⁾ | No assist | | 50 | | μs |
| | | Close frequency | | 20 | | |

(6) See Application and Implementation for more details on the different VCO calibration modes.

Electrical Characteristics (continued)

Measurements are done at 25 degree C. Parameters are measured at IF = 65MHz with high side injection, unless otherwise noted. Measurements are done with external VCM = 1.7V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--------------------------------|-----|------------|------|-------|
| K _{VCO} | VCO gain | 8 GHz | | 89 | | MHz/V |
| | | 9.2 GHz | | 93 | | |
| | | 10.3 GHz | | 110 | | |
| | | 11.3 GHz | | 124 | | |
| | | 12.5 GHz | | 189 | | |
| | | 13.3 GHz | | 182 | | |
| | | 14.5 GHz | | 205 | | |
| ΔT _{CL} | Allowable temperature drift when VCO is not re-calibrated | | | 125 | | °C |
| H2 | VCO second harmonic | FVCO = 8 GHz, divider disabled | | -30 | | dBc |
| H3 | VCO third harmonic | FVCO = 8 GHz, divider disabled | | -40 | | |
| SYNC PIN AND PHASE ALIGNMENT | | | | | | |
| F _{OSCIN_SYNC} | Maximum usable OSCIN frequency with SYNC pin | Category 3 (int LO mode) | 0 | | 100 | MHz |
| | | Category 1 or 2 | 0 | | 1400 | |
| DIGITAL INTERFACE (SCK, SDI, CSB, MUXOUT, SYNC, CE) | | | | | | |
| V _{IH} | High level input voltage | | 1.4 | | VCC | V |
| V _{IL} | Low level input voltage | | 0 | | 0.4 | V |
| I _{IH} | High level input current | | -50 | | 50 | μA |
| I _{IL} | Low level input current | | -50 | | 50 | μA |
| V _{OH} | High level output voltage | I _L = -5 mA | | VCC - 0.55 | | V |
| V _{OL} | High level output current | I _L = 5 mA | | | 0.55 | V |

6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|--|-----|-----|-----|------|
| SYNC | | | | | |
| t _{SETUP} | Setup time for pin relative to OSCIN rising edge | 2.5 | | | ns |
| t _{HOLD} | Hold time for pin relative to OSCIN rising edge | 2 | | | ns |
| DIGITAL WRITE INTERFACE⁽¹⁾ | | | | | |
| F _{SPI_WRITE} | SPI write speed | | | 50 | MHz |
| t _{ES} | Clock to enable low time | 5 | | | ns |
| t _{CS} | Data to clock setup time | 2 | | | ns |
| t _{CH} | Data to clock hold time | 2 | | | ns |
| t _{CWH} | Clock pulse width high | 5 | | | ns |
| t _{CWL} | Clock pulse width low | 10 | | | ns |
| t _{CES} | Enable to clock setup time | 10 | | | ns |
| t _{EWL} | Enable pulse width high | 10 | | | ns |
| DIGITAL READBACK INTERFACE⁽²⁾ | | | | | |
| F _{SPI_READ} | SPI readback speed | | | 50 | MHz |
| t _{ES} | Clock to enable low time | 10 | | | ns |
| t _{CS} | Clock to data wait time | | | 10 | ns |
| t _{CWH} | Clock pulse width high | 10 | | | ns |
| t _{CWL} | Clock pulse width low | 10 | | | ns |
| t _{CES} | Enable to clock setup time | 10 | | | ns |

(1) See Figure 1

(2) See Figure 2

Timing Requirements (continued)

| | | MIN | NOM | MAX | UNIT |
|-----------|-------------------------|-----|-----|-----|------|
| t_{EWH} | Enable pulse width high | 10 | | | ns |

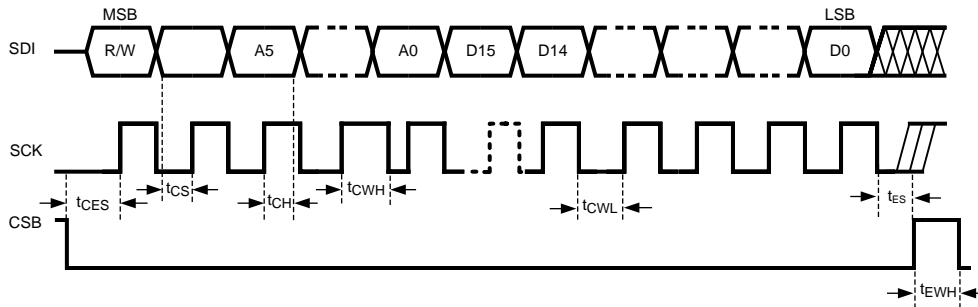


Figure 1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The signal on the SDI pin is clocked into a shift register on each rising edge of the SCK pin.
- The CSB must be held low for data to be clocked. Device ignores clock pulses if CSB is held high.
- The CSB transition from high to low must occur when SCK is low.
- When SCK and SDI lines are shared between devices, TI recommends holding the CSB line high on any devices besides the intended programming target.

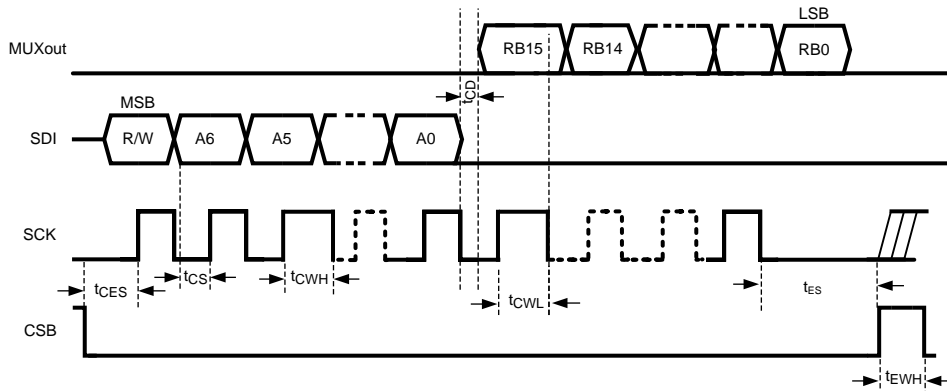


Figure 2. Serial Data Readback Timing Diagram

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXOUT pin is always for the address portion of the transaction.
- The address on the SDI pin is clocked into a shift register on each rising edge of the SCK pin.
- The data portion of the transaction on the SDI line is always ignored.
- The data on the MUXOUT pin should be considered valid on each rising edge of the SCK pin, provided all timing requirements are met.
- All CSB considerations for SPI writing also apply to SPI readback.

6.7 Typical Characteristics

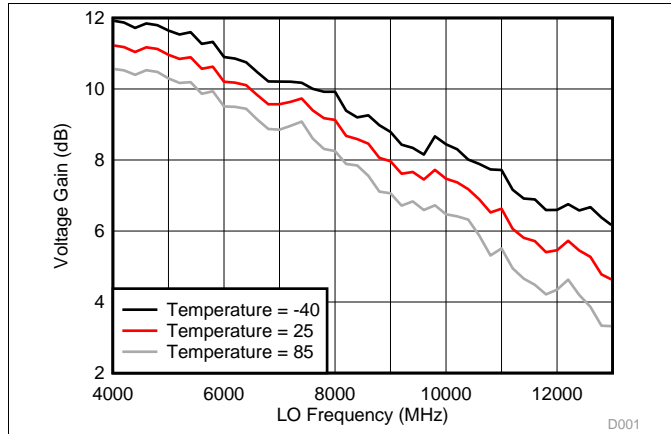


Figure 3. Voltage Gain Across LO Frequency for Internal LO Mode

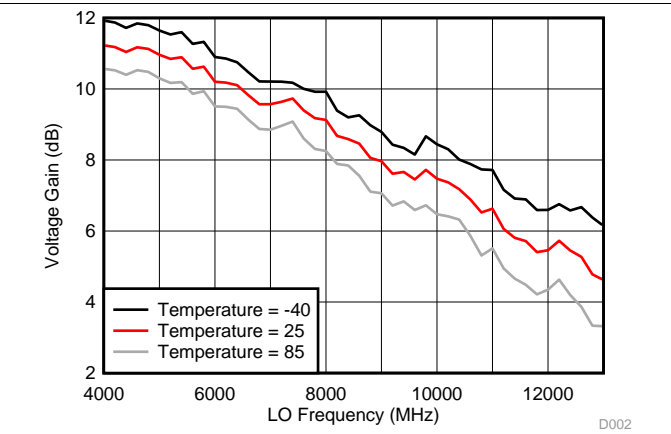


Figure 4. Voltage Gain Across LO frequency for External LO Mode

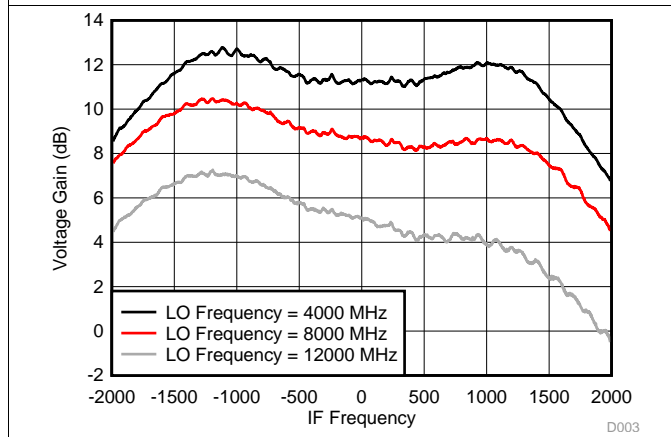


Figure 5. Voltage Gain Across IF Frequency for Internal LO Mode

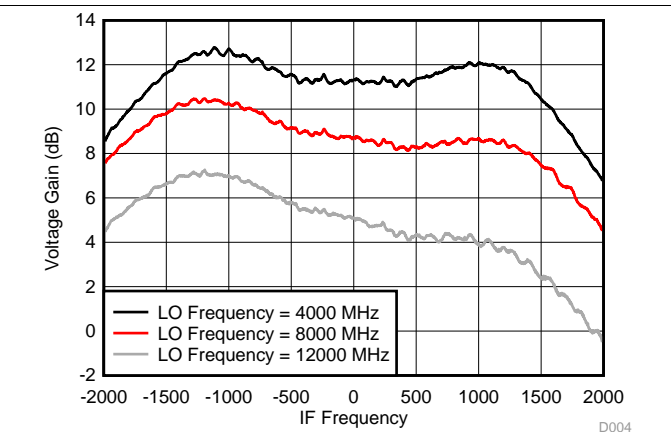


Figure 6. Voltage Gain Across IF Frequency for External LO Mode

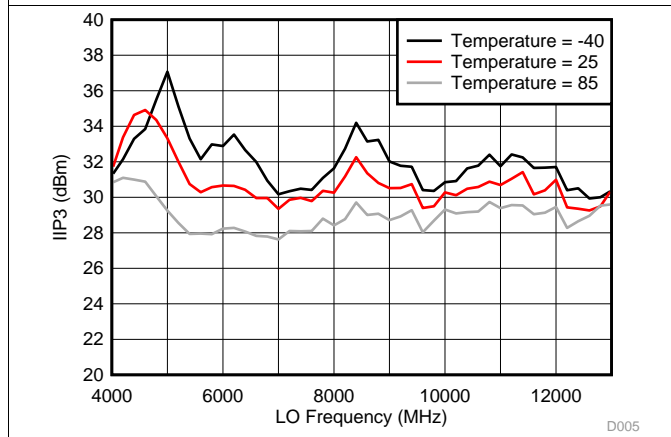


Figure 7. IIP3 Across LO Frequency for Internal LO Mode

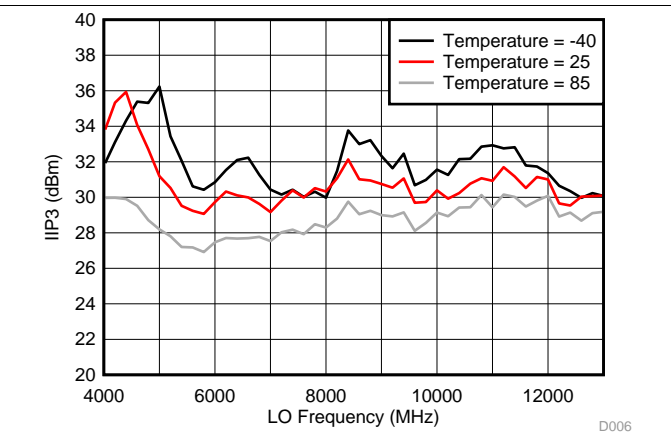


Figure 8. IIP3 Across LO Frequency for External LO Mode

Typical Characteristics (continued)

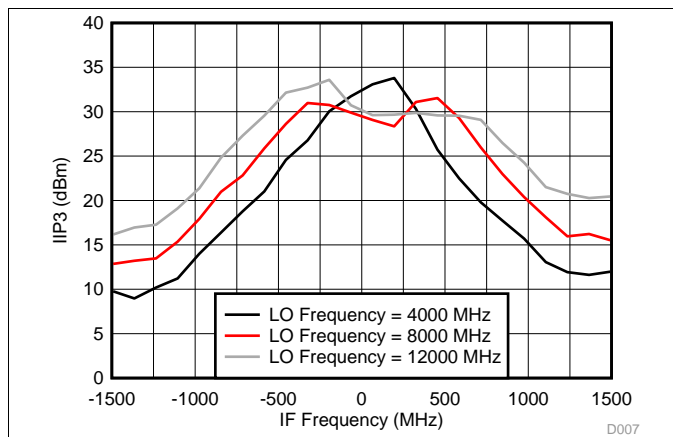


Figure 9. IIP3 Across IF Frequency for Internal LO Mode

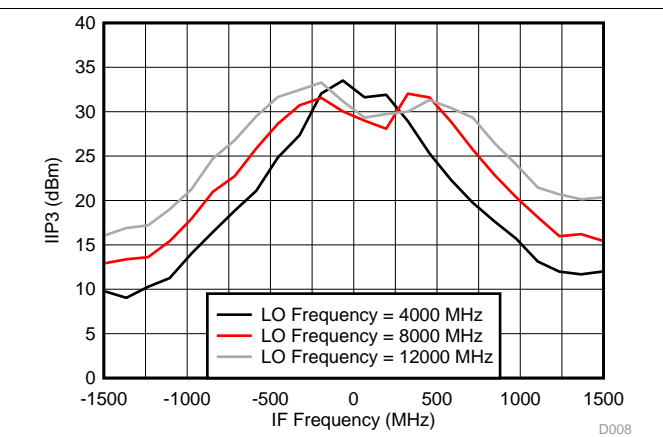


Figure 10. IIP3 Across IF Frequency for External LO Mode

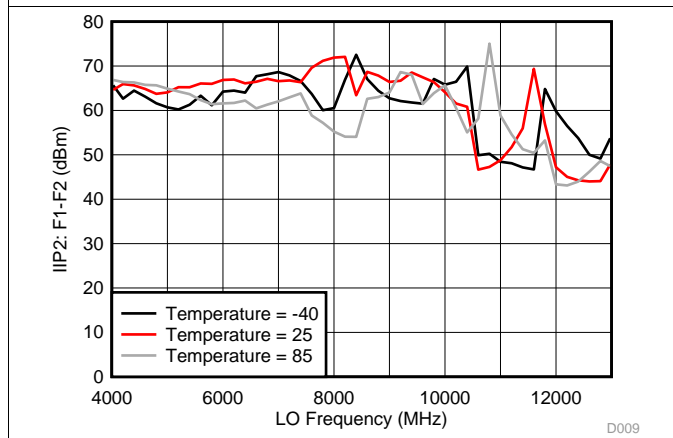


Figure 11. IIP2: F1-F2 Across LO Frequency for Internal LO Mode

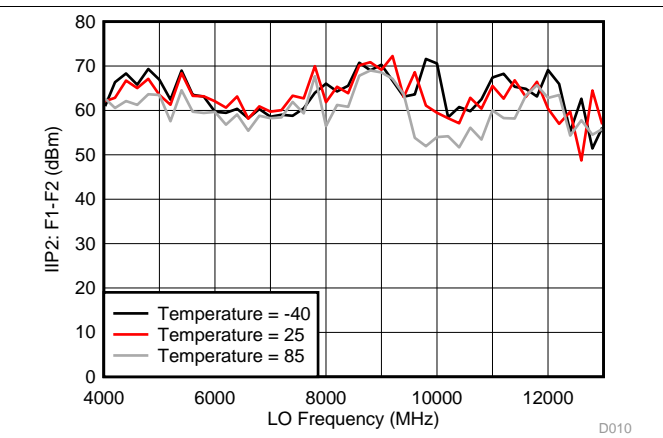


Figure 12. IIP2: F1-F2 Across LO Frequency for External LO Mode

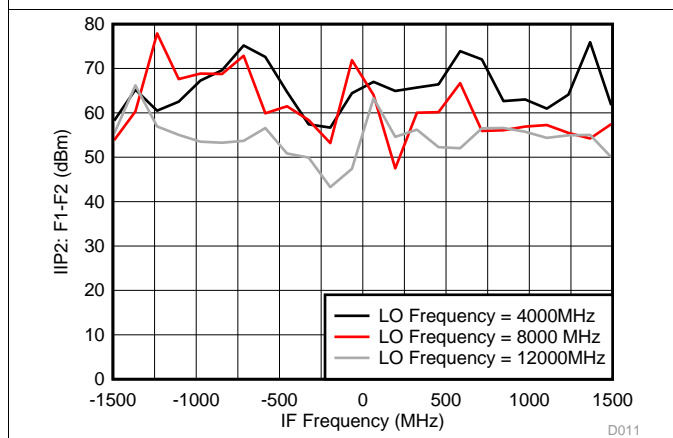


Figure 13. IIP2: F1-F2 Across IF Frequency for Internal LO Mode

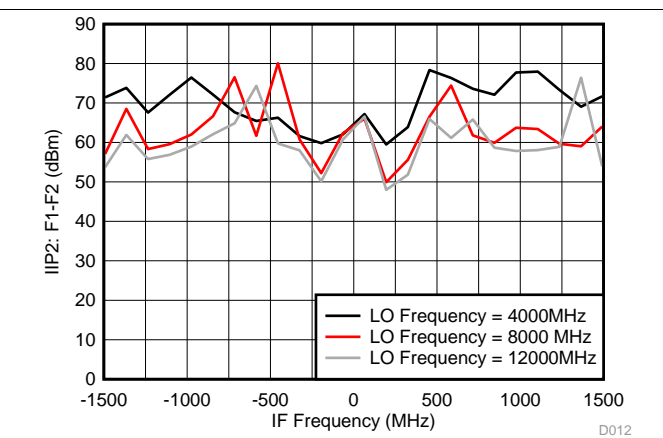


Figure 14. IIP2: F1-F2 Across IF Frequency for External LO Mode

Typical Characteristics (continued)

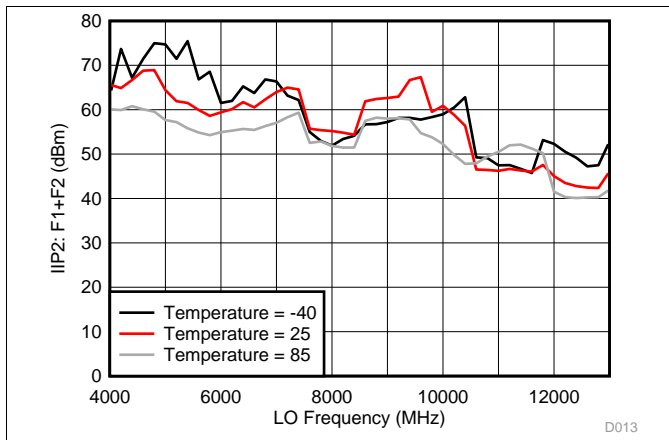


Figure 15. IIP2: F1+F2 Across LO Frequency for Internal LO Mode

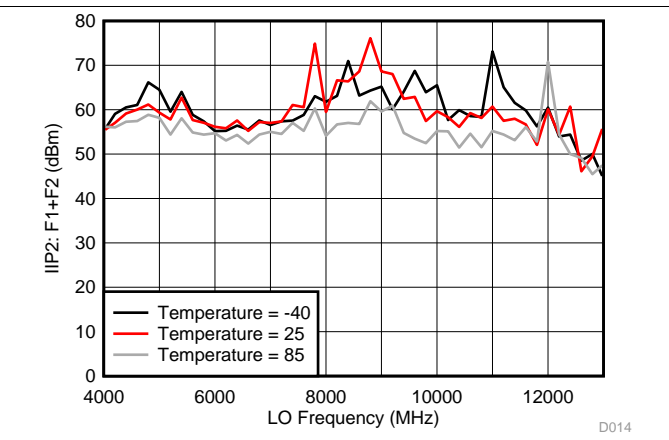


Figure 16. IIP2: F1+F2 Across LO Frequency for External LO Mode

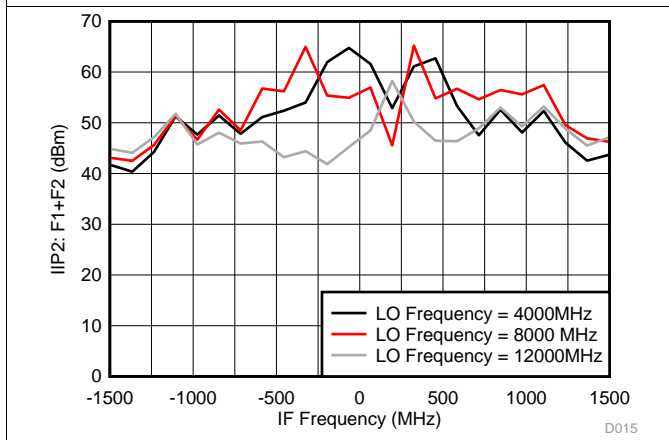


Figure 17. IIP2: F1+F2 Across IF Frequency for Internal LO Mode

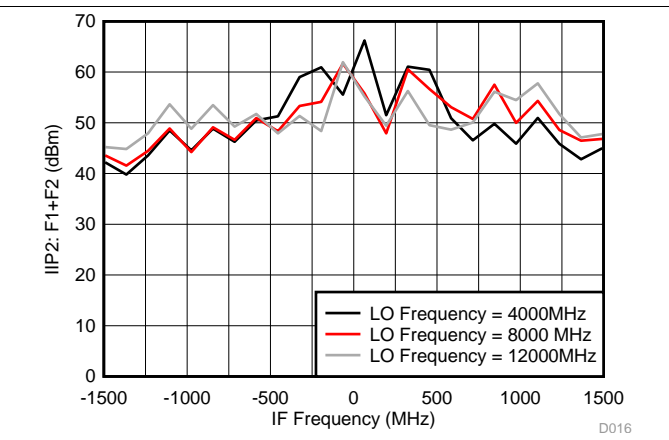


Figure 18. IIP2: F1+F2 Across IF Frequency for External LO Mode

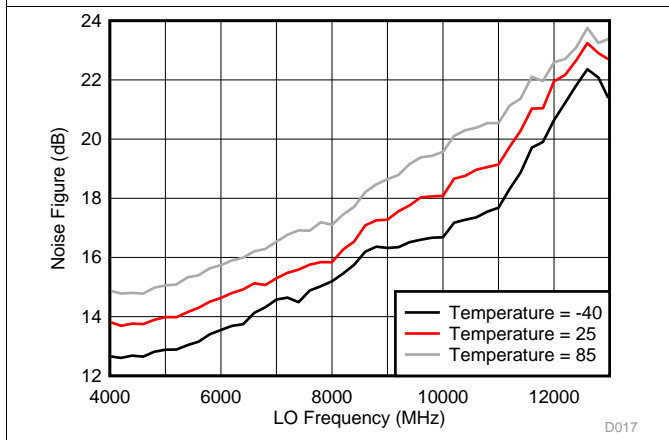


Figure 19. Noise Figure Across LO Frequency for Internal LO Mode

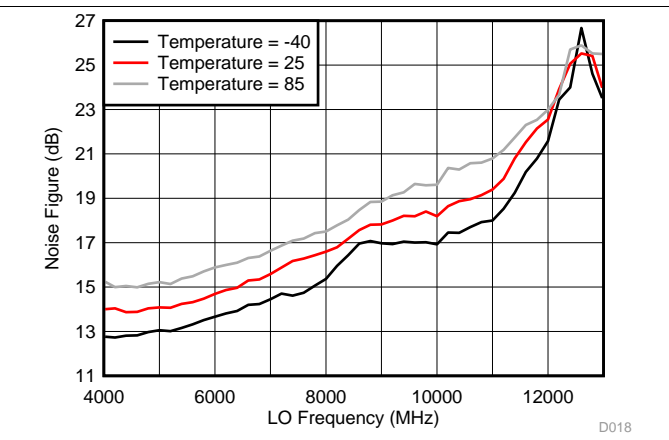


Figure 20. Noise Figure Across LO Frequency for External LO Mode

Typical Characteristics (continued)

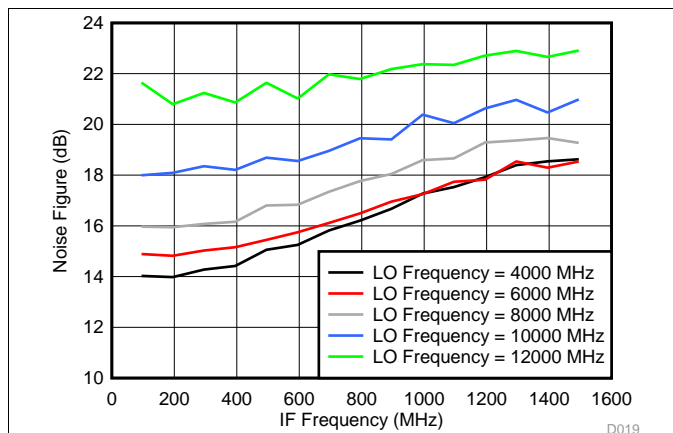


Figure 21. Noise Figure Across IF Frequency for Internal LO Mode

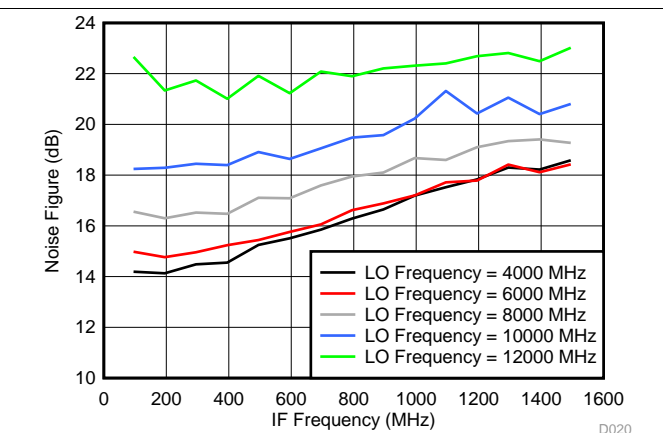


Figure 22. Noise Figure Across IF Frequency for External LO Mode

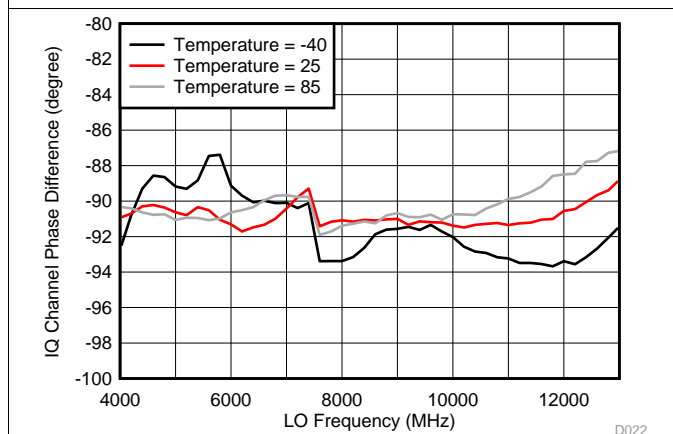


Figure 23. Uncalibrated IQ Phase Difference for Internal LO Mode

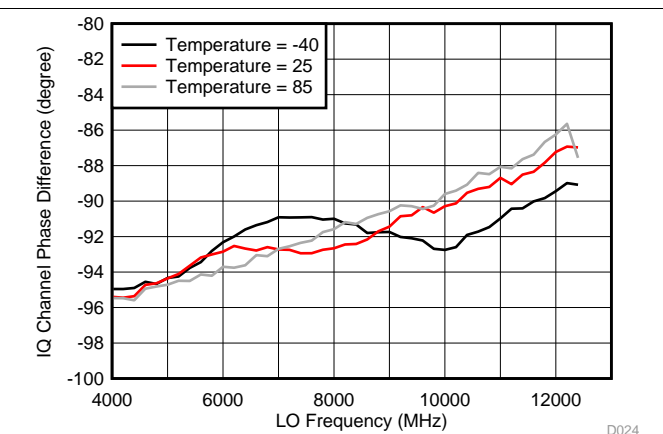


Figure 24. Uncalibrated IQ Phase Difference for External LO Mode

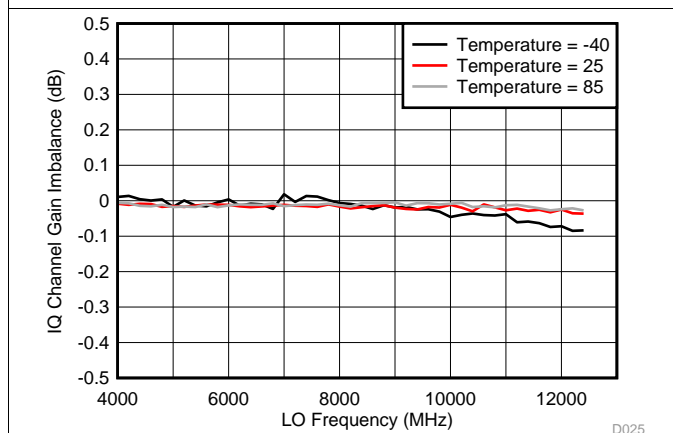


Figure 25. Uncalibrated IQ Gain Imbalance for Internal LO Mode

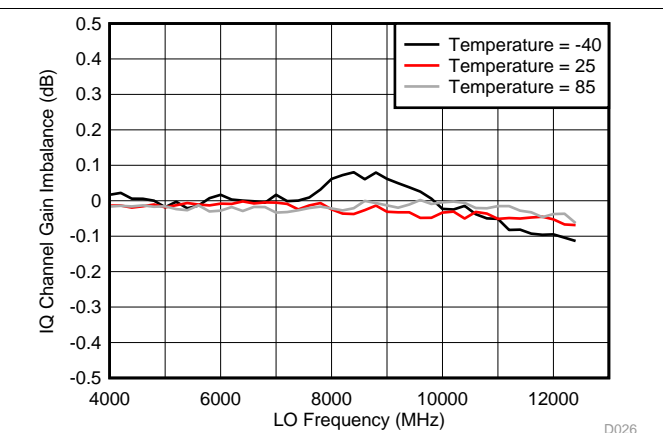
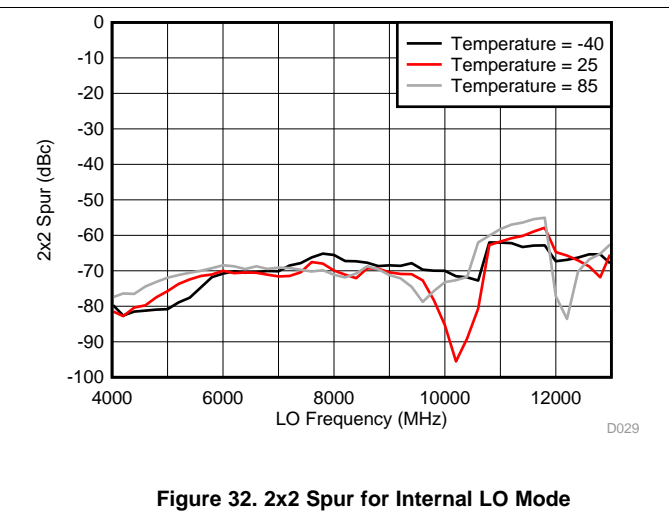
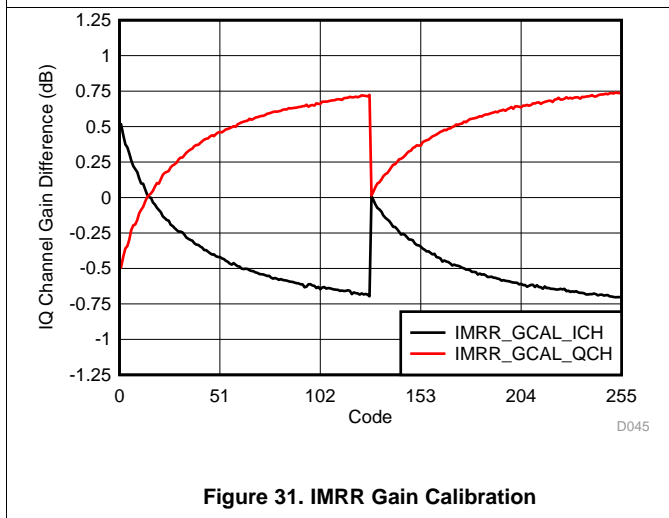
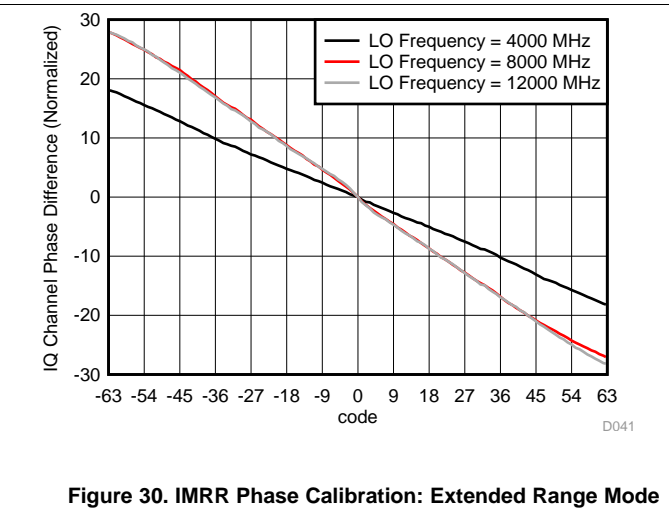
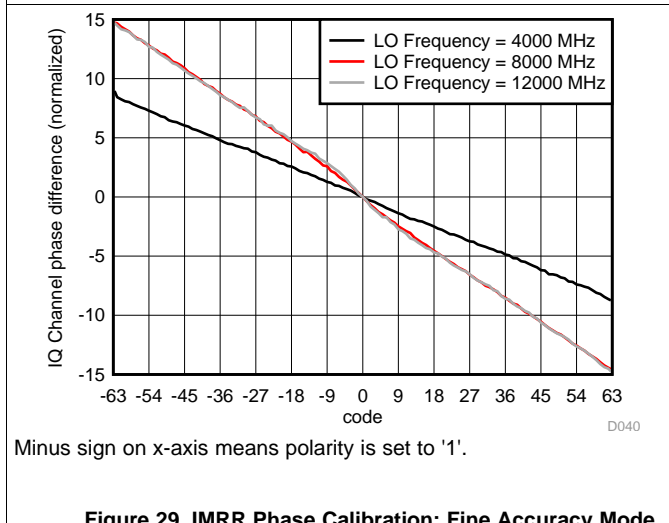
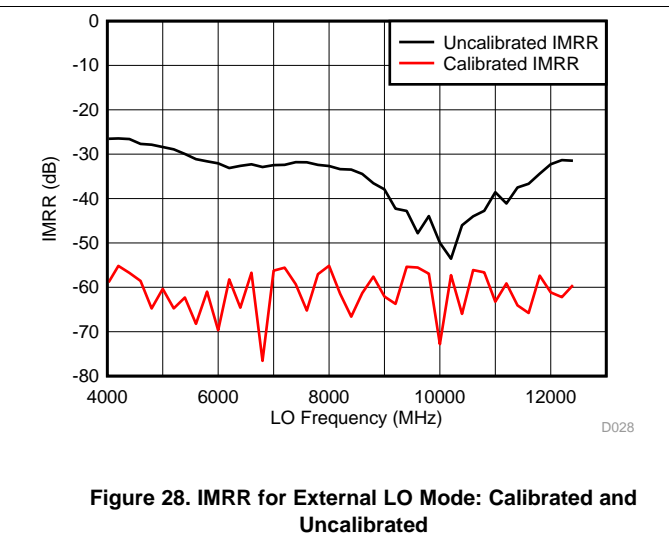
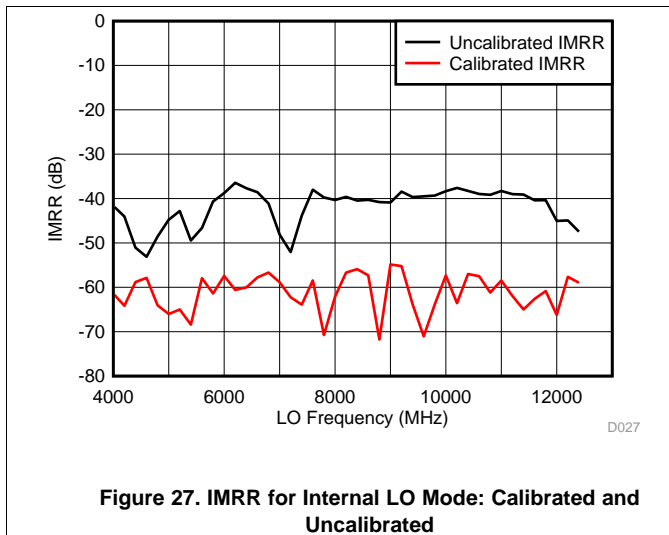


Figure 26. Uncalibrated IQ Gain Imbalance for External LO Mode

Typical Characteristics (continued)



Typical Characteristics (continued)

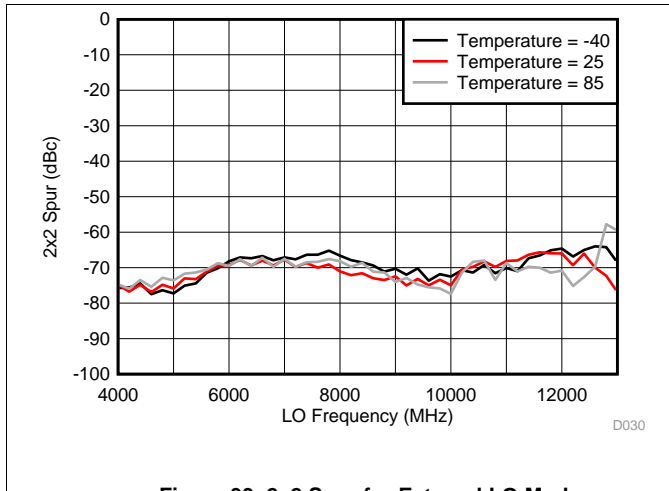


Figure 33. 2x2 Spur for External LO Mode

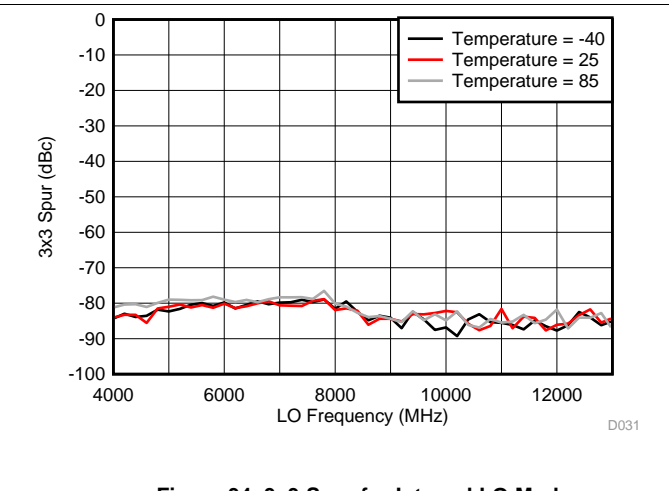


Figure 34. 3x3 Spur for Internal LO Mode

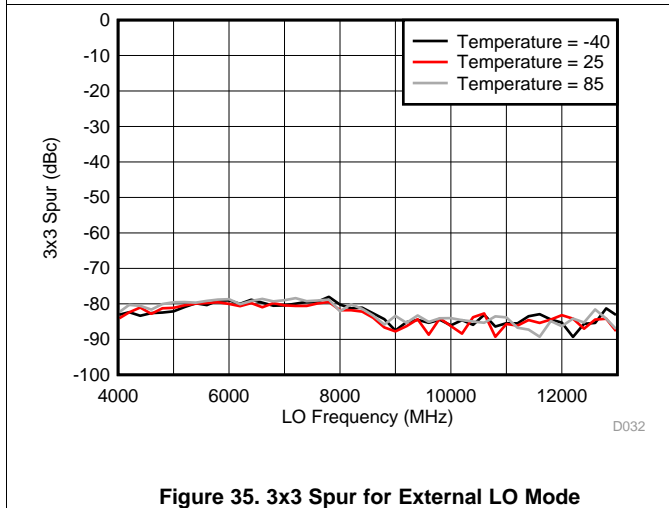


Figure 35. 3x3 Spur for External LO Mode

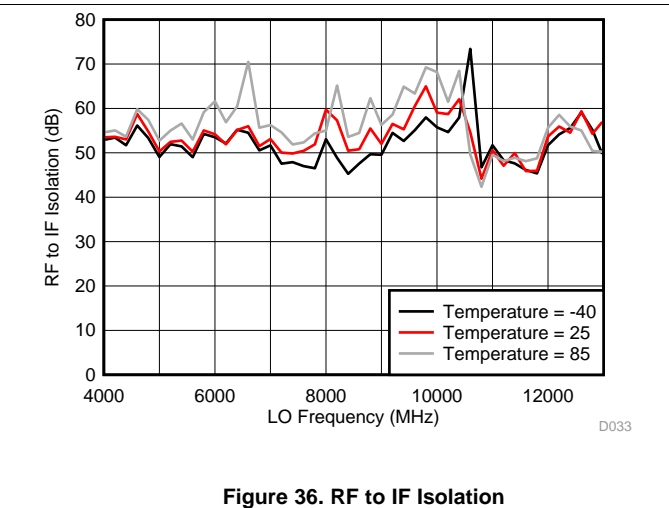


Figure 36. RF to IF Isolation

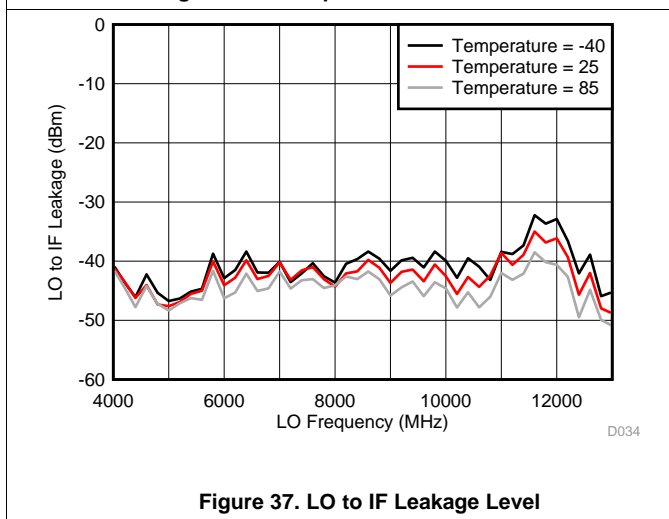


Figure 37. LO to IF Leakage Level

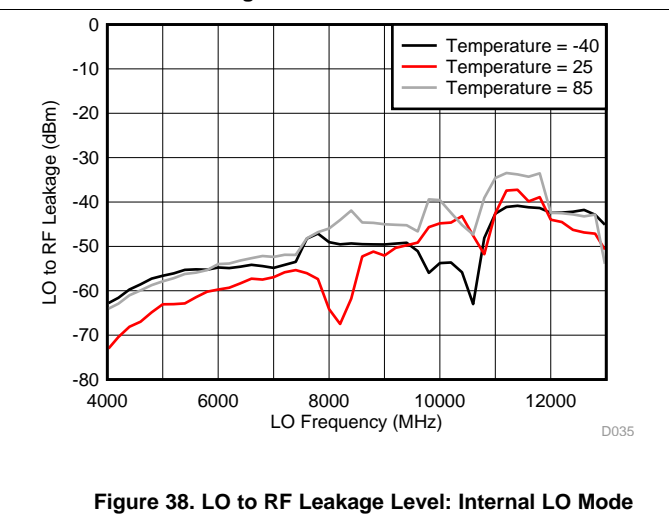


Figure 38. LO to RF Leakage Level: Internal LO Mode

Typical Characteristics (continued)

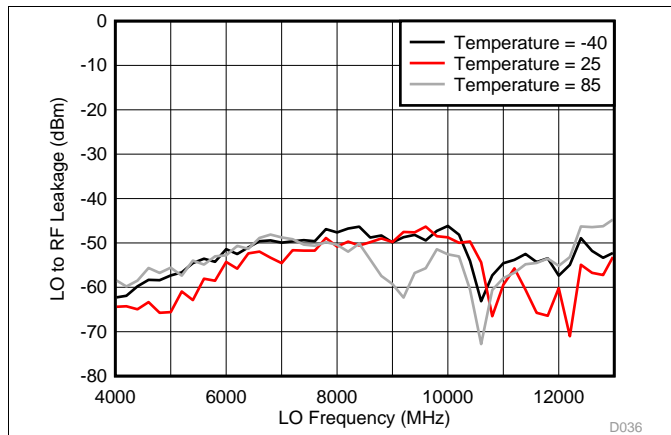
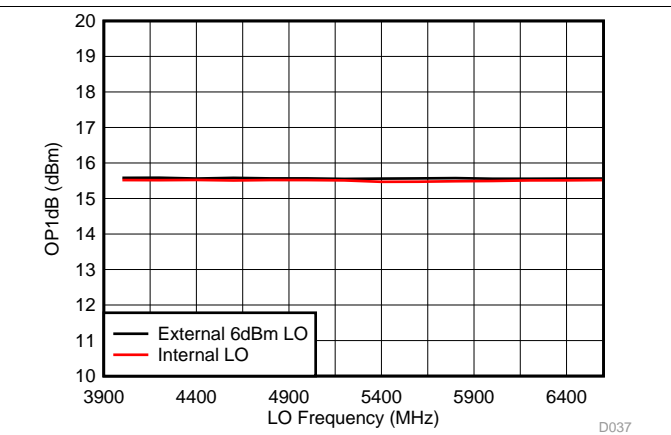
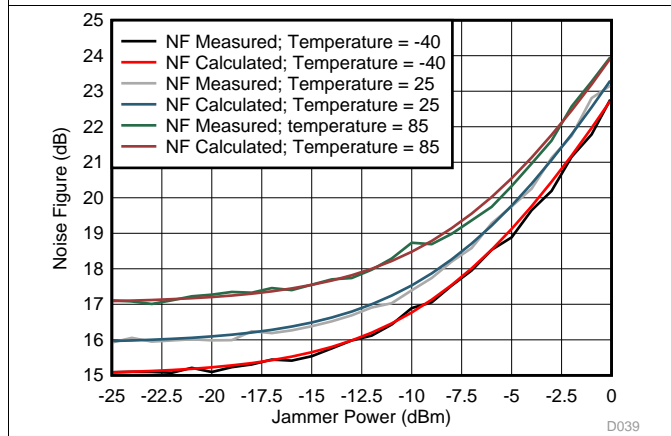


Figure 39. LO to RF Leakage Level: External LO Mode



1. The LO frequency is capped at 6600MHz because IP1dB exceeds +10dBm when LO frequency goes beyond 6600MHz; The device can be damaged when input power is more than +10dBm.

Figure 40. OP1dB Across LO Frequency



1. Jammer frequency = 8.8GHz, LO = 7.8GHz, IF = 100MHz.
2. Internal LO phase noise values used for calculation at -40, 25, and 85 degrees C are -155, -154.5 and -154 dBc/Hz, separately.

Figure 41. Noise Figure with Jammer

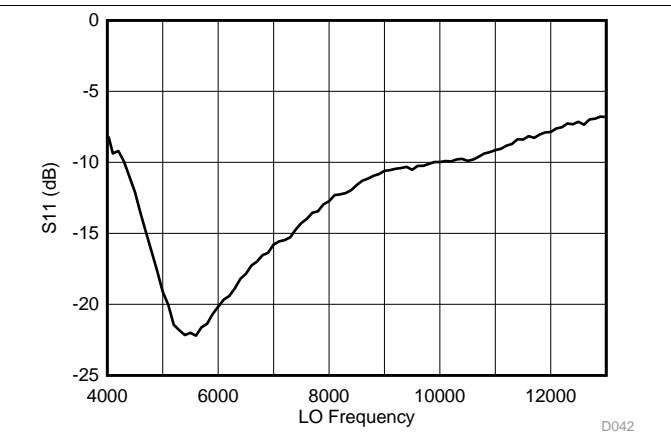
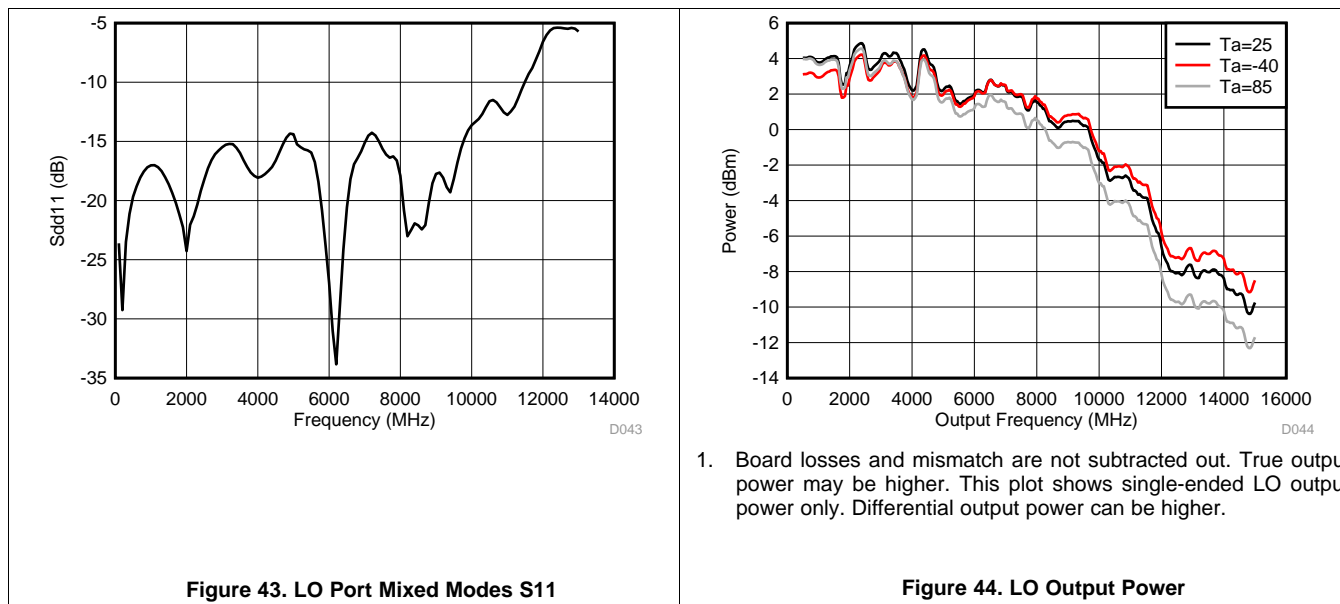


Figure 42. RF Port S11

Typical Characteristics (continued)



1. Board losses and mismatch are not subtracted out. True output power may be higher. This plot shows single-ended LO output power only. Differential output power can be higher.

Measurements are done at 25 degree C unless temperature is specified in the plots.

For measurements across LO frequency, IF = 65MHz, and LO injection type is high side injection. For measurements across IF frequency, high side injection is applied

For all measurements that require RF input, RF input power = -10 dBm unless otherwise specified.

For two-tone measurements, the separation between two tones is 17MHz.

For all measurements, internal 1.7V VCM is applied.

For all external LO mode measurements, LO power = +6 dBm.

IF baluns used for measurements are: ADT2-18+ from Mini-Circuits™.

LO balun used for measurements is: BIB-100G from PPM-Test™.

RF combiner used for measurements of IP2, IP3 and NF with jammer is: 4426-2 from Narda-MITEQ™.

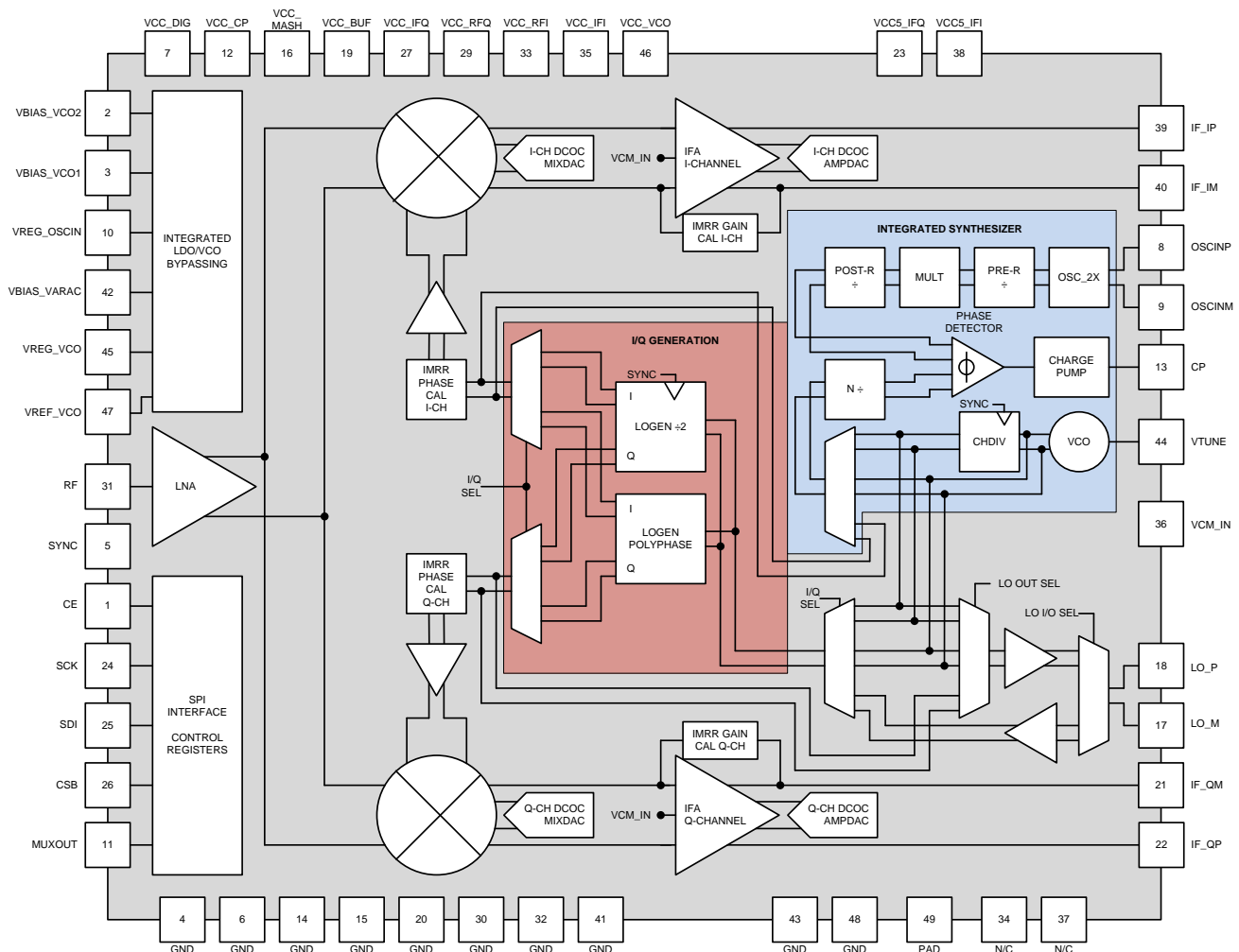
All path losses are calibrated out.

7 Detailed Description

7.1 Overview

The LMX8410L is a high-performance I/Q demodulator with an RF input range of 4 to 10 GHz and an IF output range of DC to 1350 MHz. This device integrates many components to allow high system performance as well as simplified design. There is an integrated synthesizer that generates wide-band frequencies at very low phase noise, with signal carefully conditioned for driving the mixer LO port. The RF input is single ended, enabled by an integrated wide-band RF balun at the front end. The two mixers on each I/Q channel are highly linear with optimized filtering and interfacing with components on each port. The IF amplifier is a high gain and high linearity component, saving users from matching discrete amplifiers and being restricted by common mode voltages typically encountered when interfacing mixers and ADC's. In addition to high linearity and low noise performance, the LMX8410L comes equipped with many features to further optimize certain parameters. The automatic DC offset calibration is run by an internal automatic algorithm which will sense and tune the DC offset between the N and P sides of the differential signal of each IF amplifier, thus ensuring optimal performance when directly DC coupled to the ADC. The I/Q calibration knob allows tuning blocks within the mixer and IF amplifier to balance both the gain and the phase of the I/Q output signals, thus giving the user capability to adjust and achieve high image rejection. The internal synthesizer also has a feature of synchronization, which allows multiple LMX8410L designed in parallel to have synchronized LO signal phase.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Configurations and Feature Description

7.3.1.1 RF, LO and IF Interfaces

7.3.1.1.1 RF Interface

LMX8410 RF input stage provides a wideband input matching in complete RF frequency range. The RF interface requires an external DC block capacitor.

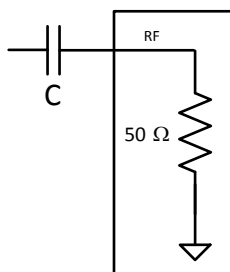


Figure 45. RF Interface

7.3.1.1.2 LO Interface

LO interface for LMX8410 serves dual functionality:

1. Drive the VCO or channel divider output to pin LO_M and LO_P.
2. Inject external LO signal in external LO mode where on-chip synthesizer needs to be bypassed.

7.3.1.1.2.1 LO Interface as Output Port

When LO interface operates as output port, it drives either VCO or Channel Divider output to the port. The device provides open collector output. Therefore, a pair of off-chip load resistors or inductors are needed in order to have LO output power.

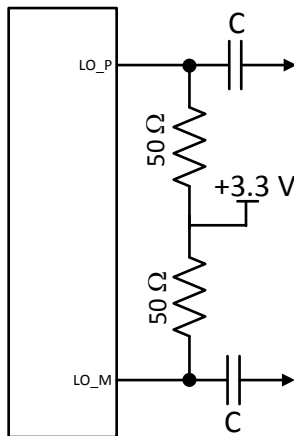


Figure 46. LO Port Operating In Output Mode Requires Load Resistors Or Inductors

7.3.1.1.2.2 LO Interface as Input Port

When LO interface operates as input port, the pull-up resistors or inductors must be removed. Device pins must be AC coupled with DC block. LO pins offer wideband differential 100 Ohm termination to enable port matching. The value of termination can be set to 100Ohm, 200Ohm or high impedance through register EXTLO_INT_MATCH_RES (R123<1:0>). It is recommended to keep the termination setting to 100 ohm during external LO injection and to high impedance mode while LO is brought out from the device.

Feature Description (continued)

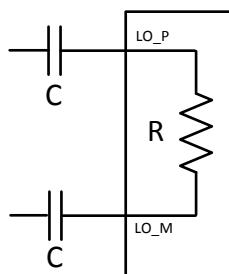


Figure 47. LO Port Operating In Input Mode

7.3.1.1.3 Baseband Interface

LMX8410 has a low impedance output driver capable of driving the resistive as well as capacitive loads. Therefore, a pair of 50 ohm off-chip resistors can be placed in both IF_P and IF_M paths to provide 100Ohm differential matching if IF port matching is required.

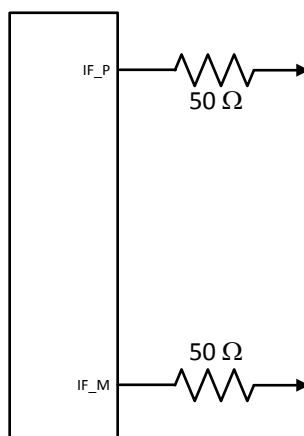


Figure 48. IF Interface Requires External Resistors for 100Ohm Differential Matching

7.3.1.2 Device Configurations Overview

Follow below steps to configure the device successfully.

7.3.1.2.1 Initialize the Device

After the device is powered on, follow below setups in sequence.

1. Set R127 = 0x0003
2. Set R6 = 0x0100
3. Set R127 = 0x0000
4. Load device configuration bits.

7.3.1.2.2 Configure LO Modes

Refer to [Table 5](#) to set up correct LO modes. After LO mode is configured, In case of internal LO mode, lock the integrated synthesizer and jump to [Perform DCOC \(DC Offset Correction\)](#). In case of external LO mode, go to [Set Up External LO Clock](#).

Feature Description (continued)

7.3.1.2.3 Set Up External LO Clock

Follow below steps to set up external LO clock:

1. Set external LO divider. Refer to [State Machine Clock](#)
2. Provide external LO signal on the pin.
3. Enable the divider by setting EXTLO_CLK_DIV_EN (R81<7:6>) to 3. This step should be done only after valid external LO signal is driven on the pin.
4. Select SM clock source towards external LO driven SM clock by setting SM_CLK_SEL (R81<0>) = 1.
5. Wait for 100 usec before performing DCOC.

7.3.1.2.4 Perform DCOC (DC Offset Correction)

Perform DCOC for both I and Q channels. Refer to [DCOC \(DC Offset Correction\)](#) for detailed instructions.

7.3.1.2.5 Turn Off SM Clock

Turn off SM clock after DCOC to remove coupling spurs from clock signals.

1. In internal LO mode, set SM_CLK_EN (R2<10>) to 0.
2. In external LO mode, set EXTLO_CLK_DIV_EN (R81<7:6>) to 0.

7.3.1.2.6 Perform IMRR (Image Rejection Ratio) Calibration

Refer to [Image Rejection Calibration](#) for detailed instructions.

7.3.1.3 State Machine Clock

The State machine clock can be derived, through a MUX, from division of OSCin frequency in internal LO mode or from division of external LO frequency in external LO mode. The upper bound for State machine clock is 200MHz while lower bound is 1MHz/10MHz in internal/external LO modes. In external LO mode, two sets of dividers need to be programmed to set the right SM clock frequency. DIV_A is an 8-state divider which drives DIV_B. Input frequency to DIV_B must be kept less than 1.4GHz. Recommended SM_CLK frequency is 100MHz.

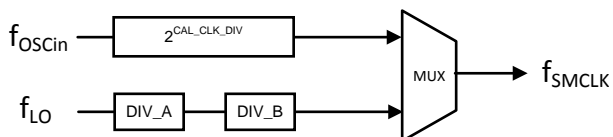


Figure 49. Block Diagram of SM Clock

7.3.1.3.1 Set Divider Values For Internal LO Mode

The value of divider in internal LO mode is $2^{(value\ of\ CAL_CLK_DIV)}$.

Feature Description (continued)

7.3.1.3.2 Set Divider Values For External LO Mode

The divider for external LO mode is EXTLO_DIV (R82<5:0>), where R82<5:3> sets DIV_A and R82<2:0> sets DIV_B. The value of DIV_A should be set according to [Table 1](#). The value of DIV_B is 2^(value of R82<2:0>).

Table 1. DIV_A Encoding

| EXTLO_DIV (R82<5:3>) | Division Value |
|----------------------|----------------|
| 000 | /1 |
| 001 | /2 |
| 010 | /16 |
| 011 | /4 |
| 100 | /16 |
| 101 | /16 |
| 110 | /16 |
| 111 | /8 |

7.3.1.4 DCOC (DC Offset Correction)

The DC offset of IF output can be automatically corrected by checking EN_DCOC_ICH_LUT and EN_DCOC_QCH_LUT

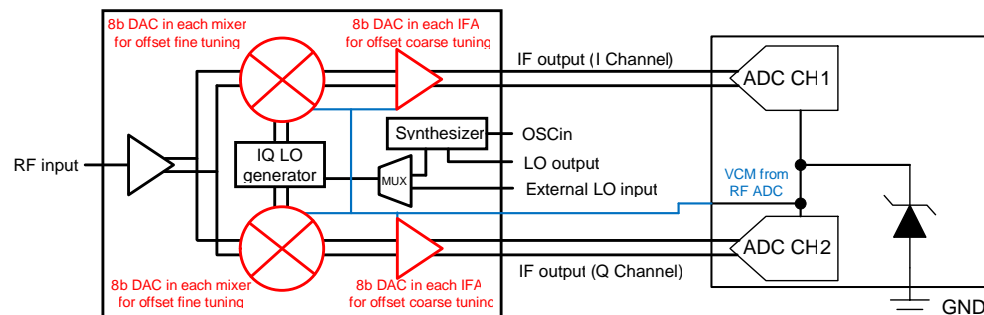


Figure 50. DC Offset Correction Diagram

7.3.1.4.1 RF Input Power Restriction During DCOC

For best accuracy, power at the RF input of the LMX8410 should be kept below -50dBm during DCOC calibration. Additional isolation (~15dB) can be obtained by turning of LNA_PD and LNA_BIAS_OFF.

7.3.1.4.2 Set Up DCOC Clock Divider

DCOC state machine clock can operate from 0.5MHz to 2MHz, preferably set to 1MHz. Calculation of clock frequency: DCOC clock Frequency = (SM_CLK frequency)/(2*DCOC_CLK_DIV value). Refer to [State Machine Clock](#) for SM_CLK setup. It is recommended to set and reset DCOC_FSM_RESET (R126<8>) every time the LO frequency is changed.

7.3.1.5 Image Rejection Calibration

LMX8410 provides registers to vary the gain and phase of the I and Q channel individually to improve image rejection.

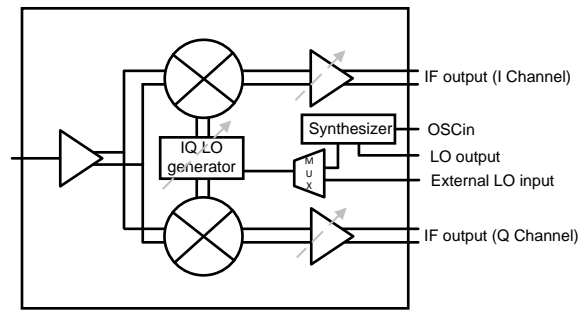


Figure 51. Image Reject Calibration Example

7.3.1.5.1 Phase Calibration

Phase magnitude can be tuned using IMRR_PHCAL (R95<14:9>), polarity of phase calibration can be set by IMRR_PHCAL_POL (R95<15>). If Q channel leads I by > 90 deg. Set polarity to '0', otherwise set it to '1'. Typical step size of magnitude tuning is 0.2 deg for fine accuracy mode and 0.45 deg for extended range mode. The fine accuracy mode and extended range mode can be set by IMRR_PHCAL_EXTEND (R126<15>). Refer to [Figure 29](#) and [Figure 30](#) for details of the two modes.

7.3.1.5.2 Gain Calibration

The voltage magnitude of I and Q channel can be tuned by IMRR_GCAL_ICH (R94<7:0>) and IMRR_GCAL_QCH (R94<15:8>). The recommended code range is 128 to 255. In this code range, gain tuning range is 0.5dB. Extended code range is 0 to 127. In this range, step size is higher and gain tuning range is 1dB. Refer to [Figure 31](#) for details of the two code ranges. Re-calibration may be needed with temperature drift.

7.3.1.6 IF Amplifier Common Mode Configurations

IF amplifier common mode voltage can be set by VCM_CONFIG (R83<12:9>). Additional setups are needed depending on VCM magnitude. Refer to [Table 2](#) for more details. For best common mode voltage accuracy, supply external VCM and choose "External" in VCM_CONFIG.

Table 2. IF Amplifier Common Mode Configurations

| IFA common mode(V) | IFA_PULLUP_EN (R79<6>) | IFA_PULLUP (R83<15:13>) | IFA_CONFIG (R88<1:0>) |
|--------------------|------------------------|-------------------------|-----------------------|
| 1.2 | 1 | 7 | 0 |
| 1.3 | 1 | 3 | 0 |
| 1.4 | 1 | 1 | 0 |
| 1.5 | 0 | 0 | 0 |
| >= 1.6 | 0 | 0 | 3 |

7.3.1.7 Synchronization Mode (Internal LO Mode Only)

7.3.1.7.1 Synchronization of the LO_OUT Output to the Fosc Input

The LO_OUT pin can be synchronized to the Fosc input in exactly the same way that the LMX2594 can. For cases where the output frequency is not a multiple of the input frequency, the SYNC pin can be used.

7.3.1.7.2 Synchronization of I/Q Outputs to Fosc Inputs Using Internal LO

When the internal LO is used, IF outputs of two devices can be synchronized to the Fosc input if and only if the VCO frequency is a multiple of the Fosc frequency and there is no multiplication in the input path (OSC_2X = 0 and MULT=1). The device is inherently in SYNC all the time in this condition so therefore there is no need to use the SYNC pin or to toggle the SYNC_PHASE_PLL bit.

7.4 Device Functional Modes

The LMX8410L can be programmed for two functional modes: internal LO mode (using the integrated synthesizer) or external LO mode (bypassing the integrated synthesizer). In internal LO mode, when 4GHz <= LO frequency <=7.5 GHz, use divide-by-2 (Div 2) mode; when 7.5 GHz <= LO frequency <= 10 GHz, use polyphase filter mode (Poly). Refer to [Table 3](#) to set up registers correctly. Under special circumstances where integrated synthesizer fails to lock at 7.5 ~ 7.7GHz, refer to [VCO Range Uncertainty for 7.5 to 7.7 GHz](#) for more instructions.

Table 3. Internal LO Mode and External LO Mode Register Configurations

| FIELD NAME | ADDRESS | INTERNAL LO/DIV2 | INTERNAL LO/Poly | EXTERNAL LO |
|---------------------|-------------|------------------|------------------|-------------|
| PLL_PD | R0[0] | 0 | 0 | 1 |
| LO_OUT_PD | R44[7] | 1 | 1 | 1 |
| SIGCHAIN_PD | R79[0] | 0 | 0 | 0 |
| LO_PATH_EN | R79[14:12] | 0 | 7 | 7 |
| LO_MUX | R80[5:0] | 9 | 10 | 34 |
| SM_CLK_SEL | R81[0] | 0 | 0 | 1 |
| EXTLO_CLK_DRV_EN | R81[2:1] | 0 | 0 | 3 |
| LO_DRVR_MODE | R81[5:4] | 1 | 0 | 3 |
| EXTLO_CLK_DIV_EN | R81[7:6] | 0 | 0 | 3 |
| LO_POLY_MODE1 | R81[11:8] | 3 | 0 | 15 |
| LO_POLY_MODE2 | R103[13:10] | 11 | 0 | 0 |
| EXTLO_INT_MATCH_RES | R123[1:0] | 0 | 0 | 3 |

7.4.1 Internal LO Mode

When using internal LO mode, the integrated synthesizer is activated to generate the desired LO frequency. The OSCINP and OSCINM pins are used to provide a reference frequency to the PLL and are required to generate the internal state machine clock. The CP pin generates the phase detector output for use with an external loop filter. The filtered phase detector output is fed into the VTUNE pin to control the internal VCO, generating frequencies between 7.5 GHz and 15 GHz. The VCO output is divided down to close the loop into the phase detector. The VCO output may be fed directly into the I/Q generation circuitry.

The I/Q generation circuitry has two paths: a divide-by-2 path, and a polyphase filter path. Depending on the frequency of the LO, the I/Q generation circuitry used will differ. The divide-by-2 path requires the VCO frequency to be double that of the LO frequency. When the LO frequency is between 4 GHz and 7.5 GHz, the VCO can be programmed to between 8 GHz and 15 GHz, and the VCO output can be fed into the divide-by-2 path. When the LO frequency is greater than 7.5 GHz, the VCO can be programmed to between 7.5 GHz and 15 GHz, and the VCO output can be fed into the polyphase filter path.

In Internal LO mode, the LO pins may be used as outputs (refer to [LO Interface as Output Port](#)) for three separate signals internal to the device:

1. The VCO output may be fed directly to the LO pins.
2. The VCO may be divided by any possible combination using the channel divider, and the divided output may be fed to the LO pins. Refer to the datasheet of LMX2594 for more details.

7.4.1.1 VCO Range Uncertainty for 7.5 to 7.7 GHz

Although the majority of devices have a VCO range of 7.5 to 15 GHz, this is NOT ensured. In reality, the VCO is tested for sure to cover 7.7 to 15 GHz. In the range of 7.5 to 7.7 GHz and 15 to 15.4 GHz, the VCO will cover at least enough frequency to cover a factor of two in frequency. What this means if using the internal mixer is that if one wants a LO frequency of 7.6 GHz, then first try this using the poly mode and VCO frequency of 7.6 GHz. However, if the VCO can not do 7.6 GHz, then one has to try DIV2 Mode with the VCO at 15.2 GHz.

Table 4. VCO Ensured Frequency

| Parameter | Symbol | Ensured Condition |
|-----------------------|--------------|---|
| Minimum VCO Frequency | f_{VCOMin} | $f_{VCOMin} \leq 7.7 \text{ GHz}$ |
| Maximum VCO Frequency | f_{VCOMax} | $f_{VCOMax} \geq \text{Max}\{ 15 \text{ GHz}, 2 \times f_{VCOMin} \}$ |

7.4.2 External LO Mode

When using External LO mode, the integrated synthesizer may be powered down and bypassed. The internal state machine clock is derived by dividing down the LO input. Since the frequency range of the LO circuit is bounded below the operational frequency of the divide-by-2 path, I/Q generation must be done using the polyphase filter path.

In External LO mode, some pins must be configured differently than in Internal LO mode. Even when the synthesizer circuitry is bypassed, VCC should be applied to all power pins (though bypass capacitors are no longer required). [Table 5](#) contains a summary of the External LO requirements.

Table 5. External LO Pin Configuration

| PIN NO. | NAME | I/O | EXTERNAL LO REQUIREMENTS |
|---------|-------------|--------|--|
| 2 | VBIAS_VCO2 | Bypass | Floating (no connection) or same configuration with internal LO mode |
| 3 | VBIAS_VCO1 | Bypass | Floating (no connection) or same configuration with internal LO mode |
| 5 | SYNC | Input | Grounded |
| 8 | OSCINP | input | Grounded |
| 9 | OSCINM | input | Grounded |
| 10 | VREG_OSCIN | Bypass | Floating (no connection) or same configuration with internal LO mode |
| 13 | CP | Output | Floating (no connection) or same configuration with internal LO mode |
| 17 | LO_M | Input | Matching network recommended. No pull-up resistors / inductors. ⁽¹⁾ |
| 18 | LO_P | Input | Matching network recommended. No pull-up resistors / inductors. ⁽¹⁾ |
| 42 | VBIAS_VARAC | Bypass | Floating (no connection) or same configuration with internal LO mode |
| 44 | VTUNE | Input | Grounded |
| 47 | VREF_VCO | Bypass | Floating (no connection) or same configuration with internal LO mode |

(1) Refer to [LO Interface as Input Port](#) for LO interfacing.

7.5 Programming

7.5.1 General Comments Regarding Programming

This device is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes

Programming (continued)

7.5.2 Recommended Initial Power Up Sequence

For the most reliable programming, TI recommends this procedure: 1. 2. Program RESET = 1 to reset registers. 3. Program RESET = 0 to remove reset. 4. Program registers as shown in the register map in REVERSE order from highest to lowest. 5. Program register R0 one additional time with FCAL_EN = 1 to ensure that the VCO calibration runs from a stable state.

1. Apply power to device.
2. Program Register R127 to value 0x7F0003
3. Program Register R6 to value 0x060100
4. Program registers R127 to R0 in REVERSE Order
5. If using internal LO, wait 10 ms and then Program register R0 again

7.5.3 Recommended and Power on Reset Bit Values

There are a few points of clarification for power on reset values and recommended values.

1. Whenever power is cycled on the chip, the registers are reset to their power on reset (not necessarily recommended) state.
2. In the main register map, there are several registers with only 1's and 0's and no defined words. DO NOT ASSUME that these registers do not need to be programmed. In many cases, these 1's and 0's are different than the power on reset values.
3. In the register description, the word 'RESET' is used, but what is really meant is "Recommended" State

7.6 Register Map

This device has 128 registers from R0 to R127. They must be programmed in REVERSE order. Note that there are several registers that have no description, but they still need to be programmed as the power on reset value is not always the correct value. The complete listing for all registers, including those not described in this datasheet are available on the Registers tab on the TI TICSPRO software.

Table 6. Full Register Map

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|------------------------|-----|--------|-------|-----|--------------|-----------------|----|-----|----|----|-------------|----------------|---------------|--------|
| R0 | 0 | SYNC_P HASE_P LL | 1 | 0 | 0 | 0 | OUT_MU TE | FCAL_HPFD_ADJ 0 | | | 0 | 1 | FCAL_E N | MUXOU T_SEL | RESET_ PLL | PLL_PD |
| R1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CAL_CLK_DIV | | |
| R2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R3 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| R4 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| R5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| R6 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| R7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| R8 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R9 | 0 | 0 | 0 | OSC_2X | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| R10 | 0 | 0 | 0 | 1 | MULT | | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| R11 | 0 | 0 | 0 | 0 | PLL_R | | | | | | | 1 | 0 | 0 | 0 | |
| R12 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R13 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R14 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | CPG | | | 0 | 0 | 0 | 0 |
| R15 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| R16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R17 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| R18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| R19 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| R20 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| R21 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R23 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| R24 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| R25 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| R26 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| R27 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| R28 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| R29 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| R30 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| R31 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

Table 6. Full Register Map (continued)

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|-----|-------------------------|-----|-------------|-----|-----|-----|----|----|-----------|----|------------------|----|----|------------|------------|-------------|---|
| R32 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | |
| R33 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | |
| R34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R35 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | |
| R36 | PLL_N | | | | | | | | | | | | | | | | |
| R37 | 1 | 0 | PFD_DLY_SEL | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| R38 | PLL_DEN[31:16] | | | | | | | | | | | | | | | | |
| R39 | PLL_DEN[15:0] | | | | | | | | | | | | | | | | |
| R40 | MASH_SEED[31:16] | | | | | | | | | | | | | | | | |
| R41 | MASH_SEED[15:0] | | | | | | | | | | | | | | | | |
| R42 | PLL_NUM[31:16] | | | | | | | | | | | | | | | | |
| R43 | PLL_NUM[15:0] | | | | | | | | | | | | | | | | |
| R44 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | LO_OUT_PD | 0 | MASH_R ESET_N | 0 | 0 | MASH_ORDER | | | |
| R45 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | |
| R46 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | LO_OUT_MUX | | |
| R47 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R48 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R49 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R51 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R52 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| R53 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R54 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R55 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R57 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R58 | SYNC_PI N_IGNO RE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| R59 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LD_TYP E | |
| R60 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | |
| R61 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | |
| R62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | |

Table 6. Full Register Map (continued)

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|-----|-----------------------|------------|-----|------------|-----------------|--------------|--------------------|----|------------------|----|---------------|----|----|------------------|------------------|------------------|-------------|
| R63 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R64 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| R65 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R66 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | |
| R67 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R68 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | |
| R69 | MASH_RST_COUNT[31:16] | | | | | | | | | | | | | | | | |
| R70 | MASH_RST_COUNT[15:0] | | | | | | | | | | | | | | | | |
| R71 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| R72 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| R73 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| R74 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R75 | 0 | 0 | 0 | 0 | 1 | CHDIV | | | | | 0 | 0 | 0 | 0 | 0 | 0 | |
| R76 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | |
| R77 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R78 | 0 | 0 | 0 | 0 | 0 | 0 | VCO_CALSTART_CLOSE | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | |
| R79 | 0 | LO_PATH_EN | | | 0 | 0 | 0 | 0 | 0 | 0 | IFA_PULLUP_EN | 0 | 0 | 0 | LNA_PD | SIGPATH_RST | SIGCHAIN_PD |
| R80 | 0 | 0 | 0 | 0 | SYNC_PHASE_MXLO | SYNC_DRV2_EN | SYNC_DRV1_EN | 0 | 0 | 0 | LO_MUX | | | | | | |
| R81 | 0 | 0 | 0 | 0 | LO_POLY_MODE1 | | | | EXTLO_CLK_DIV_EN | | LO_DRV_MODE | | 0 | EXTLO_CLK_DRV_EN | | SM_CLK_SEL | |
| R82 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | EXTLO_DIV | | | | | | |
| R83 | IFA_PULLUP | | | VCM_CONFIG | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | |
| R84 | DCOC_CLK_DIV | | | | | | | | | | 0 | 0 | 0 | 0 | EN_DCO_C_QCH_LUT | EN_DCO_C_ICH_LUT | |
| R85 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R86 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R87 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R88 | rb_DCOC_CAL | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| R89 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R90 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Table 6. Full Register Map (continued)

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|------|------------------------|------------|---------------|-----|-----|-------------|----|-----------------|----------------|-------------------------|----|----|----|----|----|----|---|
| R91 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R92 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R93 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R94 | IMRR_GCAL_QCH | | | | | | | IMRR_GCAL_ICH | | | | | | | | | |
| R95 | IMRR_P HCAL_P OL | IMRR_PHCAL | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R96 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | |
| R97 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R98 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R99 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| R101 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| R102 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R103 | 0 | 0 | LO_POLY_MODE2 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R104 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| R105 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | |
| R106 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R107 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R108 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R109 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R110 | 0 | 0 | 0 | 0 | 0 | rb_LD_VTUNE | | 0 | rb_VCO_SEL | | | 0 | 0 | 0 | 0 | 0 | |
| R111 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | rb_VCO_CAPCTRL | | | | | | | | |
| R112 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | rb_VCO_DACISSET | | | | | | | | | |
| R113 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R114 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R115 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R116 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R117 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R118 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R119 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | |
| R120 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R121 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BIAS_LNA_CUR_C ONFIG | | 0 | 0 | 0 | 0 | 0 | |
| R122 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Table 6. Full Register Map (continued)

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|-------------------------|----|
| R123 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EXTLO_INT_MATC H_RES | |
| R124 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R125 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R126 | IMRR_P HCAL_E XTEND | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R127 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 7 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 7 should be considered as reserved locations and the register contents should not be modified.

Table 7. Device Registers

| Address | Acronym | Register Name | Section |
|---------|---------|---------------|--------------------|
| 0x0 | R0 | | Go |
| 0x1 | R1 | | Go |
| 0x2 | R2 | | Go |
| 0x9 | R9 | | Go |
| 0xA | R10 | | Go |
| 0xB | R11 | | Go |
| 0xE | R14 | | Go |
| 0x24 | R36 | | Go |
| 0x25 | R37 | | Go |
| 0x26 | R38 | | Go |
| 0x27 | R39 | | Go |
| 0x28 | R40 | | Go |
| 0x29 | R41 | | Go |
| 0x2A | R42 | | Go |
| 0x2B | R43 | | Go |
| 0x2C | R44 | | Go |
| 0x2E | R46 | | Go |
| 0x3A | R58 | | Go |
| 0x3B | R59 | | Go |
| 0x45 | R69 | | Go |
| 0x46 | R70 | | Go |
| 0x4B | R75 | | Go |
| 0x4E | R78 | | Go |
| 0x4F | R79 | | Go |
| 0x50 | R80 | | Go |
| 0x51 | R81 | | Go |
| 0x52 | R82 | | Go |
| 0x53 | R83 | | Go |
| 0x54 | R84 | | Go |
| 0x58 | R88 | | Go |
| 0x5E | R94 | | Go |
| 0x5F | R95 | | Go |
| 0x67 | R103 | | Go |
| 0x6E | R110 | | Go |
| 0x6F | R111 | | Go |
| 0x70 | R112 | | Go |
| 0x79 | R121 | | Go |
| 0x7B | R123 | | Go |
| 0x7E | R126 | | Go |

Complex bit access types are encoded to fit into small table cells. Table 8 shows the codes that are used for access types in this section.

Table 8. Device Access Type Codes

| Access Type | Code | Description |
|-------------------------------|------|--|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| -n | | Value after reset or the default value |

7.6.1 R0 Register (Address = 0x0) [reset = X]

R0 is shown in [Figure 52](#) and described in [Table 9](#).

Return to [Summary Table](#).

Figure 52. R0 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----------|---|---|---------|------------|-----------|---------|
| FCAL_HPFD_ADJ | RESERVED | | | FCAL_EN | MUXOUT_SEL | RESET_PLL | PLL_PD |
| R/W-0x0 | R-0x0 | | | R/W-0x1 | R/W-0x1 | R/W-0x0 | R/W-0x0 |

Table 9. R0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 14 | SYNC_PHASE_PLL | R/W | X | Puts PLL in SYNC mode so that the channel divider can be synchronized |
| 13-10 | RESERVED | R | X | |
| 9 | OUT_MUTE | R/W | X | Output buffer automute. 0x0 = Disabled 0x1 = Mutes output buffer during FCAL and when PLL not locked |
| 8-7 | FCAL_HPFD_ADJ | R/W | 0x0 | VCO calibration adjust for higher phase detector frequencies 0x0 = Fpd < 100 MHz 0x1 = Fpd 100 - 150 MHz 0x2 = Fpd 150 - 200 MHz 0x3 = Fpd > 200 MHz |
| 6-4 | RESERVED | R | 0x0 | |
| 3 | FCAL_EN | R/W | 0x1 | Enables frequency calibration. When this bit is high, the VCO frequency calibration will be triggered whenever the R0 register is written to. |
| 2 | MUXOUT_SEL | R/W | 0x1 | Selects to route readback serial data output or lock detect output at the MUXout pin 0x0 = Readback 0x1 = Lock Detect |
| 1 | RESET_PLL | R/W | 0x0 | Reset registers to default values. This bit is self-clearing. 0x0 = No Reset 0x1 = Trigger Reset |
| 0 | PLL_PD | R/W | 0x0 | PLL power down. 0x0 = Powerd Up 0x1 = Powered Down |

7.6.2 R1 Register (Address = 0x1) [reset = 0x3]

R1 is shown in [Figure 53](#) and described in [Table 10](#).

Return to [Summary Table](#).

Figure 53. R1 Register

| | | | | | | | |
|----------|---|---|---|---|-------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | CAL_CLK_DIV | | |
| R-0x0 | | | | | R/W-0x3 | | |

Table 10. R1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7-3 | RESERVED | R | 0x0 | |
| 2-0 | CAL_CLK_DIV | R/W | 0x3 | Divides down for state machine clock [SM clock = $F_{osc}/2^{CAL_CLK_DIV}$]. Maximum state machine clock frequency is 200MHz. For fastest calibration speed, choose value which will make state machine clock closest to 200 MHz. |

7.6.3 R2 Register (Address = 0x2) [reset = X]

R2 is shown in [Figure 54](#) and described in [Table 11](#).

Return to [Summary Table](#).

Figure 54. R2 Register

| | | | | | | | |
|----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 11. R2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|-----------------------------|
| 10 | SM_CLK_EN | R/W | X | Enables state machine clock |
| 9-0 | RESERVED | R | 0x0 | |

7.6.4 R9 Register (Address = 0x9) [reset = X]

R9 is shown in [Figure 55](#) and described in [Table 12](#).

Return to [Summary Table](#).

Figure 55. R9 Register

| | | | | | | | |
|----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 12. R9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 12 | OSC_2X | R/W | X | Enables the frequency doubler after the input reference signal. 0x0 = Bypass 0x1 = Enable doubler |
| 11-0 | RESERVED | R | 0x0 | |

7.6.5 R10 Register (Address = 0xA) [reset = 0x80]

R10 is shown in [Figure 56](#) and described in [Table 13](#).

Return to [Summary Table](#).

Figure 56. R10 Register

| | | | | | | | |
|---------|---|----------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MULT | | RESERVED | | | | | |
| R/W-0x1 | | R-0x0 | | | | | |

Table 13. R10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 11-7 | MULT | R/W | 0x1 | Input signal multiplier. When not in bypass, input range is 40-70MHz, output range is 180-250MHz. 1,3,4,5,6, and 7 are the only valid values. 0x1 = Bypass 0x3 = x3 0x4 = x4 0x5 = x5 0x6 = x6 |
| 6-0 | RESERVED | R | 0x0 | |

7.6.6 R11 Register (Address = 0xB) [reset = 0x10]

R11 is shown in [Figure 57](#) and described in [Table 14](#).

Return to [Summary Table](#).

Figure 57. R11 Register

| | | | | | | | |
|---------|---|---|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL_R | | | | RESERVED | | | |
| R/W-0x1 | | | | R-0x0 | | | |

Table 14. R11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 11-4 | PLL_R | R/W | 0x1 | PLL R divider that is after the input multiplier. |
| 3-0 | RESERVED | R | 0x0 | |

7.6.7 R14 Register (Address = 0xE) [reset = 0x70]

R14 is shown in [Figure 58](#) and described in [Table 15](#).

Return to [Summary Table](#).

Figure 58. R14 Register

| | | | | | | | |
|----------|---|---------|---|---|----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CPG | | | RESERVED | | |
| R-0x0 | | R/W-0x7 | | | R-0x0 | | |

Table 15. R14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | RESERVED | R | 0x0 | |
| 6-4 | CPG | R/W | 0x7 | Charge pump gain 0x0 = 0 mA 0x1 = 6 mA 0x2 = 6 mA 0x3 = 12 mA 0x4 = 3 mA 0x5 = 9 mA 0x6 = 9 mA 0x7 = 15 mA |
| 3-0 | RESERVED | R | 0x0 | |

7.6.8 R36 Register (Address = 0x24) [reset = 0x64]

 R36 is shown in [Figure 59](#) and described in [Table 16](#).

 Return to [Summary Table](#).

Figure 59. R36 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL_N | | | | | | | | | | | | | | | |
| R/W-0x64 | | | | | | | | | | | | | | | |

Table 16. R36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 15-0 | PLL_N | R/W | 0x64 | Integer part of N divider |

7.6.9 R37 Register (Address = 0x25) [reset = 0x200]

 R37 is shown in [Figure 60](#) and described in [Table 17](#).

 Return to [Summary Table](#).

Figure 60. R37 Register

| | | | | | | | |
|----------|----|----|----|-------------|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | PFD_DLY_SEL | | | |
| R-0x0 | | | | R/W-0x2 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 17. R37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 15-14 | RESERVED | R | 0x0 | |
| 13-8 | PFD_DLY_SEL | R/W | 0x2 | Sets the appropriate delay adjustment for the phase detector based on PLL_N, MASH_ORDER, and phase detector frequency. |
| 7-0 | RESERVED | R | 0x0 | |

7.6.10 R38 Register (Address = 0x26) [reset = 0x0]

R38 is shown in [Figure 61](#) and described in [Table 18](#).

Return to [Summary Table](#).

Figure 61. R38 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL_DEN_31:16 | | | | | | | | | | | | | | | |
| R/W-0x0 | | | | | | | | | | | | | | | |

Table 18. R38 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 15-0 | PLL_DEN_31:16 | R/W | 0x0 | Denominator of N divider fraction (MSB) |

7.6.11 R39 Register (Address = 0x27) [reset = 0x2710]

R39 is shown in [Figure 62](#) and described in [Table 19](#).

Return to [Summary Table](#).

Figure 62. R39 Register

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL_DEN | | | | | | | | | | | | | | | |
| R/W-0x2710 | | | | | | | | | | | | | | | |

Table 19. R39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|--------|---|
| 15-0 | PLL_DEN | R/W | 0x2710 | Denominator of N divider fraction (LSB) |

7.6.12 R40 Register (Address = 0x28) [reset = 0x0]

R40 is shown in [Figure 63](#) and described in [Table 20](#).

Return to [Summary Table](#).

Figure 63. R40 Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASH_SEED_31:16 | | | | | | | | | | | | | | | |
| R/W-0x0 | | | | | | | | | | | | | | | |

Table 20. R40 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|----------------------|
| 15-0 | MASH_SEED_31:16 | R/W | 0x0 | MSB bit of MASH_SEED |

7.6.13 R41 Register (Address = 0x29) [reset = 0x0]

R41 is shown in [Figure 64](#) and described in [Table 21](#).

Return to [Summary Table](#).

Figure 64. R41 Register

| | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASH_SEED | | | | | | | | | | | | | | | |
| R/W-0x0 | | | | | | | | | | | | | | | |

Table 21. R41 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 15-0 | MASH_SEED | R/W | 0x0 | The MASH_SEED can be used for optimizing fractional mode (see simulation tool) and also phase adjustment feature. Phase adjustment writing to this register will trigger a phase shift (in degrees) = $360 \times [\text{MASH_SEED}] \times [\text{PLL_N_PRE}] / [\text{N-divider denominator}] / [\text{Channel divider}]$. MASH_SEED must be less than N-divider denominator For example, for MASH_SEED = 100, PLL_N_PRE=2, PLL_DEN = 200, CHDIV=3, Phase Shift = $360 * 100 * 2 / 200 / 3 = 120$ degrees |

7.6.14 R42 Register (Address = 0x2A) [reset = 0x0]

R42 is shown in [Figure 65](#) and described in [Table 22](#).

Return to [Summary Table](#).

Figure 65. R42 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL_NUM_31:16 | | | | | | | | | | | | | | | |
| R/W-0x0 | | | | | | | | | | | | | | | |

Table 22. R42 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---------------------------------------|
| 15-0 | PLL_NUM_31:16 | R/W | 0x0 | Numerator of N divider fraction (MSB) |

7.6.15 R43 Register (Address = 0x2B) [reset = 0x0]

R43 is shown in [Figure 66](#) and described in [Table 23](#).

Return to [Summary Table](#).

Figure 66. R43 Register

| | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL_NUM | | | | | | | | | | | | | | | |
| R/W-0x0 | | | | | | | | | | | | | | | |

Table 23. R43 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---------------------------------------|
| 15-0 | PLL_NUM | R/W | 0x0 | Numerator of N divider fraction (LSB) |

7.6.16 R44 Register (Address = 0x2C) [reset = 0xA2]

R44 is shown in [Figure 67](#) and described in [Table 24](#).

Return to [Summary Table](#).

Figure 67. R44 Register

| | | | | | | | |
|-----------|----------|--------------|----------|----|----|------------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LO_OUT_PD | RESERVED | MASH_RESET_N | RESERVED | | | MASH_ORDER | |
| R/W-0x1 | R-0x0 | R/W-0x1 | R-0x0 | | | R/W-0x2 | |

Table 24. R44 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 15-8 | RESERVED | R | 0x0 | |
| 7 | LO_OUT_PD | R/W | 0x1 | Disable output buffer of output A 0x0 = Enable 0x1 = Disable (disable if not using output B) |
| 6 | RESERVED | R | 0x0 | |
| 5 | MASH_RESET_N | R/W | 0x1 | MASH enable. Should be set to 1 in fractional mode. To reset the MASH toggle from 0 to 1. |
| 4-3 | RESERVED | R | 0x0 | |
| 2-0 | MASH_ORDER | R/W | 0x2 | Fractional-N divider sigma-delta MASH engine order. This sets the algorithm used in fractional-N mode generation and has impact on fractional spurs. Refer to the datasheet for more information. Recommended values are as follows, but other values may also work. |

7.6.17 R46 Register (Address = 0x2E) [reset = 0x1]

 R46 is shown in [Figure 68](#) and described in [Table 25](#).

 Return to [Summary Table](#).

Figure 68. R46 Register

| | | | | | | | |
|----------|----|----|----|----|----|------------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | LO_OUT_MUX | |
| R-0x0 | | | | | | R/W-0x1 | |

Table 25. R46 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 15-2 | RESERVED | R | 0x0 | |
| 1-0 | LO_OUT_MUX | R/W | 0x1 | Selects signal to route to output B 0x0 = Selects the output from channel divider MUX 0x1 = Selects output from VCO |

7.6.18 R58 Register (Address = 0x3A) [reset = 0x8000]

 R58 is shown in [Figure 69](#) and described in [Table 26](#).

 Return to [Summary Table](#).

Figure 69. R58 Register

| | | | | | | | |
|---------------------|----------|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SYNC_PIN_IG NORE | RESERVED | | | | | | |
| R/W-0x1 | R-0x0 | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 26. R58 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 15 | SYNC_PIN_IGNORE | R/W | 0x1 | Enable this bit when NOT using SYNC mode as the SYNC pin interferes with lock detect in this case. When PLL_PHASE_SYNC=1, this bit may be disabled with no issues with lock detect. |
| 14-0 | RESERVED | R | 0x0 | |

7.6.19 R59 Register (Address = 0x3B) [reset = 0x1]

 R59 is shown in [Figure 70](#) and described in [Table 27](#).

 Return to [Summary Table](#).

Figure 70. R59 Register

| | | | | | | | |
|----------|----|----|----|----|----|---|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | LD_TYPE |
| R-0x0 | | | | | | | R/W-0x1 |

Table 27. R59 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-1 | RESERVED | R | 0x0 | |
| 0 | LD_TYPE | R/W | 0x1 | Lock detect type. VCOCal lock detect is high except when the VCO is calibrating and also during a timeout count right after calibration set LD_DLY. Vtune and VCOCal lock detect is high whenever VCOCal lock detect would be high and the VCO tuning voltage is within an acceptable range. 0x0 = VCOCal 0x1 = Vtune and VCOCal. |

7.6.20 R69 Register (Address = 0x45) [reset = 0x0]

 R69 is shown in [Figure 71](#) and described in [Table 28](#).

 Return to [Summary Table](#).

Figure 71. R69 Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASH_RST_COUNT_31:16 | | | | | | | | | | | | | | | |
| R/W-0x0 | | | | | | | | | | | | | | | |

Table 28. R69 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-----------------------|
| 15-0 | MASH_RST_COUNT_31:16 | R/W | 0x0 | MSB of MASH_RST_COUNT |

7.6.21 R70 Register (Address = 0x46) [reset = 0xC350]

 R70 is shown in [Figure 72](#) and described in [Table 29](#).

 Return to [Summary Table](#).

Figure 72. R70 Register

| | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASH_RST_COUNT | | | | | | | | | | | | | | | |
| R/W-0xC350 | | | | | | | | | | | | | | | |

Table 29. R70 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|--------|---|
| 15-0 | MASH_RST_COUNT | R/W | 0xC350 | When using a fractional N value with PLL_PHASE_SYNC=1, this is used to set a delay to allow the SYNC to work properly. In general, it should be set to a count equal to 4X the analog settling time of the PLL. (LSB) |

7.6.22 R75 Register (Address = 0x4B) [reset = 0x0]

R75 is shown in [Figure 73](#) and described in [Table 30](#).

Return to [Summary Table](#).

Figure 73. R75 Register

| | | | | | | | |
|----------|----|----------|----|----|----|---------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | CHDIV | |
| R-0x0 | | | | | | R/W-0x0 | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHDIV | | RESERVED | | | | | |
| R/W-0x0 | | R-0x0 | | | | | |

Table 30. R75 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 15-11 | RESERVED | R | 0x0 | |
| 10-6 | CHDIV | R/W | 0x0 | Channel divider that divides the VCO frequency. |
| 5-0 | RESERVED | R | 0x0 | |

7.6.23 R78 Register (Address = 0x4E) [reset = 0x0]

R78 is shown in [Figure 74](#) and described in [Table 31](#).

Return to [Summary Table](#).

Figure 74. R78 Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | VCO_CALSTA RT_CLOSE | RESERVED |
| R-0x0 | | | | | | R/W-0x0 | R-0x0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 31. R78 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 15-10 | RESERVED | R | 0x0 | |
| 9 | VCO_CALSTART_CLOS E | R/W | 0x0 | Uses current values for VCO core, frequency band, and amplitude as the starting point for the next VCO calibration. Enable this if the VCO frequency change is close, on the order of 50 MHz or less. |
| 8-0 | RESERVED | R | 0x0 | |

7.6.24 R79 Register (Address = 0x4F) [reset = 0x7000]

 R79 is shown in [Figure 75](#) and described in [Table 32](#).

 Return to [Summary Table](#).

Figure 75. R79 Register

| | | | | | | | |
|----------|---------------|----------|----|----------|---------|-------------|-------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | LO_PATH_EN | | | RESERVED | | | |
| R-0x0 | R/W-0x7 | | | R-0x0 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | IFA_PULLUP_EN | RESERVED | | | LNA_PD | SIGPATH_RST | SIGCHAIN_PD |
| R-0x0 | R/W-0x0 | R-0x0 | | | R/W-0x0 | R/W-0x0 | R/W-0x0 |

Table 32. R79 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 15 | RESERVED | R | 0x0 | |
| 14-12 | LO_PATH_EN | R/W | 0x7 | Enables various parts of the Poly and DIV2 Path |
| 11-7 | RESERVED | R | 0x0 | |
| 6 | IFA_PULLUP_EN | R/W | 0x0 | Enable the pull up resistor at the input of the IFA. Needed when the output comoon mode is <1.4V |
| 5-3 | RESERVED | R | 0x0 | |
| 2 | LNA_PD | R/W | 0x0 | LNA power down |
| 1 | SIGPATH_RST | R/W | 0x0 | Master reset for the signal chain |
| 0 | SIGCHAIN_PD | R/W | 0x0 | Master power down for the signal chain. |

7.6.25 R80 Register (Address = 0x50) [reset = 0xA]

 R80 is shown in [Figure 76](#) and described in [Table 33](#).

 Return to [Summary Table](#).

Figure 76. R80 Register

| | | | | | | | |
|----------|----|---------|----|------------------|--------------|--------------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | SYNC_PHASE_MIXLO | SYNC_DRV2_EN | SYNC_DRV1_EN | RESERVED |
| R-0x0 | | | | R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | LO_MUX | | | | | |
| R-0x0 | | R/W-0xA | | | | | |

Table 33. R80 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 15-12 | RESERVED | R | 0x0 | |
| 11 | SYNC_PHASE_MIXLO | R/W | 0x0 | Sync bit to close the loop from Mixer LO back to synthesizer |
| 10 | SYNC_DRV2_EN | R/W | 0x0 | Enables the SYNC 2nd stage driver from the LO output path. It should be enabled in SYNC mode. 0x0 = Disabled 0x1 = Enabled |
| 9 | SYNC_DRV1_EN | R/W | 0x0 | Enables the SYNC first stage driver from the LO output path. It should be enabled in SYNC mode. 0x0 = Disabled 0x1 = Enabled |
| 8-6 | RESERVED | R | 0x0 | |

Table 33. R80 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 5-0 | LO_MUX | R/W | 0xA | Sets up various MUXs and Drivers 0x9 = Internal LO DIV2 Mode 0x10 = Internal LO Poly 48 External LO |

7.6.26 R81 Register (Address = 0x51) [reset = 0x0]

R81 is shown in [Figure 77](#) and described in [Table 34](#).

Return to [Summary Table](#).

Figure 77. R81 Register

| | | | | | | | |
|------------------|----|-------------|----|---------------|------------------|---|------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | LO_POLY_MODE1 | | | |
| R-0x0 | | | | R/W-0x0 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EXTLO_CLK_DIV_EN | | LO_DRV_MODE | | RESERVED | EXTLO_CLK_DRV_EN | | SM_CLK_SEL |
| R/W-0x0 | | R/W-0x0 | | R-0x0 | R/W-0x0 | | R/W-0x0 |

Table 34. R81 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 15-12 | RESERVED | R | 0x0 | |
| 11-8 | LO_POLY_MODE1 | R/W | 0x0 | Sets up parameters for the poly path 0x0 = Internal LO Poly 0x15 = External LO 0x19 = Internal LO DIV2 |
| 7-6 | EXTLO_CLK_DIV_EN | R/W | 0x0 | Selects driver for SMCLK 0x0 = Internal LO 0x1 = Reserved 0x2 = Reserved 0x3 = External LO |
| 5-4 | LO_DRV_MODE | R/W | 0x0 | Sets up drivers for LO quadrature path 0x0 = Internal LO Poly 0x1 = Internal LO DIV2 0x2 = Reserved 0x3 = External LO |
| 3 | RESERVED | R | 0x0 | |
| 2-1 | EXTLO_CLK_DRV_EN | R/W | 0x0 | Enables drivers for state machine clock. |
| 0 | SM_CLK_SEL | R/W | 0x0 | Selects the state machine clock source for the signal path 0x0 = Internal LO 0x1 = External LO |

7.6.27 R82 Register (Address = 0x52) [reset = 0x23]

R82 is shown in [Figure 78](#) and described in [Table 35](#).

Return to [Summary Table](#).

Figure 78. R82 Register

| | | | | | | | |
|----------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | |
|----------|-----------|
| RESERVED | EXTLO_DIV |
| R-0x0 | R/W-0x23 |

Table 35. R82 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|--|
| 15-6 | RESERVED | R | 0x0 | |
| 5-0 | EXTLO_DIV | R/W | 0x23 | Sets total divide value for the state machine clock when using an external LO. This total divide is the product of two divides, DIVA and DIVB. 0x0 = 1 0x1 = 2 0x2 = 16 0x3 = 8 0x4 = 16 0x5 = 16 0x6 = 64 0x7 = 8 |

7.6.28 R83 Register (Address = 0x53) [reset = 0x2000]

 R83 is shown in [Figure 79](#) and described in [Table 36](#).

 Return to [Summary Table](#).

Figure 79. R83 Register

| | | | | | | | |
|------------|----|----|------------|----|----|---|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IFA_PULLUP | | | VCM_CONFIG | | | | RESERVED |
| R/W-0x1 | | | R/W-0x0 | | | | R-0x0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 36. R83 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 15-13 | IFA_PULLUP | R/W | 0x1 | IFA virtual node pull up resistor to set the biasing of the IFA input stage correct when the output common mode is <1.4V. Should be used in conjunction with the corresponding EN bit in first register. 0x2 = Invalid 0x4 = Invalid 0x5 = Invalid 0x6 = Invalid |
| 12-9 | VCM_CONFIG | R/W | 0x0 | Output Common mode (VOCM) configuration for IFA. Only one bit to be set as high at a time. Only valid states are 0,3,5,9. 0x0 = 1.7 0x3 = 2V 0x5 = External 0x9 = 1.4V |
| 8-0 | RESERVED | R | 0x0 | |

7.6.29 R84 Register (Address = 0x54) [reset = 0x1900]

 R84 is shown in [Figure 80](#) and described in [Table 37](#).

 Return to [Summary Table](#).

Figure 80. R84 Register

| | | | | | | | |
|--------------|----|----------|----|----|----|---------------------|---------------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DCOC_CLK_DIV | | | | | | | |
| R/W-0x64 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DCOC_CLK_DIV | | RESERVED | | | | EN_DCOC_QC H_LUT | EN_DCOC_IC H_LUT |
| R/W-0x64 | | R-0x0 | | | | R/W-0x0 | R/W-0x0 |

Table 37. R84 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 15-6 | DCOC_CLK_DIV | R/W | 0x64 | DCOC clock division controlled |
| 5-2 | RESERVED | R | 0x0 | |
| 1 | EN_DCOC_QCH_LUT | R/W | 0x0 | Enable offset calibration for Q channel. Write 1 to trigger calibration. To re-trigger, clear this bit and then write 1 again. |
| 0 | EN_DCOC_ICH_LUT | R/W | 0x0 | Enable offset calibration for I channel. Write 1 to trigger calibration. To re-trigger, clear this bit and then write 1 again. |

7.6.30 R88 Register (Address = 0x58) [reset = 0x0]

R88 is shown in [Figure 81](#) and described in [Table 38](#).

Return to [Summary Table](#).

Figure 81. R88 Register

| | | | | | | | |
|----------|----|-------------|----------|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | rb_DCOC_CAL | RESERVED | | | | |
| R-0x0 | | R-0x0 | R-0x0 | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 38. R88 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 15 | RESERVED | R | 0x0 | |
| 14 | rb_DCOC_CAL | R | 0x0 | Status bit. Indicates whether I channel DC offset calibration is done. 0x0 = Neither Channel Done 1 I Channel Done 0x2 = Q Channel Done 0x3 = Both Channels Done |
| 13-0 | RESERVED | R | 0x0 | |

7.6.31 R94 Register (Address = 0x5E) [reset = 0x8080]

R94 is shown in [Figure 82](#) and described in [Table 39](#).

Return to [Summary Table](#).

Figure 82. R94 Register

| | | | | | | | |
|---------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IMRR_GCAL_QCH | | | | | | | |
| R/W-0x80 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IMRR_GCAL_ICH | | | | | | | |
| R/W-0x80 | | | | | | | |

Table 39. R94 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--------------------------------------|
| 15-8 | IMRR_GCAL_QCH | R/W | 0x80 | IMRR gain control for the Q channel. |
| 7-0 | IMRR_GCAL_ICh | R/W | 0x80 | IMRR gain control for the I channel. |

7.6.32 R95 Register (Address = 0x5F) [reset = X]

 R95 is shown in [Figure 83](#) and described in [Table 40](#).

 Return to [Summary Table](#).

Figure 83. R95 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 40. R95 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|------|-------|---|
| 15 | IMRR_PHCAL_POL | R/W | X | IMRR Phase polarity control using the phase interpolator. |
| 14-9 | IMRR_PHCAL | R/W | X | IMRR Phase control using the phase interpolator. Preferred method of the IMRR phase correction. |
| 8 | LODRV_IMRR_PHCAL_P OLCTRL | R/W | X | IMRR Phase polarity control using the slew control driver. |
| 7-0 | RESERVED | R | 0x0 | |

7.6.33 R103 Register (Address = 0x67) [reset = X]

 R103 is shown in [Figure 84](#) and described in [Table 41](#).

 Return to [Summary Table](#).

Figure 84. R103 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 41. R103 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 13-10 | LO_POLY_MODE2 | R/W | X | Selects configurations between Poly and DIV2 Mode |
| 9-0 | RESERVED | R | 0x0 | |

7.6.34 R110 Register (Address = 0x6E) [reset = X]

 R110 is shown in [Figure 85](#) and described in [Table 42](#).

 Return to [Summary Table](#).

Figure 85. R110 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|----------|---|---|---|---|
| rb_VCO_SEL | | | RESERVED | | | | |
| R-0x0 | | | R-0x0 | | | | |

Table 42. R110 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 10-9 | rb_LD_VTUNE | R | X | Readback word for the PLL lock status 0x0 = Unlock (Fvco Low) 0x1 = Invalid 0x2 = PLL Locked 0x3 = Unlock (Fvco High) |
| 8 | RESERVED | R | X | |
| 7-5 | rb_VCO_SEL | R | 0x0 | Reads back the VCO core selected. 0x0 = Invalid 0x1 = VCO1 0x2 = VCO2 0x3 = VCO3 0x4 = VCO4 0x5 = VCO5 0x6 = VCO6 0x7 = VCO7 |
| 4-0 | RESERVED | R | 0x0 | |

7.6.35 R111 Register (Address = 0x6F) [reset = 0x0]

R111 is shown in [Figure 86](#) and described in [Table 43](#).

Return to [Summary Table](#).

Figure 86. R111 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|
| rb_VCO_CAPCTRL | | | | | | | |
| R-0x0 | | | | | | | |

Table 43. R111 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7-0 | rb_VCO_CAPCTRL | R | 0x0 | Readback word for the actual value of VCO_CAPCTRL chosen by the VCO frequency calibration. |

7.6.36 R112 Register (Address = 0x70) [reset = 0x0]

R112 is shown in [Figure 87](#) and described in [Table 44](#).

Return to [Summary Table](#).

Figure 87. R112 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---|---|---|---|---|---|---|
| rb_VCO_DACISSET | | | | | | | |
| R-0x0 | | | | | | | |

Table 44. R112 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 8-0 | rb_VCO_DACISSET | R | 0x0 | Readback word for the actual value of VCO_DACISSET chosen by the VCO amplitude calibration. |

7.6.37 R121 Register (Address = 0x79) [reset = 0x0]

 R121 is shown in [Figure 88](#) and described in [Table 45](#).

 Return to [Summary Table](#).

Figure 88. R121 Register

| | | | | | | | |
|----------|---|-----------------------|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | BIAS_LNA_CUR_CONFIG_2 | | RESERVED | | | |
| R-0x0 | | R/W-0x0 | | R-0x0 | | | |

Table 45. R121 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|-------------|
| 7 | RESERVED | R | 0x0 | |
| 6-5 | BIAS_LNA_CUR_CONFIG_2 | R/W | 0x0 | |
| 4-0 | RESERVED | R | 0x0 | |

7.6.38 R123 Register (Address = 0x7B) [reset = 0x3]

 R123 is shown in [Figure 89](#) and described in [Table 46](#).

 Return to [Summary Table](#).

Figure 89. R123 Register

| | | | | | | | |
|----------|---|---|---|---|---|---------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | EXTLO_INT_MATCH_RES | |
| R-0x0 | | | | | | R/W-0x3 | |

Table 46. R123 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-2 | RESERVED | R | 0x0 | |
| 1-0 | EXTLO_INT_MATCH_RES | R/W | 0x3 | Control internal resistor termination at EXTLO input pin 0x0 = No termination 0x1 = 200 Ohms differential termination 0x2 = Same as 1 0x3 = 100 Ohms differential termination |

7.6.39 R126 Register (Address = 0x7E) [reset = X]

 R126 is shown in [Figure 90](#) and described in [Table 47](#).

 Return to [Summary Table](#).

Figure 90. R126 Register

| | | | | | | | |
|----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |

Table 47. R126 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|---|
| 15 | IMRR_PHCAL_EXTEND | R/W | X | Increase the range of the IMRR phase interpolator DAC by 2x |
| 14-9 | RESERVED | R | X | |
| 8 | DCOC_FSM_RST | R/W | X | Reset DC offset |
| 7-0 | RESERVED | R | 0x0 | |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Typical Application shows a typical usage of the LMX8410L with internal synthesizer and shows the basic components needed for the operation of the device. There is also guidance on how to design the loop external loop filter which is part of the LMX8410L synthesizer. The PLLatinum Sim is a tool that allows users to enter the information regarding the input reference and target LO frequency they need and simulate the expected phase noise and performance parameters for the synthesizer.

8.2 Typical Application

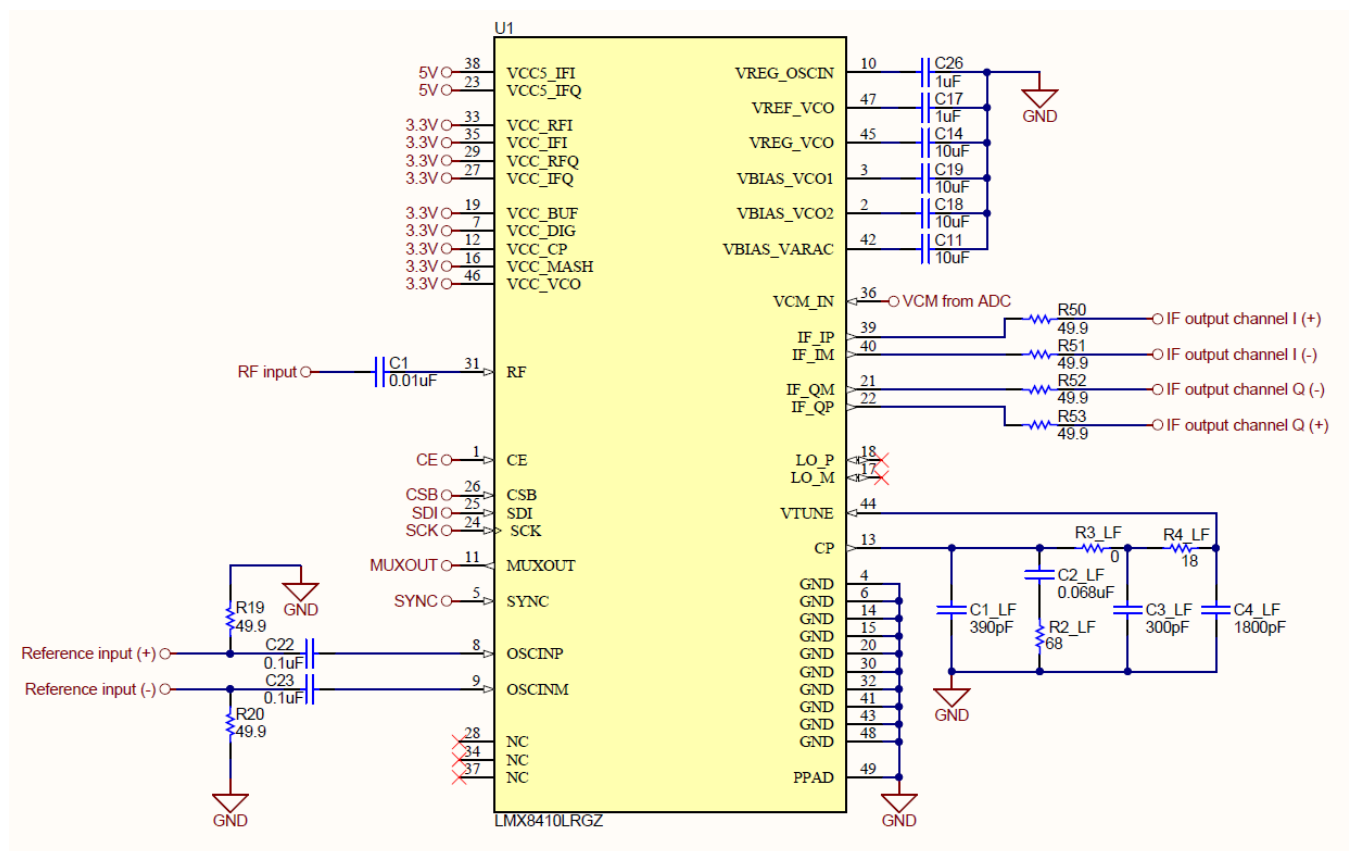


Figure 91. Typical Application Schematic

8.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLatinum Sim software is an excellent resource for doing this and the design is shown in the following figure. For those interested in the equations involved, the PLL Performance, Simulation, and Design Handbook listed in the end of this document goes into great detail as to theory and design of PLL loop filters. PLLatinum Sim does not model the mixers and LNAs in this device, but it can be used for the PLL. To use this tool, it can be modeled as the LMX2594 PLL.

Typical Application (continued)

8.2.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this is that longer lock times and spurs must be considered in design as well.

As for software programming, it is highly recommended to use the TICSPRO software. In addition to simplifying the process, it also gives the user recommended programming default values for the undisclosed registers not mentioned in the datasheet.

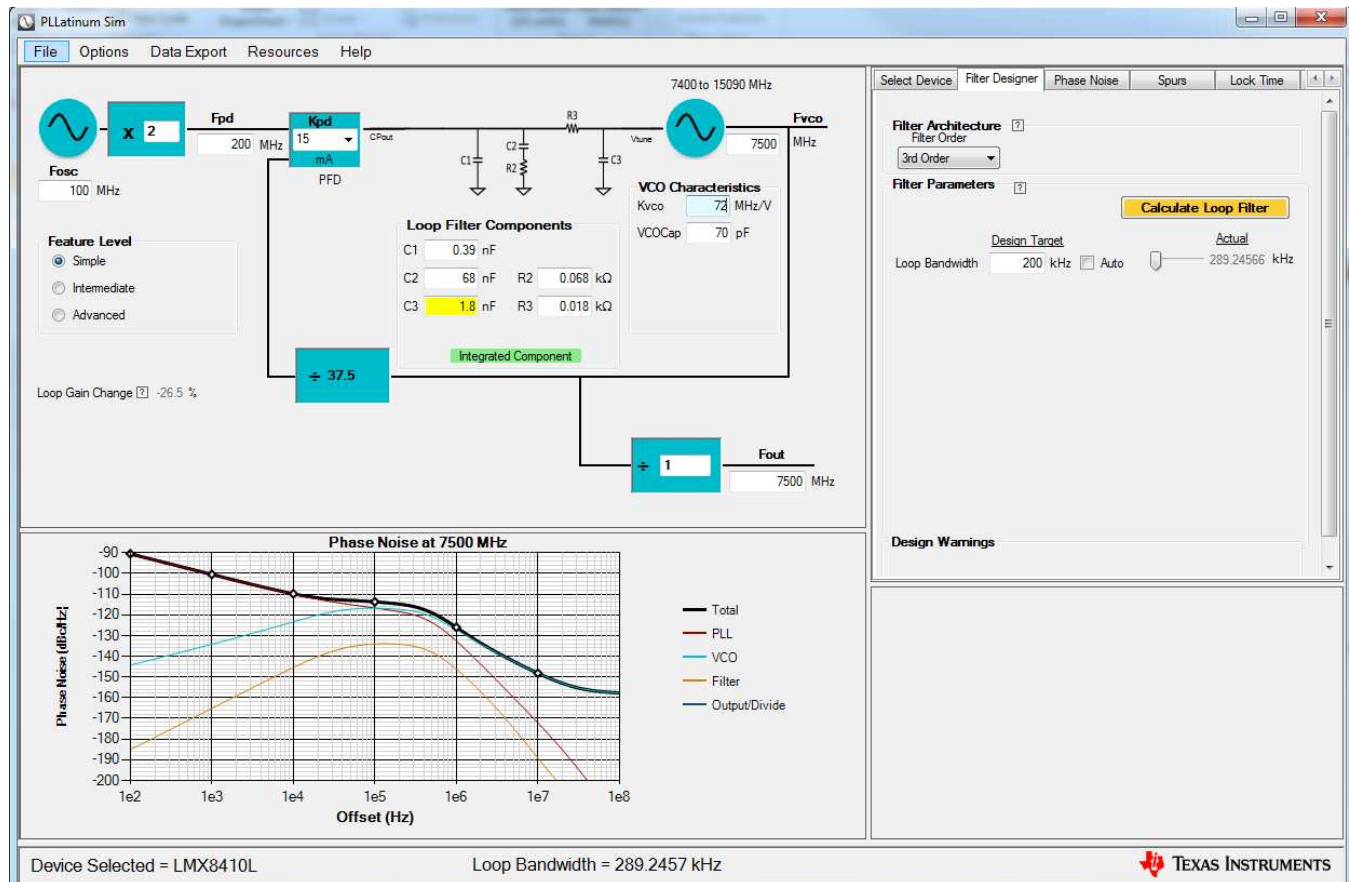
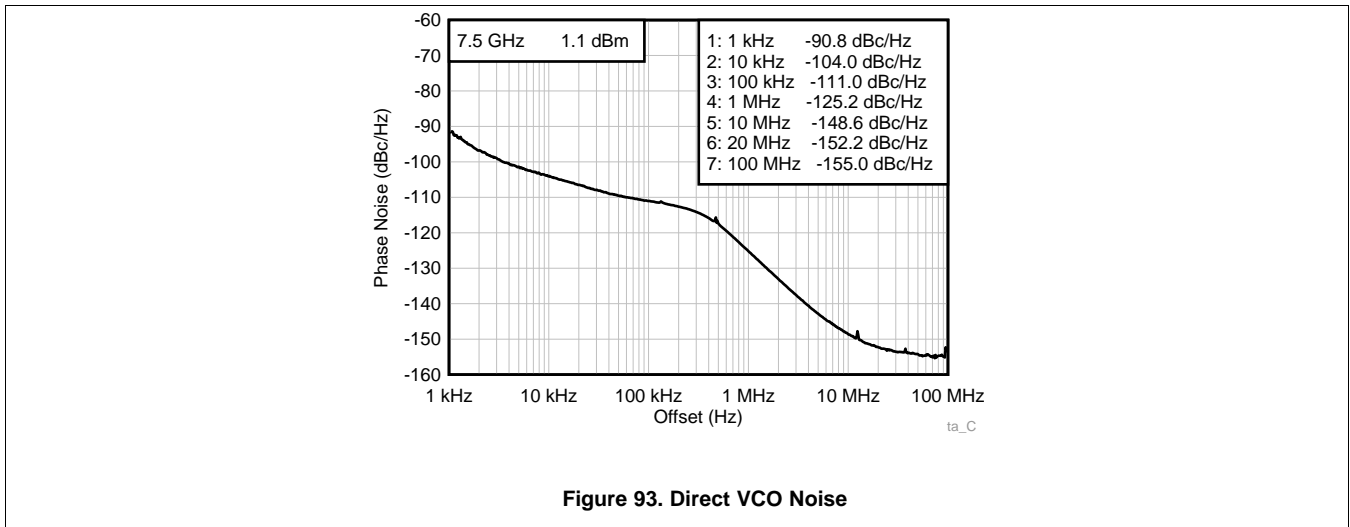


Figure 92. PLLatinum Sim Design Example

Typical Application (continued)

8.2.3 Application Curve



9 Power Supply Recommendations

1. Design 5-V supply to be capable of greater than 200 mA.
2. Design 3.3-V supply to be capable of greater than 800 mA.
3. Supply to channel I and Q sides must be well matched and isolated from one another. Recommend using ferrite beads in series to the pin. The I and Q supplies are for IF amplifier (at pin 38 and 23), for RF input (at pin 33 and 29), and for IF path circuitry (at pin 35 and 27).
4. Pins 7 and 16 are supplies for digital circuitry, and they can have extra isolation in this path (TI recommends using ferrite bead in series to the pin).
5. Pins 12, 19, and 46 are supplies for the internal synthesizer; designer must take care not to have noise sources that can couple to it nearby.
6. Typically use 0.1- μ F capacitors near the pins. Add extra capacitance values at specific frequencies if known interfering frequencies in system. See [Pin Configuration and Functions](#) for more recommendations on component value recommendations.

10 Layout

10.1 Layout Guidelines

Generally, there are two major focuses of layout guidelines: high frequency signals and power routing.

10.1.1 High Frequency Trace Routing

- Design all traces for matched impedance. The single-ended RF trace must be controlled for 50- Ω impedance, while the differential OSCIN, LO, and IF traces must be controlled for 100- Ω differential impedance.
- Run an uninterrupted ground plane beneath all impedance-controlled traces. No other currents should flow directly under the controlled impedance traces.
- Keep high-frequency traces as short as possible to minimize losses, or potential for cross-coupling.
- Controlled impedance can be challenging in materials not designed for RF applications. For example, standard FR-4 has a wide range of acceptable dielectric constants in practice. Although the constants seen in boards from the same panel or material lot code may match very well, this does not ensure that the constants match between different lots or different dielectric manufacturers. Furthermore, FR-4 has a high loss tangent compared to many other materials, which can result in much greater attenuation of high frequency signals across the same distances. TI recommends the use of materials designed specifically for high-frequency use, such as RO4350B or RO4003C from Rogers Corporation.
- The RF pin is surrounded on three sides by ground pins to assist in the creation of a coplanar waveguide structure. Design the coplanar waveguide to minimize current flow on the ground traces around the pins.
- The IF outputs are low impedance, and require resistors to set the output impedance.
- The LO pins are capacitively coupled as inputs, with internal 50- Ω termination. Use 50- Ω pullup resistors to VCC_BUF to bias these pins as inputs, if driven through external capacitors. The LO pins require 50- Ω pullup resistors to VCC_BUF as outputs.
- The LO pins are located very close to the Q-channel IF pins, and the LO buffer supply is located between these two ports. Placing a bypass capacitor as close as possible to the LO buffer is recommended for proper operation, but this presents a potential problem: vias to VCC and GND must be routed between the differential pairs. Because the high frequency currents in the bypass capacitor and the LO buffer circuit tend to follow the loop with the lowest inductance, and since the VCC via interrupts the path from capacitor ground to IC ground on the plane layer immediately below the top, ground currents tend to travel around this via, in the path of the LO and IF coupling to the plane layer. To maintain the signal integrity of both the LO and IF differential traces, no other currents should be flowing immediately below them on the plane layer. Therefore, the LO bypass capacitor ground via must not connect to the plane layer immediately below the capacitor. TI recommends connecting through the subsequent layer. See the Layout Example section on how this is done.

Layout Guidelines (continued)

10.1.2 Power Trace Routing

- Regardless of whether the part is used in internal or external LO mode, all synthesizer VCC and GND pins must be connected properly. If VCC and GND pins are not connected on the synthesizer, the internal power-up procedure may not execute properly. Noise may also be coupled into the mixer from the synthesizer circuitry if power and ground are not properly connected.
- Place bypass capacitors, whenever possible, to minimize the inductance of the current loop formed by the capacitor and the IC. Placing the bypass capacitors on the same surface as the IC allows one terminal to be connected closely to the IC, minimizing this loop. The ground connection can also be made low-inductance by placing a ground via to a plane layer immediately below. Placing capacitors on the opposite surface substantially limits the effective frequencies they can bypass, since the current must travel through two vias. The loop area formed by placing a capacitor on the opposite surface is almost always larger than the loop area formed by placing a capacitor on the same surface.
- Consider the path that ground currents will take. For optimal performance, supply and bypass capacitor currents must not flow underneath high-frequency traces.
- Use as many ground vias as possible to connect the IC pad to the ground plane. This is required for optimal thermal performance.
- Connect ground pins back to the pad. Aside from routing convenience, the inductance through the bond wires tends to be very high, and the inductance through the ground pad tends to be very low.
- Avoid connecting different VCC pins in such a way that the current paths overlap. Overlapping current paths can inject common-mode noise into the supply pins, degrading performance.

10.2 Layout Examples

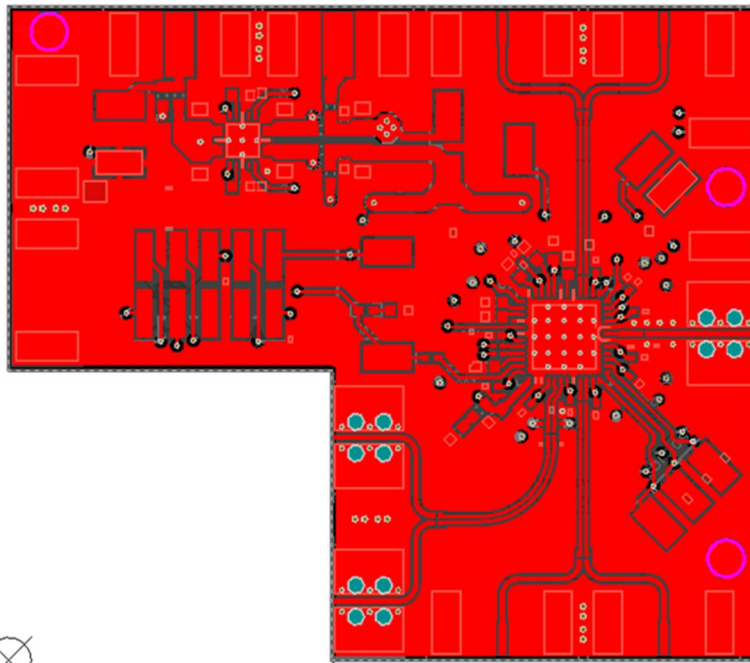


Figure 94. Top Layer

Layout Examples (continued)

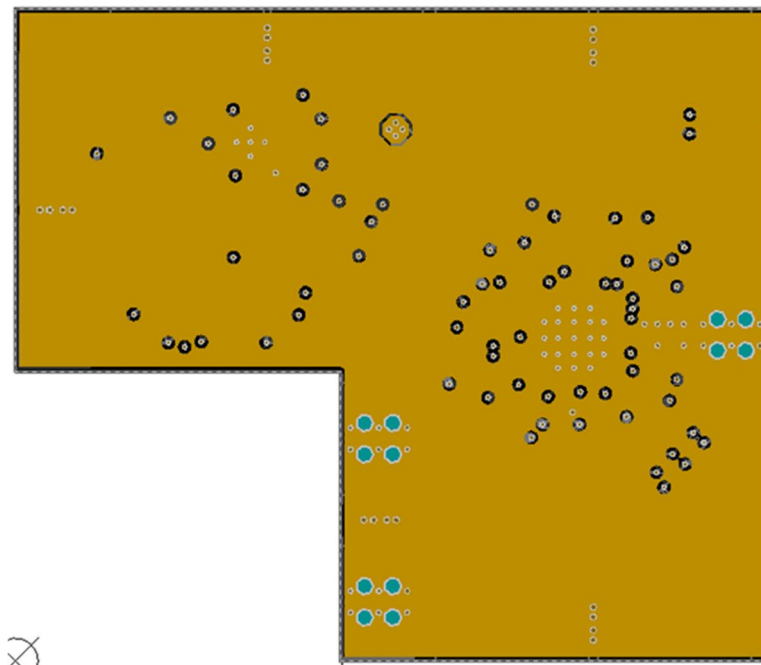


Figure 95. Ground Layer 1

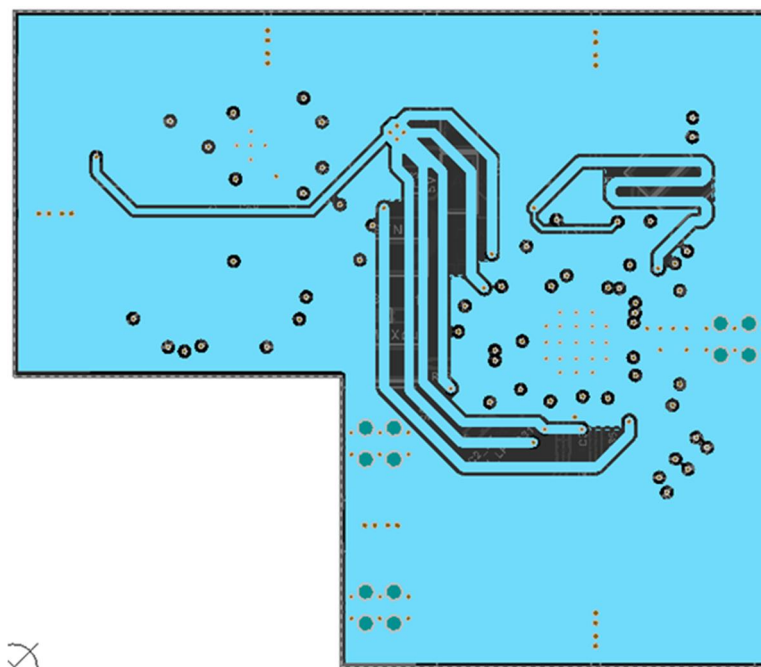


Figure 96. Mid Layer 1

Layout Examples (continued)

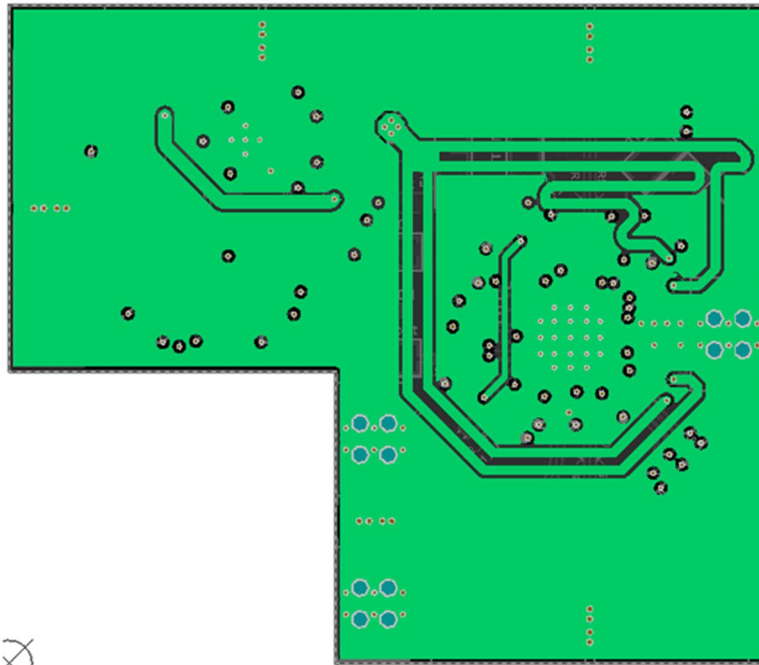


Figure 97. Mid Layer 2

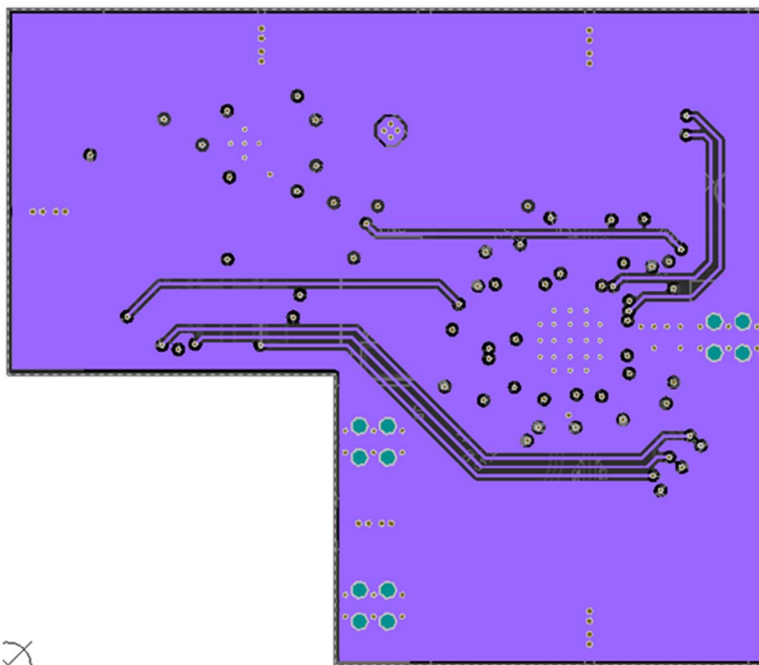


Figure 98. Mid Layer 3

Layout Examples (continued)

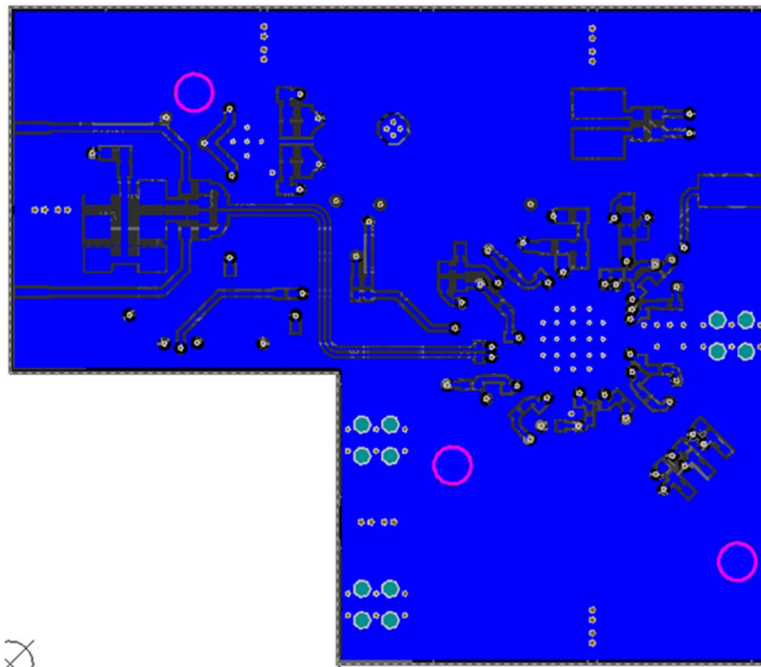


Figure 99. Bottom Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

[LMX8410LEVM User Guide](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMX8410RGZR | ACTIVE | VQFN | RGZ | 48 | 1000 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | LMX8410 | Samples |
| LMX8410RGZT | ACTIVE | VQFN | RGZ | 48 | 250 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | LMX8410 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMX8410RGZR | VQFN | RGZ | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |
| LMX8410RGZT | VQFN | RGZ | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMX8410RGZR | VQFN | RGZ | 48 | 1000 | 356.0 | 356.0 | 35.0 |
| LMX8410RGZT | VQFN | RGZ | 48 | 250 | 208.0 | 191.0 | 35.0 |

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

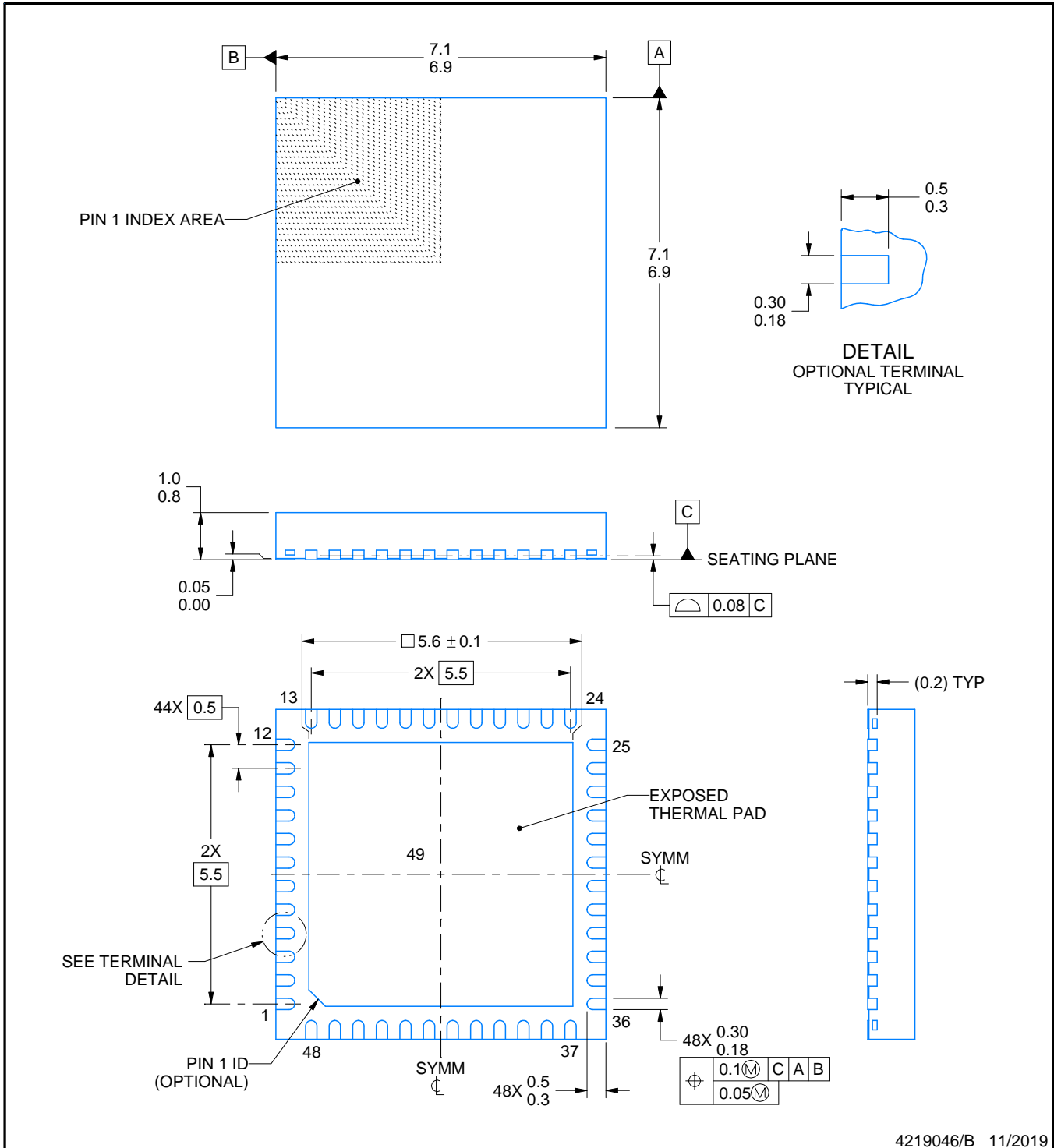
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



4219046/B 11/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

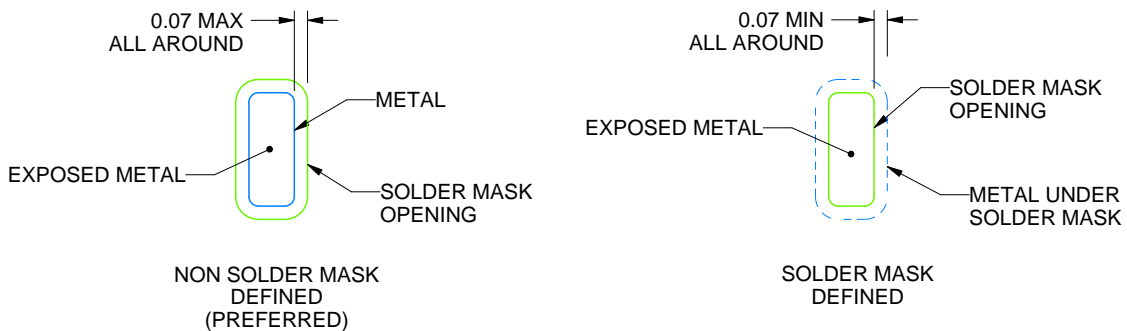
RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

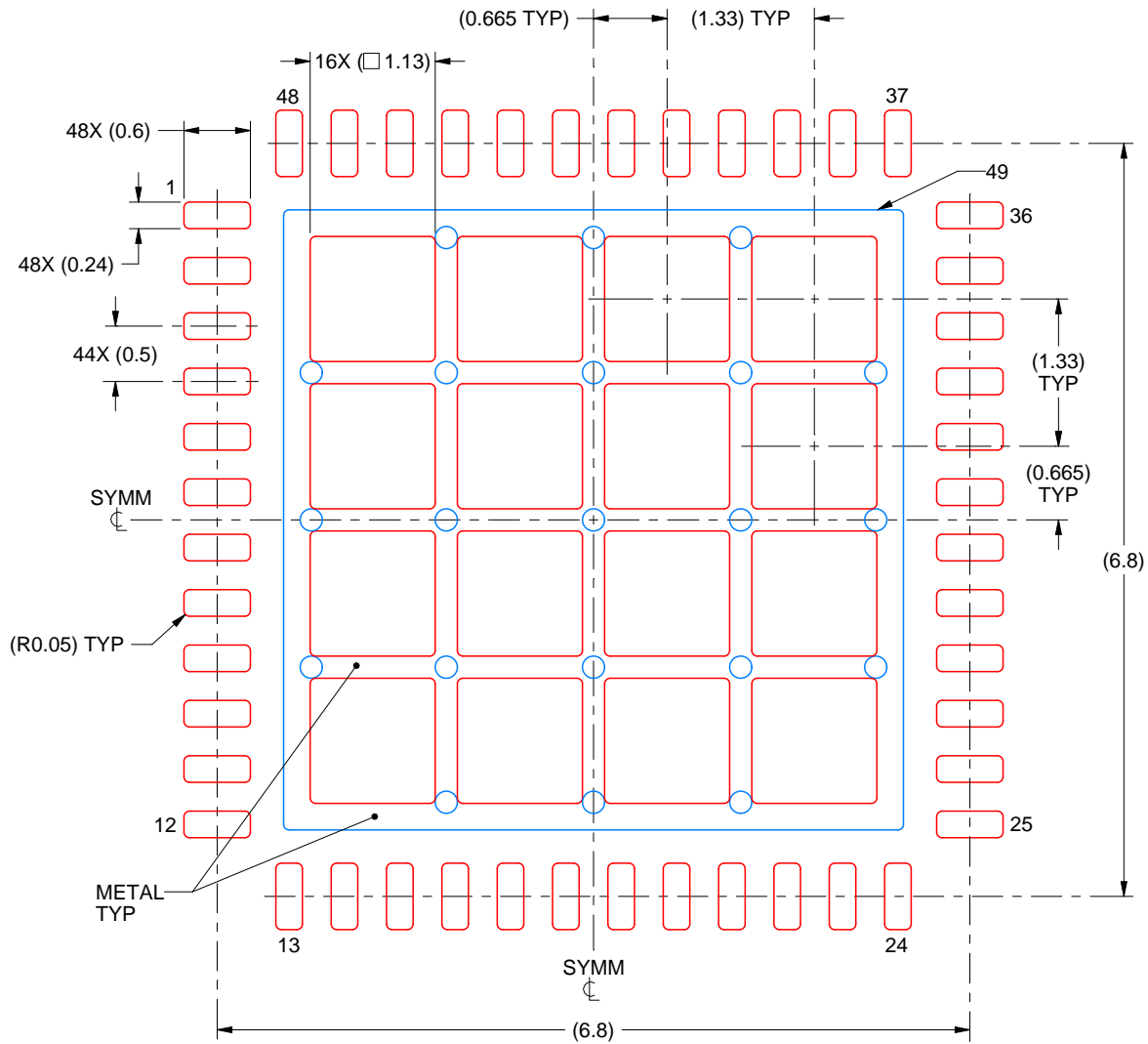
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
 66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:15X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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