73M1866B/73M1966B
MicroDAA™ with PCM Highway

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73M1x66B Daisy Chaining

Introduction

This application note provides guidance on using the 73M1x66B FXO in multi-device applications. Figure 1 shows a simple architecture for daisy chaining the devices,
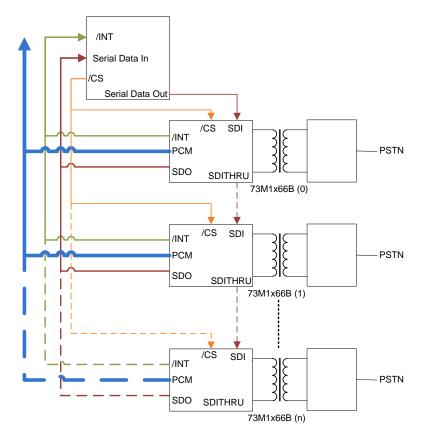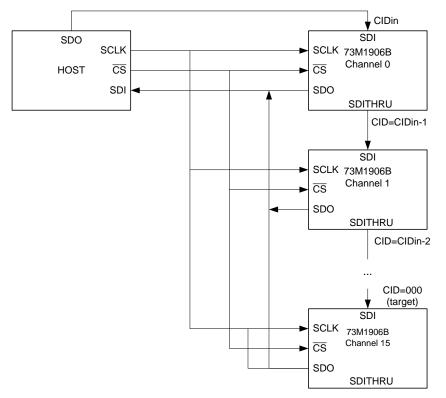

Figure 1: 73M1x66B Daisy Chain

SPI Interface

When using multiple SPI devices in a design, the user may wish to share the SPI bus between these multiple devices. To allow for the sharing of CS lines between multiple 73M1x66B devices, the 73M1x66B offers a daisy-chain mode for the SPI interface. In this mode, the CS, SCLK and SDO lines for each device are shared while the SDI is "daisy-chained" from device to device.

Figure 2 shows a daisy-chain SPI configuration.

Figure 2: Daisy-Chain SPI Configuration

The host accesses the 73M1x66B using an SPI interface to write to control registers and read status registers. The host is the master of the transaction. Four pins orchestrate the communication between the host and the SPI, and a fifth pin is dedicated to support the daisy-chain mode. The signals are as follows:

- SDI   Serial data input driven by the host.
- SDO   Serial data output driven by the 73M1x66B.
- SCLK   Clock input driven by the host.
- $\overline{CS}$ Chip select input driven by the host.
- SDITHRU   Serial data output for daisy-chain mode.

The SPI implemented by the 73M1x66B has the following key features:

- Support for 8-bit and 16-bit mode operations.
- Support for daisy-chain operations.
- Support for both continuously active SCLK or SCLK active during transfers only.
- Support for broadcast mode.

Transactions between the host and the 73M1x66B require three bytes. All bytes are transmitted most-significant byte first. The first is the control byte, the second the address byte and the third is the data byte. The control byte is structured as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCT	R/W	X	X	CID[0]	CID[1]	CID[2]	CID[3]

The value of CID[0:3] determines which 73M1x66B in the daisy chain should execute the read or write operation requested by the host. Up to 16 devices in the daisy chain can be supported. The daisy chain organization is shown in Figure 2. The control byte is submitted to the first 73M1x66B in the daisy chain. If the value of CID[0:3] is different from zero, the SPI of that device decreases the value of CID[0:3] by one and passes the new value through SDIT to the next 73M1x66B in the chain. This process continues until CID[0:3] is zero, thus stopping at the device designated to execute the operation. The value of CID will be the position in the daisy chain for the device being addressed minus one.

✔ If the host is controlling only one 73M1x66B, CID[0:3] must be set to 0.

The BRCT bit overrides the chip addressing driven by CID[0:3]. The host asserts BRCT for all write operations that must be executed by all 73M1x66B devices in the chain. At that time, whatever comes in SDI comes out through SDIT. BRCT does not affect read operations.
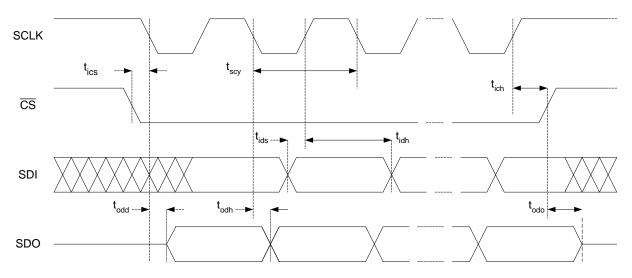
SPI Timing

Figure 3: SPI Timing Diagram

73M1x66B Single Device
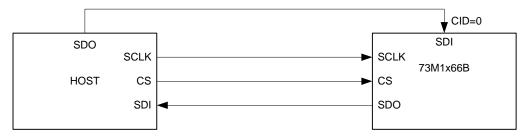
Figure 4 shows a single device SPI configuration.

Figure 4: Single Device Configuration

Table 1 represents the timing characteristics for a single 73M1x66B design.

Table 1: Single 73M1x66B SPI Interface Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time[1]	t_{scy}	62.5	–	–	ns
SCLK rise time	t_{scr}	–	–	25	ns
SCLK fall time	t_{scf}	–	–	25	ns
$\overline{CS}$ setup time	t_{ics}	25	–	–	ns
$\overline{CS}$ hold time	t_{ich}	20	–	–	ns
SDI setup time	t_{ids}	25	–	–	ns
SDI hold time	t_{idh}	20	–	–	ns
SDO turn on delay	t_{odd}	–	–	20	ns
SDO turn off delay	t_{odo}	–	–	20	ns
SDO hold time	t_{odh}	–	–	20	ns
SDI to SDITHRU propagation delay	t_{idt}	–	6	–	ns
Note 1: The minimal value of this parameter is for the case where only one 73M1906B is connected to the host. If the daisy chain mode is used, the minimum SCLK cycle time increases according to the number of slaves in the chain.					

73M1x66B Daisy-Chain

Table 2 represents the timing characteristics for a daisy-chained 73M1x66B design.

Table 2: Daisy-Chain 73M1x66B SPI Interface Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time[*]	t_{scy}	62.5+2*M*N	–	–	ns
SCLK rise time	t_{scr}	–	–	25	ns
SCLK fall time	t_{scf}	–	–	25	ns
$\overline{CS}$ setup time	t_{ics}	25	–	–	ns
$\overline{CS}$ hold time	t_{ich}	20	–	–	ns
SDI setup time	t_{ids}	25 + M*N	–	–	ns
SDI hold time	t_{idh}	20	–	–	ns
SDO turn on delay	t_{odd}	–	–	20	ns
SDO turn off delay	t_{odo}	–	–	20	ns
SDO hold time	t_{odh}	–	–	20	ns
SDI to SDITHRU propagation delay	t_{idt}	–	6	–	ns
*Assumes 50% Duty Cycle of SCLK. N= 73M1x66B devices in Daisy-Chain – 1 M = SDI to SDITHRU + Board propagation delays					

Table 3: Daisy-Chain 73M1x66B SCLK Rate Examples

Number of Devices in Daisy Chain	Minimum SCLK Cycle Time*	Max SCLK Frequency*
1	62.5	16 MHz
2	74.5	13.4 MHz
3	86.5	11.6 MHz
4	98.5	10.2 MHz
5	110.5	9.0 MHz
6	122.5	8.2 MHz
7	134.5	7.4 MHz
8	146.5	6.8 MHz
9	158.5	6.3 MHz
10	170.5	5.9 MHz
11	182.5	5.5 MHz
12	194.5	5.1 MHz
13	206.5	4.8 MHz
14	218.5	4.6 MHz
15	230.5	4.3 MHz
16	242.5	4.1 MHz
*Assumes a 50% duty cycle of SCLK and no board propagation delay.		

SDITHRU

The SDITHRU pin on the 73M1x66B device is designed to operate as an output that mimics the SDI pin's input while subtracting 1 from the CID. However, while in reset, the SDITHRU pin acts an input that will put the device into a test mode if the level of SDITHRU is low when reset is released. The SDITHRU output is designed to be internally weakly pulled high during reset but it is optional for the user to provide an additional external weak pull up to VCC (see Figure 5). A suggested value for this resistor (Rpu) is 10 KΩ.
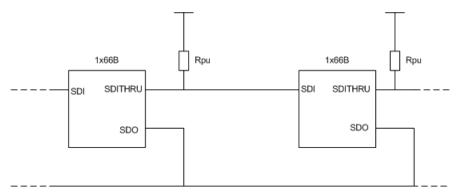
Figure 5: SDITHRU Optional Pull-up Resistor

Interrupt Strategies

The 73M1x66B can operate in interrupt polling mode, where interrupt is detected by reading the status from the device's interrupt register, For this polling mode, no hardware interrupt signal wiring is required, however, the software must perform constant reading of the interrupt status register for each device to determine if and when interrupt occurs. Alternatively, this constant polling can be eliminated using hardware interrupt signal. Depending upon design criteria, the design can trade off the required number of interrupt I/O against the interrupt response time. Several methods are available as shown in the following architectures.

Individual Interrupt Lines per Device

This method provides the fastest response by reducing the process latency. It does require a separate input per device, which can be a valuable resource.
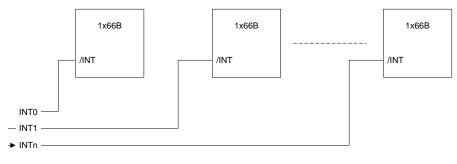
Figure 6: Individual Interrupt

Common Interrupt Line for All Devices

This method uses the least number of input lines but will have an increased latency due to querying and determining which device is making an interrupt request.
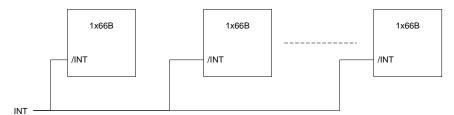

Figure 7: Common Interrupt Line

Block Shared Interrupt Line

This architecture is a combination of both the Individual and common interrupt line methods. The devices can be divided into blocks or groups of any size. Each group shares a common interrupt line while different groups have separate lines from each other.
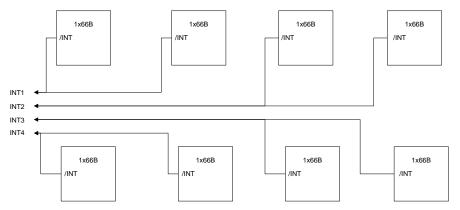

Figure 8: Block Shared Interrupt Lines

Software Consideration

The SPI transaction for accessing the 73M1x66B register consists of a 3-byte sequence:

- A control byte containing the transaction type (read/write) and the device address.
- The address byte indentifying the device's internal register.
- The actual data byte for read and write transaction.

Since all devices share the same SPI signals (SDI/SDO) it is important that each SPI transaction is executed without interruption. Software semaphore must be used to prevent fragmentation of the SPI transaction.

Revision History

Revision	Date	Description
1.0	7/31/2009	First Publication.