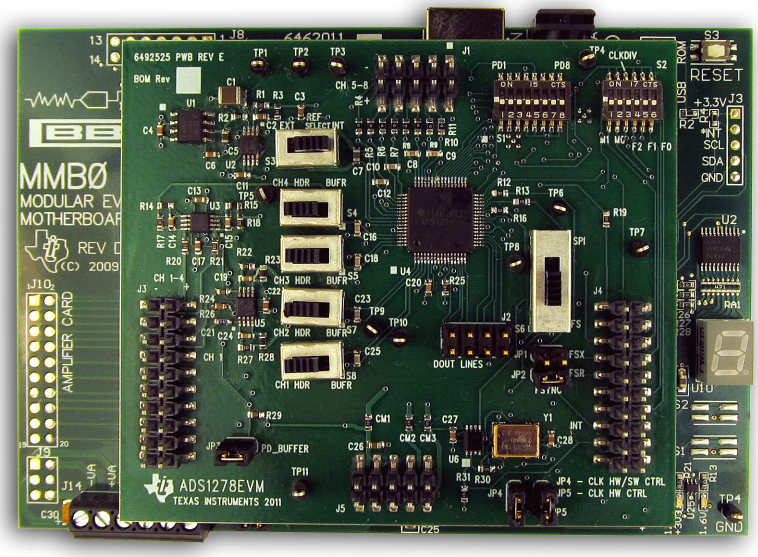
ADS1x7xEVM-PDK



ADS1x7xEVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS1x7xEVM-PDK. These evaluation module kits (EVM-PDK) are an evaluation system for the ADS1278, a 24-bit, 8 channel, delta-sigma analog-to-digital converter (ADC), the ADS1178, a 16-bit version of the ADS1278 and the ADS1274 and ADS1174, which are 4 channel versions of the ADS1278 and ADS1178, respectively. The EVM-PDK allows evaluation of all aspects of the ADS1x7x devices.

This document includes an EVM QuickStart, hardware and software details, bill of materials, and schematic.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Table 1. EVM-Compatible Device Data Sheets

Device	Literature Number	Device	Literature Number
ADS1278	SBAS367	OPA1632	SBOS286
ADS1274	SBAS367	SN74LVC2G157	SCES207
ADS1178	SBAS373	TPS73018	SBVS054
ADS1174	SBAS373	TPS65131	SLVS493
REF5025	SBOS410	PCA9535	SCPS129
OPA2350	SBOS099		

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1 EVM Overview

The ADS1x7xEVM-PDK is an evaluation module kit that includes an EVM, MMB0 motherboard and software. As a standalone PCB, the ADS1x7xEVM is useful for prototyping designs and firmware. It can be connected to any modular EVM system interface card.

1.1 Features

ADS1x7xEVM Features:

- Contains all support circuitry needed for the ADS1178/ADS1278/ADS1174/ADS1274
- Voltage reference options: external or onboard
- Clock options: External clock source (PLL or DSP supplied) or 27MHz onboard crystal oscillator
- GPIO access
- Compatible with the TI Modular EVM System

ADS1x7xEVM-PDK includes the ADS1x7xEVM board with the DSP-based MMB0 motherboard, that can be used with ADCPro™ to quickly evaluate the device.

This manual covers the operation of the ADS1x7xEVM-PDK. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1178EVM/ADS1278EVM/ADS1174EVM/ADS1274EVM. For clarity of reading, this manual will refer only to the ADS1278EVM or ADS1x7xEVM-PDK, but operation of the EVM and kit for the ADS1178/ADS1274/ASD1174 is identical, unless otherwise noted.

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2 Quick Start

This section provides a QuickStart guide to quickly begin evaluating the ADS1x7xEVM with ADCPro.

2.1 Default Jumper/Switch Configuration

Figure 1 shows the jumpers found on the EVM and the respective factory default conditions for each.

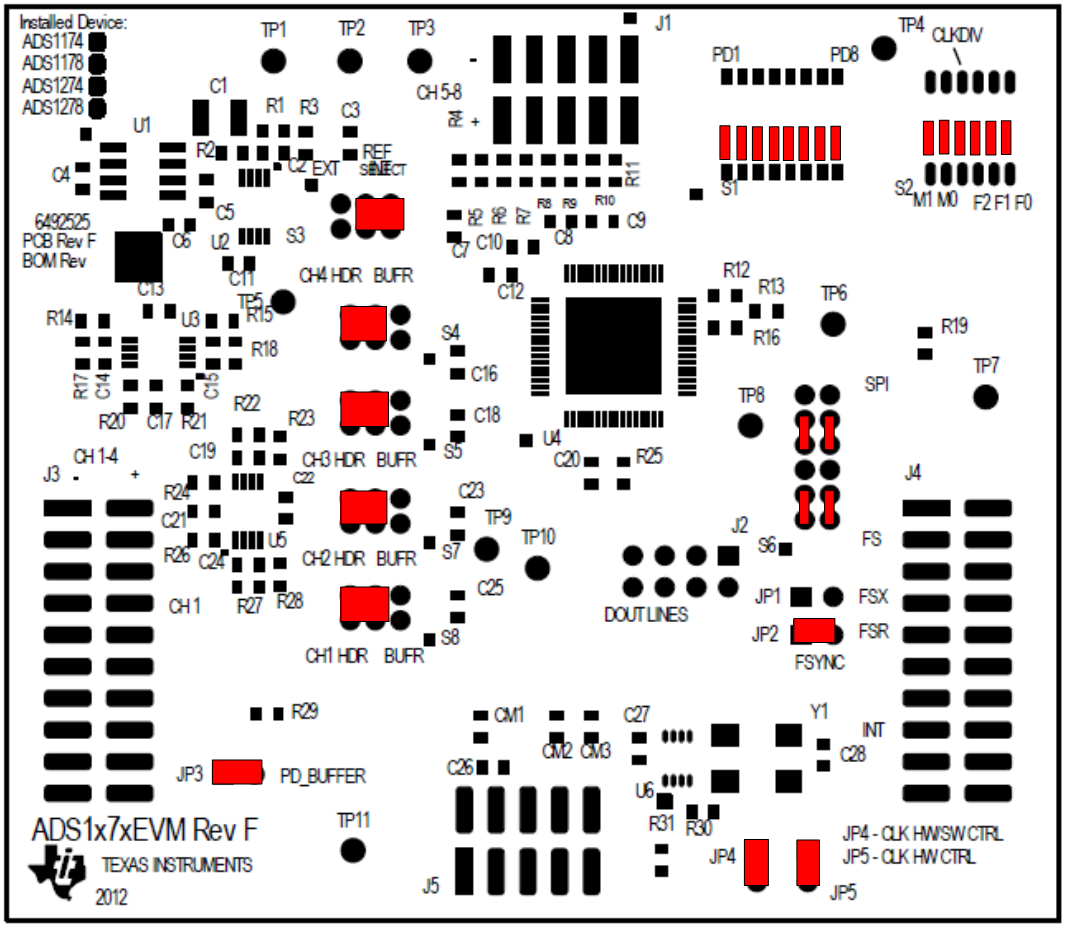

Figure 1. ADS1x7xEVM Default Jumper Locations

Table 2 lists the jumpers and switches and the factory default conditions.

Table 2. Default Jumper/Switch Configuration

Switch	Default Position	Switch Description
S1	All OFF (Down)	Power-down channel DIP switches (Hardware control)
S2	All OFF (Down)	Mode, Format, and CLKDIV DIP switches (Hardware control)
S3	INT (Right)	On-board voltage reference selected
S4	Header connected to converter (Left)	Channel 4 header connected to converter (not buffered)
S5	Header connected to converter (Left)	Channel 3 header connected to converter (not buffered)
S6	[1-2], [4-5], [7-8], [10-11]	Jumpers installed to select FS serial interface format
S7	Header connected to converter (Left)	Channel 2 header connected to converter (not buffered)

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Table 2. Default Jumper/Switch Configuration (continued)

Switch	Default Position	Switch Description
S8	Header connected to converter (Left)	Channel 1 header connected to converter (not buffered)
Jumper		
JP1	Open	FSX **NOT** connected to SYNC/$\overline{\text{DRDY}}$
JP2	Short	FSR connected to SYNC/$\overline{\text{DRDY}}$
JP3	Short	Input buffer op-amps are powered-down
JP4	Short	Clock source selection using software control
JP5	Short	External clock source selected (invalid since using software control)

2.2 ADS1x7xEVM-PDK Operation

To prepare to evaluate the ADS1278 with the ADS1x7xEVM-PDK, complete the following steps:

1. Verify the jumpers on the ADS1x7xEVM are as shown in Figure 1 (note that these settings are the factory-configured settings for the EVM).
2. Using ADCPro HW/SW Installation Manual, verify the MMB0 jumpers are in the default position and install ADCPro and ADS1278EVM plug-in software. Complete hardware connection and driver installation as part of ADCPro HW/SW Installation Manual using the below settings.
   - MMB0 J13A → Open
   - MMB0 J13B → Short
   - No additional power connections are required
3. Plug the ADS1278EVM onto the MMB0 (if not already connected). The female portion of J3, J4 and J5 on the EVM align with male connectors J10, J4, and J5 respectively on the MMB0.
4. Connect power to the MMB0 board. If power is supplied from an AC adapter (not included), ensure that it satisfies the following requirements:
   - Output voltage: 5.5 VDC to 15 VDC
   - Maximum output current: ≥ 500 mA
   - Output connector: barrel plug (positive center), 2.5-mm I.D. x 5.5-mm O.D. (9-mm insertion depth)
   - Complies with applicable regional safety standards

CAUTION

Do not misalign the pins when plugging the ADS1278EVM into the MMB0. Check the pin alignment of J3, J4, and J5 carefully before applying power to the PDK.

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3 Quick Reference

Table 3 provides a quick summary of the connections required for operation of the EVM as a standalone

Table 3. Critical Connections

Function		Header/Pin	Pin Name	Description
Interface	SCLK	J4.3	CLKX	SCLK
	DIN	J4.11	DX	Data In
	DOUT	J4.13	DR	Data Out
	Interrupt	J4.15	$\overline{\text{INT}}$	$\overline{\text{DRDY}}$/FSYNC
Power	1.8V	J5.7	+1.8VD	Digital supply
	3.3V	J5.9	+3.3VD	Digital supply
	5.0V	J5.3	+5VA	Analog supply
Analog Inputs	Channels 1-4	J3.1-8		Analog Inputs
	Channels 5-8	J1.3-10		Analog Inputs (ADS1178 and ADS1278 only)

CAUTION

When using the EVM as part of the ADS1278EVM-PDK, the DIP switches S1 and S2 must all be switched so that they are down, toward the center of the board. Failure to do so may damage the EVM.

3.1 Analog Inputs

The analog inputs for the ADS1278EVM are connected to J1 and J3. Channels 1-4 connect to J3 and provisions are provided to buffer these signals before being connected to the converter. Switches S4, S5, S7, and S8 control whether the buffered or unbuffered signal is connected to the ADS1278. Channels 5-8 connect to J1 and have an RC filter available to filter the input before connecting to the converter. Channels 5-8 do not have provisions for buffering the signal.

3.2 Digital Control

The digital control signals can be applied directly to J4 (top or bottom side).

3.3 Power Supply

The ADS1278EVM requires power rails as follows:

- 5.0V analog supply - supplied by MMB0 motherboard via J13B
- 3.3V digital supply - supplied by MMB0 motherboard
- 1.8V digital supply - supplied by MMB0 motherboard

3.4 Voltage Reference

The ADS1278EVM has two options for the reference voltage. Switch S3 selects the reference voltage from either the buffered REF5025 or a external reference voltage that is connected to the reference pins of J3 (J3.18 = REFN and J3.20 = REFP).

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4 Using the ADS1178EVM-PDK/ADS1278EVM-PDK Plug-in ADCPro

The ADS1278EVM-PDK plug-in for ADCPro provides complete control over all settings of the ADS1278. It consists of a tabbed interface (see Figure 2) with different functions available on different tabs. The tabs are:

- Channel Enable
- Settings
- About

The user can adjust the ADS1178EVM/ADS1278EVM settings when not acquiring data. During acquisition, all controls are disabled and settings may not be changed. When a setting is changed on the ADS1178EVM/ADS1278EVM plug-in, the setting immediately updates on the board.

Settings on the ADS1178EVM/ADS1278EVM correspond to settings described in the ADS1278 product data sheet product data sheet.

4.1 Top Level Controls

You can adjust the ADS1278EVM settings when you are not acquiring data. During acquisition, all controls are disabled and settings may not be changed.

The effective data rate of the ADS1278 depends upon settings of the Clock Freq and Operating Mode. The **Data Rate** indicator in the upper right corner of the plug-in interface (see Figure 2) is always visible and updates whenever a setting changes that affects the data rate.

4.2 Channel Enable Tab

The ADS1278 can acquire data from one to eight channels simultaneously. The *Channel Enable* tab (as shown in Figure 2) provides the control to power on or off each channel.

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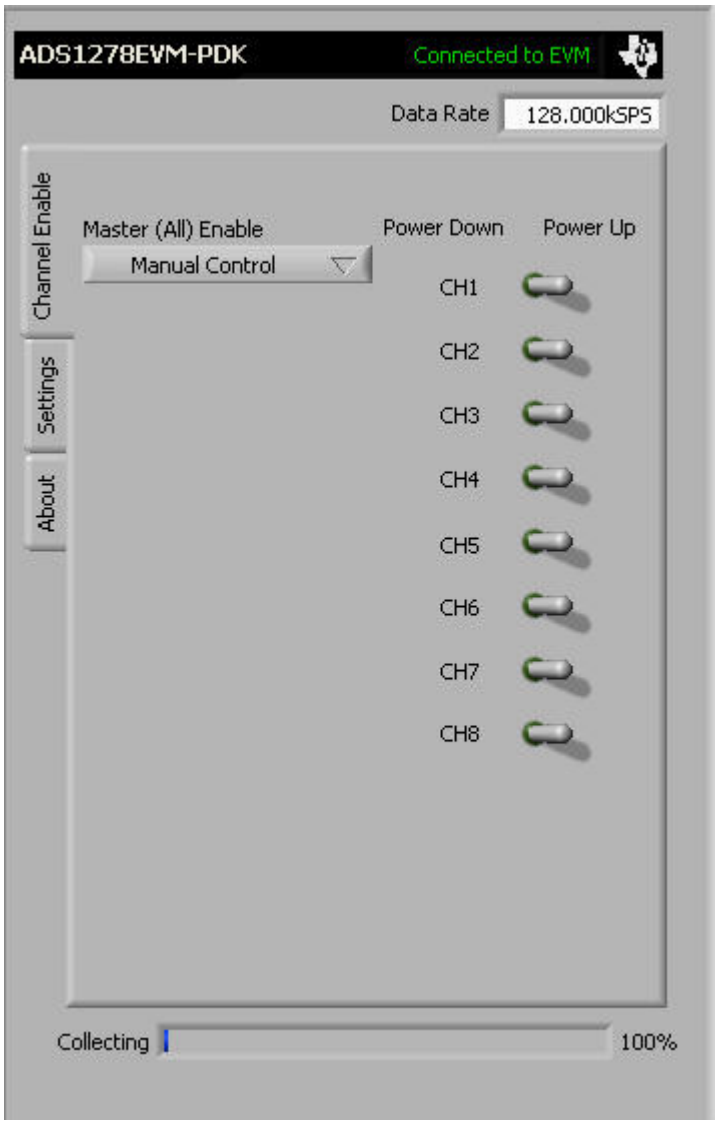

Figure 2. Channel Enable

The **Master (All) Enable** control allows for the selection of channels to convert. *Manual Control* allows channel enable control via **CH1** through **CH8** selector switches. *All Channels Enabled* and *All Channels Disabled* turn all the selector switches either ON or OFF.

4.3 Settings Tab

The **Settings** tab allows for the selection of the various clock frequencies, operating mode, data format, and other settings.

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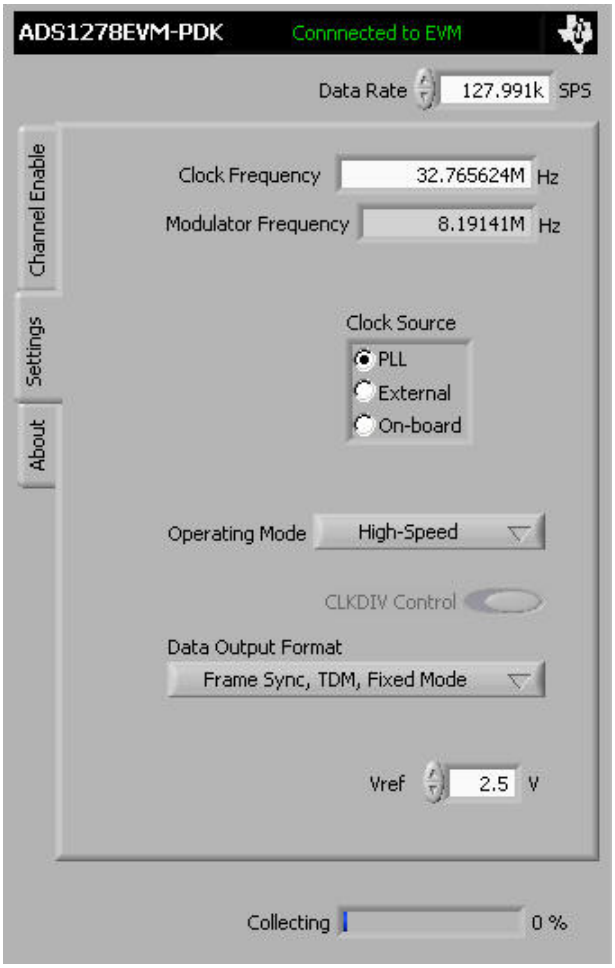

Figure 3. Clock Settings and Mode

The **Clock Source** control selects the input clock source for the ADS1278. The clock can be selected from the MMB0 *PLL*, an *External* source, or use the *On-board* oscillator.

The **Modulator Frequency** indicator shows the ADS1278 modulator frequency based on the clock source.

The **Clock Frequency** control allows the user to input the desired clock frequency when the *PLL* clock source is selected. Once the frequency is entered, the software finds the closest frequency for the PLL to synthesize (and which is within the maximum allowable frequency for the mode selected). This clock frequency is configured in the PLL and overwrites the user entered value in the **Clock Frequency** indicator.

The **Operating Mode** control allows selection of the converter operating mode: *High-Speed*, *High-Resolution*, *Low-Power*, or *Low-Speed*.

The **CLKDIV** control can be set to **0** or **1**.

The **Data Output Format** allows selection of the data output formats. For the ADS1278EVM software, the formats are limited to the *Frame-Sync, TDM Format*. The available options select whether the software collects data for all channels *Fixed Mode* or only channels that are powered up *Dynamic Mode*.

The **Vref** control allows the user to input the current Vref value being used by the data converter. This control does not change the actual reference voltage, but is required for the software to process the data correctly for display.

The maximum clock frequency is shown for the different converter options in Table 4.

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Table 4. Operating Modes: Clock Frequency

Operating Mode	CLKDIV	Frequency (MHz)
High-Speed	1	32.768
High-Resolution	1	27
Low-Power	1	27
Low-Power	0	13.5
Low-Speed	1	27
Low-Speed	0	5.4

4.4 About Tab

The **About** tab provides information on the EVM hardware and software versions.

Plug-in Version is software version of ADCPro plug-in.

Firmware Version is firmware version loaded and running on the processor.

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5 ADS1278EVM Hardware Details

The ADS1278EVM is designed to easily interface with multiple control platforms. Dual-row, header/socket combinations at J3, J4, and J5 allow connection to external circuitry for evaluation and debug.

5.1 Jumpers and Switches

Jumpers and Switches function shown in table below

Table 5. Jumper and Switch Descriptions

Jumper/Switch	Functions	Descriptions
JP1	FSYNC/$\overline{\text{DRDY}}$ Source	Short to select FSR as the source[1]
JP2	FSYNC/$\overline{\text{DRDY}}$ Source	Short to select FSX as the source[1]
JP3	Analog Input Buffers Power-down	Short - input buffers powered-down Open - input buffers powered-up
JP4	Hardware/Software Control of Clock Source	Short - Software control Open - Hardware control
JP5	Internal/External Clock Select (Hardware control)	Short - External clock source selected Open - Internal clock source selected
S1	Power down Channel 1	Hardware control for PWDN1 (set to OFF position for use with software)
	Power down Channel 2	Hardware control for PWDN2 (set to OFF position for use with software)
	Power down Channel 3	Hardware control for PWDN3 (set to OFF position for use with software)
	Power down Channel 4	Hardware control for PWDN4 (set to OFF position for use with software)
	Power down Channel 5[2]	Hardware control for PWDN5 (set to OFF position for use with software)
	Power down Channel 6[2]	Hardware control for PWDN6 (set to OFF position for use with software)
	Power down Channel 7[2]	Hardware control for PWDN7 (set to OFF position for use with software)
	Power down Channel 8[2]	Hardware control for PWDN8 (set to OFF position for use with software)
S2	GPIO2	Hardware control for GPIO2 (set to OFF position for use with software)
	GPIO3	Hardware control for GPIO3 (set to OFF position for use with software)
	GPIO4	Hardware control for GPIO4 (set to OFF position for use with software)
	CLKDIV	Hardware control for CLKDIV (set to OFF position for use with software)
	GPIO0	Hardware control for GPIO0 (set to OFF position for use with software)
	GPIO1	Hardware control for GPIO1 (set to OFF position for use with software)
S3	Converter voltage reference source selector	Selects source for reference voltage - buffered on-board reference or header (external)
S4	Channel 4 input source selector	Selects Channel 4 input source - header or input buffer Left - header Right - input buffer
S5	Channel 3 input source selector	Selects Channel 3 input source - header or input buffer Left - header Right - input buffer

(1) Only one of FSYNC/$\overline{\text{DRDY}}$ signals should be connected at a time (JP1 or JP2).
(2) Channels 4-8 only available for ADS1278 and ADS1178.

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Table 5. Jumper and Switch Descriptions (continued)

Jumper/Switch	Functions	Descriptions
S6	Serial Interface format	FS - Frame Sync format. [1-2], [4-5], [7-8], [10-11] installed. (3) SPI - SPI-compatible mode. [2-3], [5-6], [8-9], [11-12] installed.(3)
S7	Channel 2 input source selector	Selects Channel 2 input source - header or input buffer Left - header Right - input buffer
S8	Channel 1 input source selector	Selects Channel 1 input source - header or input buffer Left - header Right - input buffer

(3) Refer to Section 5.5.1 for more details.

5.2 Power-Down, MODE, and FORMAT Control

The ADS1278 has several pins to control the power-down of individual channels, and select the mode and format for the digital interface.

For users of the ADS1278EVM as a standalone module, these pins may be pulled high or low through DIP switches S1 and S2 (see Table 5). Refer to the ADS1278 product data sheet for complete details on these pins and which state sets which options.

For use in the ADS1x7xEVM-PDK, the state of these pins is controlled by software, using the I^2C port expanders (U7 and U8) on the EVM. When using the EVM with the EVM-PDK, the DIP switches S1 and S2 must all be switched down (toward the center of the board). The ADS1278EVM-PDK software checks at startup to verify that these switches are set correctly, and generates an error message for incorrect settings. The software cannot detect if the switches are changed after startup.

CAUTION

When using the ADS1x7xEVM-PDK, the DIP switches S1 and S2 must all be switched down (toward the center of the board). Failure to do so may damage the EVM.

5.3 Clock Source

The ADS1278 clock can come from one of several sources: the onboard 27MHz crystal oscillator, a clock supplied by a processor on the TOUT pin (J4.17), or an external clock source connected between J4.17 (TOUT) and J4.18 (DGND).

If the onboard 27MHz oscillator is selected, the device can be run in high-speed mode, high-resolution mode, low-power mode, or low-speed modes with CLKDIV set to 1.

If the performance of the device must be explored with CLKDIV set to 0 in the low-power and low-speed modes, an external clock must be provided to the board, either using the TOUT connection or having an external clock source connected to J4.17. The same condition is true if frequencies other than the 27MHz provided by the onboard oscillator must be investigated.

5.4 Analog Headers, J1 and J3

For maximum flexibility, the ADS1278EVM is designed for easy interfacing to multiple analog sources. These headers/socket provide access to the analog input pins of the ADS1278.

Four of the analog input sources (Channels 1–4) connect directly to J3 (top or bottom side) or through signal-conditioning modules available for the modular EVM system. These inputs have provisions to buffer the inputs using THS4521 before connecting to the converter. Switches S4, S5, S7, and S8 provide the capability to connect either the header directly or through a buffer. When the buffers are not selected, the op-amps used for buffering can be powered down by shorting JP3.

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Analog input sources (Channels 5-8) are connected directly to J1. These inputs can be filtered by installing passive components in the option filter circuitry. By default, the resistors are populated with 0-Ω resistors and the capacitors are not installed. No circuitry is provided to buffer these signals before connecting to the converter.

Table 6. J3: Primary Analog Interface Pinout

Description	Signal	Pin Number		Signal	Description
Analog Input Channel 4 Negative	AINN4	J3.1[1]	J3.2	AINP4	Analog Input Channel 4 Positive
Analog Input Channel 3 Negative	AINN3	J3.3	J3.4	AINP3	Analog Input Channel 3 Positive
Analog Input Channel 2 Negative	AINN2	J3.5	J3.6	AINP2	Analog Input Channel 2 Positive
Analog Input Channel 1 Negative	AINN1	J3.7	J3.8	AINP1	Analog Input Channel 1 Positive
Analog Ground	AGND	J3.9	J3.10	Not Connected	Not used for this design
Analog Ground	AGND	J3.11	J3.12	Analog Ground	AGND
Analog Ground	AGND	J3.13	J3.14	Not Connected	Not used for this design
Not used for this design	Not Connected	J3.15	J3.16	Not Connected	Not used for this design
Analog Ground	AGND	J3.17	J3.18	EXTREFN	External Reference negative input
Analog Ground	AGND	J3.19	J3.20	EXTREFP	External Reference positive input

(1) Pin 1 is top left-hand corner, located next to reference designator.

Table 7. J1: Secondary Analog Interface Pinout

Description	Signal	Pin Number		Signal	Description
Not used for this design	Not Connected	J1.1[1]	J1.2	Not Connected	Not used for this design
Analog Input Channel 8 Negative	AINN8	J1.3	J1.4	AINP8	Analog Input Channel 8 Positive
Analog Input Channel 7 Negative	AINN7	J1.5	J1.6	AINP7	Analog Input Channel 7 Positive
Analog Input Channel 6 Negative	AINN6	J1.7	J1.8	AINP6	Analog Input Channel 6 Positive
Analog Input Channel 5 Negative	AINN5	J1.9	J1.10	AINP5	Analog Input Channel 5 Positive

(1) Pin 1 is top right-hand corner, located next to reference designator.

5.5 Digital Interface

The digital signals are controlled via DSP interface or I^2C ICs on the EVM. Some of the digital control pins allow control via hardware or software methods. See Section 5.2 for details on these pins and their operation. The digital control signals can be applied directly to the EVM or by connecting the EVM to a DSP or micro controller interface board, such as the MMB0 if purchased as part of the ADS1278EVM-PDK, the 5-6K Interface or HPA-MCUInterface boards which are available from Texas Instruments. For a list of compatible interface and/or accessory boards for the EVM or the ADS1278, see the relevant product folder on the TI web site.

5.5.1 Digital Format Control

The ADS1278 allows the serial interface to be used in two different formats: an SPI-compatible mode and a frame-sync format. Switch S6 is populated with jumpers to select between these two formats:

- **SPI** format configures the signals as follows:

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- The SCLK input of the converter is driven by the serial port signal CLKX, pin J4.3.
- The signal from the selected source for the clock (see Section 5.3, *Clock Source*) is connected to the CLKR pin (J4.5) allowing the serial port of a processor to be synchronized to the converters master clock.
- The signal from the selected clock source is routed to the CLK input of the converter.
- Port P10 of the I2C port expander U8 is connected to a logic high level, so that the position of switch S12 can be read back by software.

• **FS** format configures the signals as follows:

- The SCLK input of the converter is driven by the serial port signal CLKR, pin J4.5.
- The signal from the selected clock source is connected to the CLKX pin (J4.3), allowing the serial port of a processor to be synchronized to the converter's master clock.
- The CLK input of the converter is driven by the CLKR signal (J4.5). This ensures that the CLK and SCLK signals have the same phase and the correct ratio as outlined in the data sheet of the device.
- Port P10 of the I^2C port expander U8 is connected to a logic low level, so that the position of S6 can be read back by software.

For use in the ADS1278EVM-PDK, the jumpers on S6 must be installed in the **FS** positions, which is the factory default setting. See Figure 1.

Switching to **SPI** format will allow users to connect the EVM to any SPI-compatible processor not supporting the frame-sync mode. If this format is selected, keep in mind that the high-speed mode will not operate at full speed (32.768MHz) because of the limitations outlined in the device product data sheet.

5.5.2 Serial Data Interface, J4

This header/socket provides access to the digital control and serial data pins of the ADC.

All logic levels on J4 are 3.3V CMOS, except for the I^2C™ pins. These pins conform to 3.3V I^2C rules. Table 8 describes the J4 serial interface pins.

Table 8. J4, Serial Interface Header

	Signal Name	Pin Number (J4)		Signal Name	Function
Synchronize channels input	$\overline{\text{SYNC}}$	1[1]	2	MODE0	Select bit 0 of converter MODE
SPI clock	SCLK	3	4	DGND	Digital ground
SCLK clock	CLKR	5	6	MODE1	Select bit 1 of converter MODE
$\overline{\text{DRDY}}$/FSYNC source 1	$\overline{\text{DRDY}}$/FSYNC	7	8	FORMAT0	Select bit 0 of FORMAT to select Frame-Sync/SPI Protocol
$\overline{\text{DRDY}}$/FSYNC source 2	$\overline{\text{DRDY}}$/FSYNC	9	10	DGND	Digital ground
ADS1278 SPI data in	DIN	11	12	FORMAT1	Select bit 1 of FORMAT to select Frame-Sync/SPI Protocol
ADS1278 data out	DOUT1[2]	13	14	FORMAT2	Select bit 2 of FORMAT to select Frame-Sync/SPI Protocol
$\overline{\text{DRDY}}$/FSYNC to DSP (interrupt)	$\overline{\text{DRDY}}$/FSYNC	15	16	SCL	I^2C clock
Can be used to provide a clock from a processor	CLK	17	18	DGND	Digital ground
Clock source select (SW mode)	CLK Select	19	20	SDA	I^2C data

(1) Pin 1 is top left-hand corner, located next to reference designator.
(2) DOUT1 buffered through a D flip-flop. See Section 5.5.3.1 below.

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Some pins on J5 have weak pull-up/down resistors. These resistors provide default settings for many of the control pins. Many pins on J5 correspond directly to ADS1278 pins. See the ADS1278 product data sheet for complete details on these pins.

5.5.3 Data Output Signals

5.5.3.1 DOUT on Digital Interface J4

In TDM mode, the data from all eight channels can be observed on the DOUT1 pin of the converter. The DOUT1 signal is used by the ADS1x7xEVM-PDK to read back and display all the channels. The digital data output pin on the digital interface header J4 is connected to DOUT1 signal via a D flip-flop. The D flip-flop provides a half cycle delay in order to align the data correctly to reach the higher speeds of the device. Otherwise, the propagation delay from the MSB in Frame Sync mode may result in missing the MSB out of the data word.

5.5.3.2 DOUTx Header, J2

All the data output signals (DOUT1 to DOUT8) can be monitored on J2. Table 9 illustrates the pinout for J2.

Table 9. J2, DOUTx Header

Data Out Line	Pin Number		Data Out Line
DOUT1	1(1)	2	DOUT2
DOUT3	3	4	DOUT4
DOUT5	5	6	DOUT6
DOUT7	7	8	DOUT8

(1) Pin 1 is top right-hand corner, located next to reference designator.

5.6 Power Supply Header, J5

J5 is the power-supply input connector. Table 10 lists the configuration details for J5. Supplies of 1.8V, 3.3V, and 5.0V are required for operation of the EVM. When using the EVM as part of the EVM-PDK, these voltages are generated by the MMB0 and no external supplies are required. For operation as a stand-alone EVM, the power supplies should be connected as shown below.

Table 10. J5 Configuration: Power-Supply Input

Function	Pin Name	Pin Number (J5)		Pin Name	Function
Not used for this design	Not used	1(1)	2	Not used	Not used for this design
+5V analog supply	+5VA	3	4	Not used	Not used for this design
Digital ground	DGND	5	6	AGND	Analog ground input
1.8V digital supply	+1.8VD	7	8	Not used	Not used for this design
3.3V digital supply	+3.3VD	9	10	N/A	Do not use

(1) Pin 1 is bottom left-hand corner, located next to reference designator.

NOTE: For monitoring the current from each supply, CM1, CM2, and CM3 (0Ω resistors) can be removed and replaced with sense resistors or ammeters.

The ADS1278 digital supplies are connected as follows:

- IOVDD supply is connected to the +1.8VD pin of the J3 header.
- DVDD supply is connected to the +3.3VD pin of the J3 header.

The ADS1278 analog supply, AVDD, is connected to the +5VA pin of the J5 header.

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6 Schematic and Bill of Materials

A complete schematic for the ADS1x7xEVM is appended to this user's guide. The bill of materials is provided in Table 11. Gerber files are available on request. Please e-mail support@ti.com or E2E Community Forums and ask for details on how to receive the files.

6.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the http://www.ti.com.)

Table 11. ADS1x7xEVM Bill of Materials

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
1	1	100u	C1	Capacitor, Ceramic, X5R, 10V	Taiyo Yuden	LMK325BJ107MM-T
2	1	150n	C2	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E154K
3	25	0.1u	C3, C11, C13, C17, C20, C21, C22, C27, C28, C29, C38, C39, C40, C41, C42, C44, C45, C46, C49, C50, C51, C54, C55, C56, C58	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E104K
4	3	1.0u	C4, C6, C43	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E105K
5	4	10u	C5 C7 C26 C57	Capacitor, Ceramic, X5R, 10V	TDK	C1608X5R1A106M
6	4(1)	2.2n	C8-10 C12	Capacitor, Ceramic, C0G, 50V	TDK	C1608COG1H222/*J
	4	2.2n	C16 C18 C23 C25			
7	8	1.5n	C14-15 C19 C24 C47-48 C52-53	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E152M
	8(1)	1.5n	C30-37			
8	3	0	CM1-3	Resistor, Chip, 1/4W	Vishay Dale	CRCW06030000Z0EAHP
9	1(1)		J1 (Top)	Header, SMT Vert. 5x2 pin, 100mil spacing	Samtec	TSM-105-01-T-DV-P
10	1		J5 (Top)	Header, SMT Vert. 5x2 pin, 100mil spacing	Samtec	TSM-105-01-T-DV-P
11	1		J5 (Bottom)	Header, SMT Vert. 5x2 pin, 100mil spacing	Samtec	SSW-105-22-F-D-VS-K
12	1		J2	Header, SMT Vert. 4x2 pin, 100mil spacing	Samtec	TSW-104-07-L-S
13	2		J3 J4	Header, SMT Vert. 10x2 pin, 100mil spacing	Samtec	TSM-110-01-T-DV-P
14	2		J3 J4 (Bottom)	Header, SMT Vert. 10x2 pin, 100mil spacing	Samtec	SSW-110-22-F-D-VS-K
15	5		JP1-JP5	Header, Male 2-pin, 100mil spacing	Samtec	TSW-102-07-L-S
16	1	2k	R1	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ202
17	18	1k	R2 R17-18 R20-22 R24 R26-27 R38-40 R42-43 R45-48	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ102
18	6	47	R3 R12-13 R16 R25 R41	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ470
19	8(1)	0	R4-11	Resistor, Chip, 1/10W	Rohm	MCR03EZPJ000
20	8	49.9	R14-15 R23 R28 R36-37 R49-50	Resistor, Chip, 1/10W, 1%	Rohm	MCR03EZPJ49R9
21	3	100k	R19 R29 R44	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ104
22	2	470k	R30-31	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ474
23	2	100k	R32-33	Resistor Pack, 8x	Panasonic	EXB-2HV104JV
24	1	10k	R34	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ103
25	1	4.3k	R35	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZP432
26	2	47k	R51-52	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ473
27	1		S1	Switch, SMD Low Profile 08 Position	CTS	218-8LPST

(1) These parts are not installed for ADS1274 and ADS1174

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Table 11. ADS1x7xEVM Bill of Materials (continued)

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
28	1		S2	Switch, 6 POS, SPST, Low Profile, SMT, 0.50 centers	CTS	218-8LPST
29	5		S3-5 S7-8	Switch, Slide DPDT, Low Profile	TE Connectivity	SSB22
30	1		S6	CONN HEADER 12POS DUAL 2MM T/H	Samtec	TMM-106-01-T-D
31	4		TP1 TP4 TP7 TP11	Test Point, Black, Thru Hole Color Keyed	Keystone	5001
32	2		TP6 TP8	Test Point, White, Thru Hole Color Keyed	Keystone	5002
33	5		TP2 TP3 TP5 TP9 TP10	Test Point, Red, Thru Hole Color Keyed	Keystone	5000
34	1		U1	IC, Precision Voltage Reference, 2.5V	TI	REF5025AID
35	1		U2	IC, Op Amp, High-Speed, Single-Supply, R-R	TI	OPA2350DGK
36	4		U3 U5 U9 U11	IC, Negative R-R Input, R-R Output, Fully Differntial Amplifier	TI	THS4521DGK
37	1[(2)]		U4	IC, Quad/Octal, Simultaneous Sampling, 24-Bit A-D Converter	TI	ADS1278PAP
38	1		U6	Single 2 line To 1Line Data Selector/Multiplexer	TI	SN74LVC2G157DCT
39	1		U10	IC, Single Inverter	TI	SN74LVC1G04DBV
40	1		U12	IC, single Positive-Edge-Triggered D-Type Flip-Flop With Clear And Reset	TI	SN74LVC2G74DCU
41	1		U13	IC, Configurable Multiple-Function Gate	TI	SN74LVC1G97DCK
42	1		U14	IC, 256K CMOS Serial EEPROM	Microchip	24AA256-I/ST
43	2		U7-8	IC, Low Voltage 16-BIT I2C and SMBus Low-Power I/O Expander With Interrupt Output and Configuration Registers	TI	TCA9535RTW
44	1		Y1	Clock Oscillator, 27MHz	CTS	CB3LV-3I-27M0000
45	1			PCB, 3.31 In x 2.88 In x 0.062 In	Any	6492525
46	4			Shunt, 100-mil, Black	3M	929950-00
47	4			SHUNT JUMPER	Samtec	2SN-BK-G

(2) Installed for ADS1278EVM-PDK. For other EVM-PDKs, the appropriate device will be installed.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2012) to A Revision	Page
• Changed step 4 of *Section 2.2*	5

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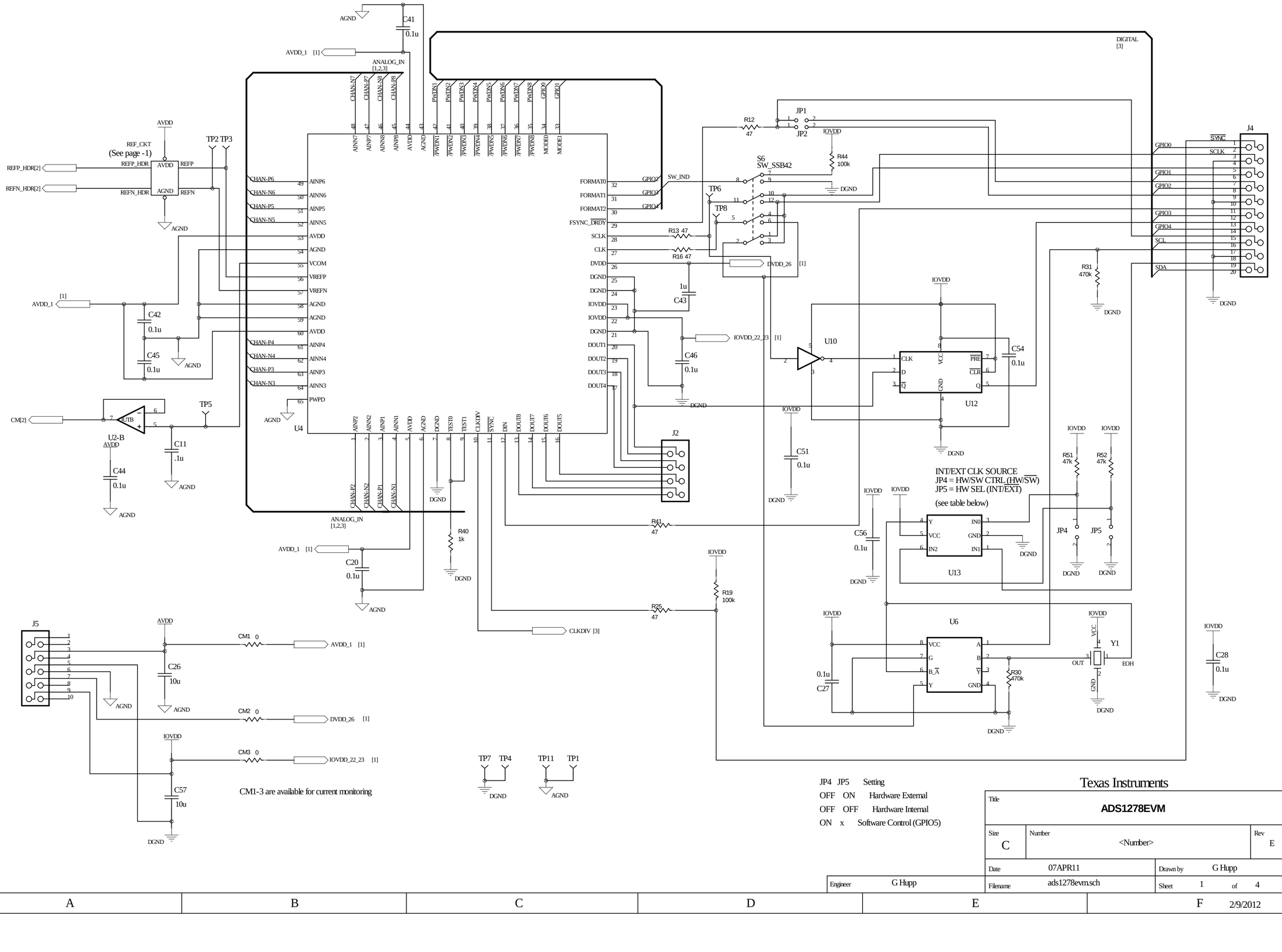

Texas Instruments

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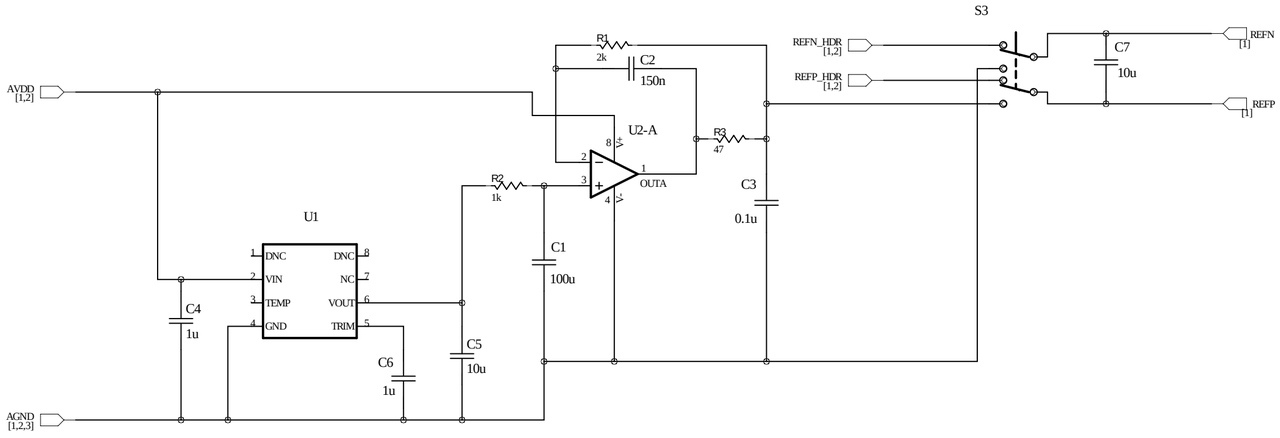
Engineer G Hupp	Filename ads1278evm.sch	Sheet 1 of 4	

2/9/2012



Texas Instruments

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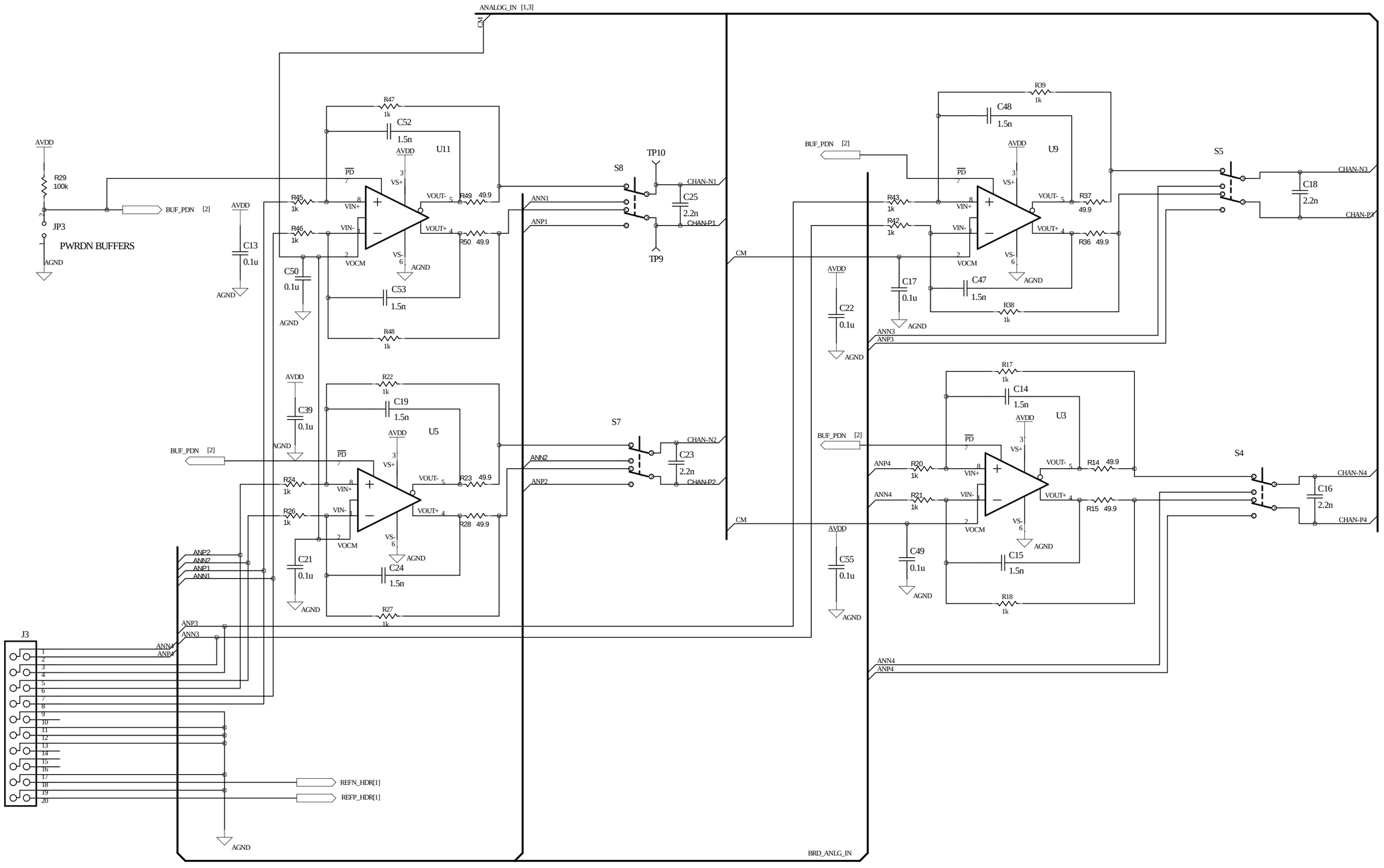
Engineer G Hupp	Filename ads1278evm.sch	Sheet -1 of 4	

2/9/2012



Texas Instruments

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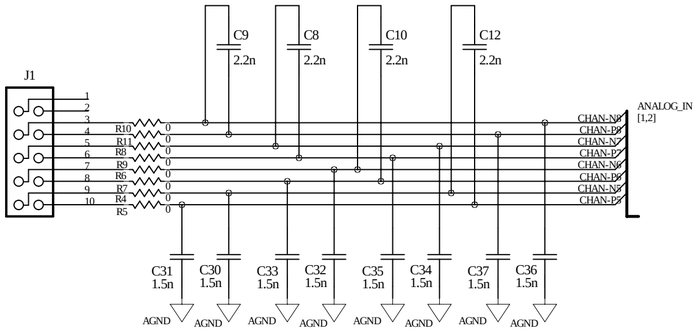
Size C	Number <Number>		Rev E
Date 07APR11		Drawn by G Hupp	
Engineer G Hupp	Filename ads1278evm.sch	Sheet 2 of 4	

2/9/2012

Channels 5-8 Analog Connections



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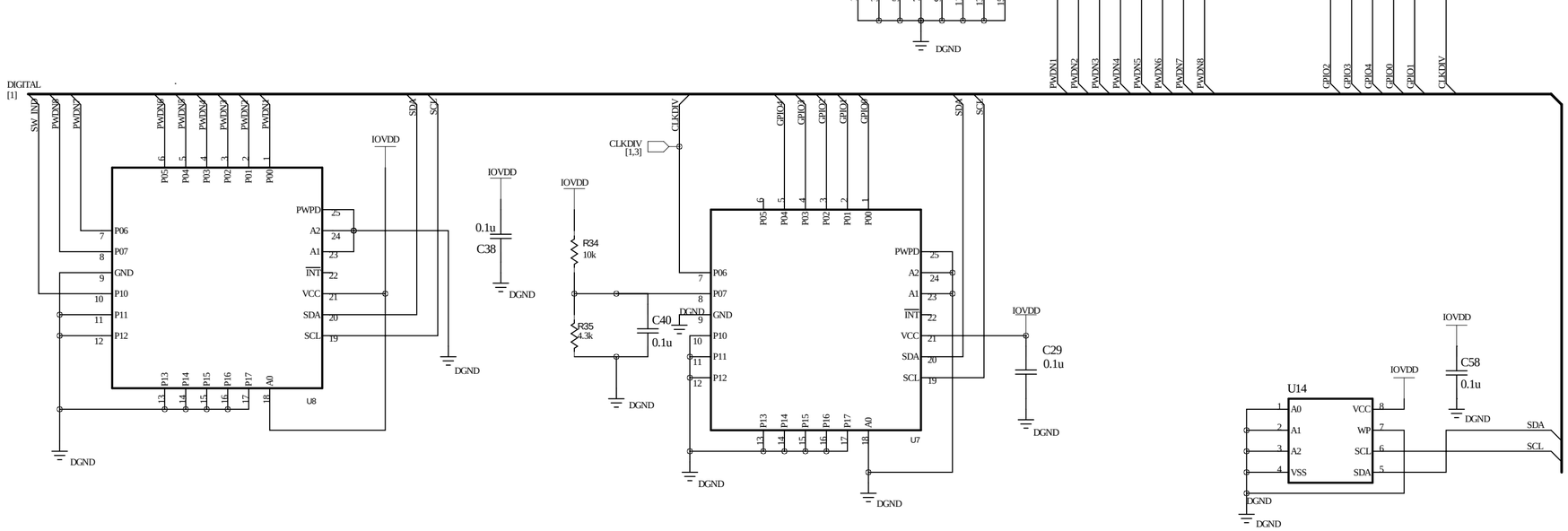

Texas Instruments

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Size: C	Number: <Number>	Rev: E
Date: 07APR11		Drawn by: G Hupp
Engineer: G Hupp	Filename: ads1278evm.sch	Sheet: 3 of 4

2/9/2012

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

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