V_{DSS} = ± 60 V, $I_{D(DC)}$ = ± 6 A
3-phase Motor Drive Inverter

SMA5135

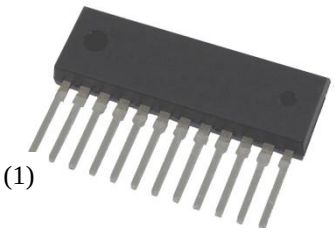
Features

- $V_{(BR)DSS}$ ----------± 60 V (I_D = 100 µA)
- I_D ----------± 6A
- $R_{DS(ON)}$ ----------0.22 Ω max.

- Built-in three half bridge circuit configured by P-channel MOSFET and N-channel MOSFET
- Low On Resistance
- ESD protection Zener with each Gate
- Compliant with RoHS directive

Package

SIP12 (SMA-12)

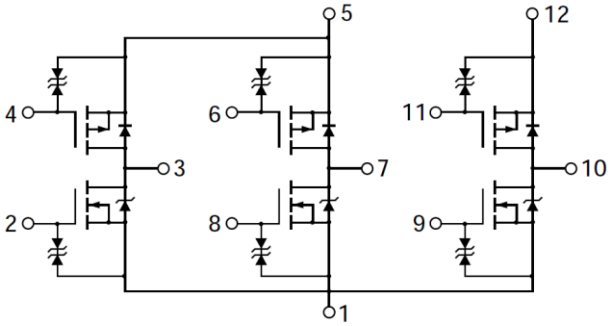


Not to scale

Applications

- 3-phase DC Motor Driver

Equivalent circuit



Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C

Characteristic	Symbol	Test conditions	Rating		Unit
			N-channel MOSFET	P-channel MOSFET	
Drain to Source Voltage	V_{DSS}		60	−60	V
Gate to Source Voltage	V_{GSS}		±20	±20	V
Continuous Drain Current	$I_{D(DC)}$		6	−6	A
Pulsed Drain Current	$I_{D(PULSE)}$	PW ≤ 1 ms Duty cycle ≤25 %	10	−10	A
Maximum Allowable Power Dissipation	P_T	No.Fin Ta=25°C All Element Operation	4		W
		Tc=25°C All Element Operation	29		
Thermal Resistance	θ_{j-a}	Junction-to-Ambient All Element Operation	31.25		°C/W
	θ_{j-c}	Junction-to-Case All Element Operation	4.31		°C/W
Channel Temperature	T_{ch}		150		°C
Storage Temperature	T_{stg}		−40 to 150		°C

Electrical Characteristics

Unless otherwise specified, T_A = 25 °C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
N-channel MOSFET						
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	60	−	−	V
Drain to Source Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	−	−	100	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V	−	−	± 10	µA
Gate Threshold Voltage	V_{TH}	V_{DS} = 10 V, I_D = 250 µA	1.0	−	2.0	V
Forward Transconductance	$Re(y_{fs})$	V_{DS} = 10 V, I_D = 3 A	−	5.5	−	S
Static Drain to Source On-State	$R_{DS(ON)}$	I_D = 3 A, V_{GS} = 4 V	−	−	0.22	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V V_{GS} = 0 V f = 1 MHz	−	320	−	pF
Output Capacitance	C_{oss}		−	160	−	
Reverse Transfer Capacitance	C_{rss}		−	35	−	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} ≒ 20 V I_D = 3 A V_{GS} = 5 V, R_L = 6.67 Ω	−	16	−	ns
Rise Time	t_r		−	65	−	
Turn-Off Delay Time	$t_{d(off)}$		−	70	−	
Fall Time	t_f		−	45	−	
Source to Drain Diode Forward Voltage	V_{SD}	I_S = 6A, V_{GS} = 0 V	−	1.2	−	V
Source to Drain Diode Reverse Recovery Time	t_{rr}	I_{SD} = 3 A, V_{GS} = 0 V di/dt = 100 A/µs	−	65	−	ns
P-channel MOSFET						
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = − 100 µA, V_{GS} = 0 V	− 60	−	−	V
Drain to Source Leakage Current	I_{DSS}	V_{DS} = − 60 V, V_{GS} = 0 V	−	−	− 100	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V	−	−	± 10	µA
Gate Threshold Voltage	V_{TH}	V_{DS} = − 10 V, I_D = − 250 µA	− 1.0	−	− 2.0	V
Forward Transconductance	$Re(y_{fs})$	V_{DS} = − 10 V, I_D = − 3 A	−	6.0	−	S
Static Drain to Source On-State	$R_{DS(ON)}$	I_D = − 3 A, V_{GS} = − 10 V	−	−	0.22	Ω
Input Capacitance	C_{iss}	V_{DS} = − 10 V V_{GS} = 0 V f = 1 MHz	−	790	−	pF
Output Capacitance	C_{oss}		−	310	−	
Reverse Transfer Capacitance	C_{rss}		−	90	−	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} ≒ − 20 V I_D = − 3 A V_{GS} = − 5 V, R_L = 6.67 Ω	−	40	−	ns
Rise Time	t_r		−	110	−	
Turn-Off Delay Time	$t_{d(off)}$		−	160	−	
Fall Time	t_f		−	80	−	
Source to Drain Diode Forward Voltage	V_{SD}	I_S = − 6A, V_{GS} = 0 V	−	− 1.1	−	V
Source to Drain Diode Reverse Recovery Time	t_{rr}	I_{SD} = − 3 A, V_{GS} = 0 V di/dt = 100 A/µs	−	85	−	ns

Typical Characteristics

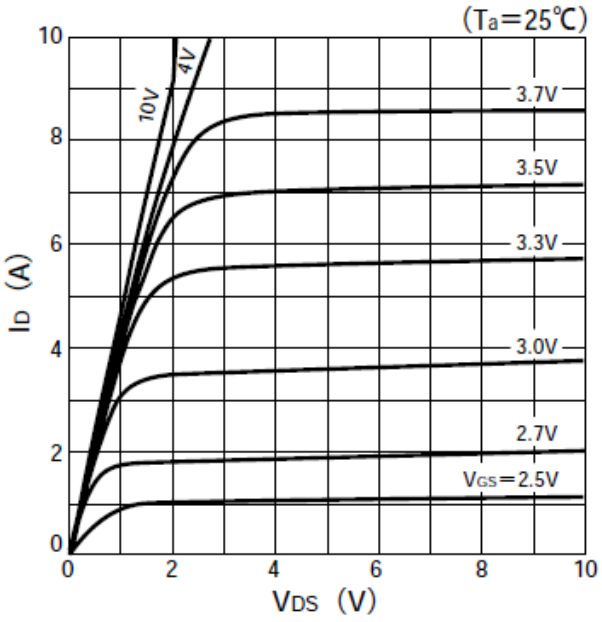


Figure 1 I_D vs. V_{DS} Characteristics (N-channel)

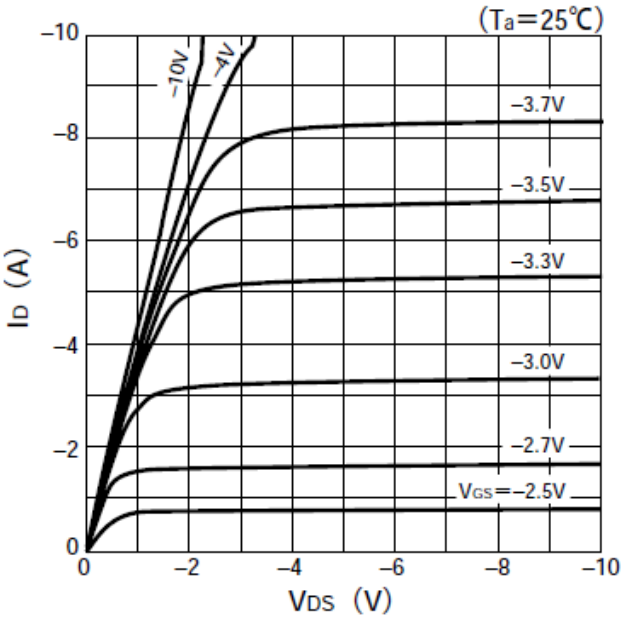


Figure 2 I_D vs. V_{DS} Characteristics (P-channel)

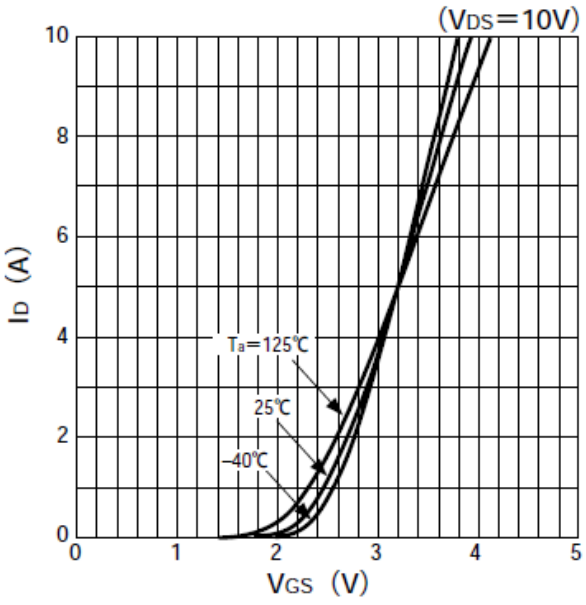


Figure 3 I_D vs. V_{GS} Characteristics (N-channel)

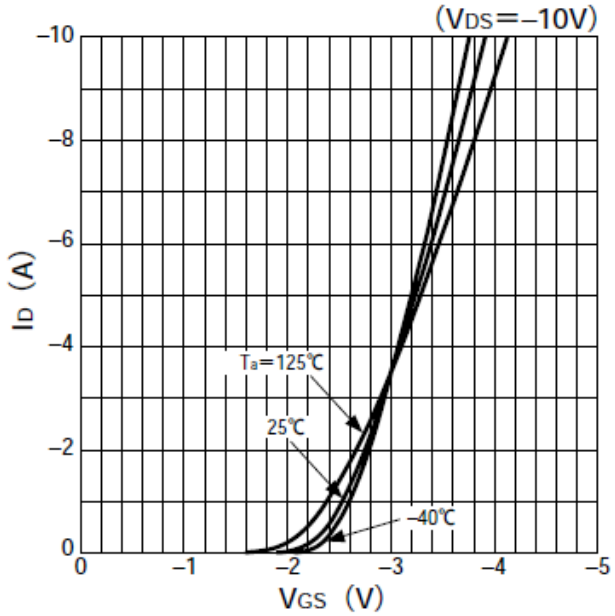


Figure 4 I_D vs. V_{GS} Characteristics (P-channel)

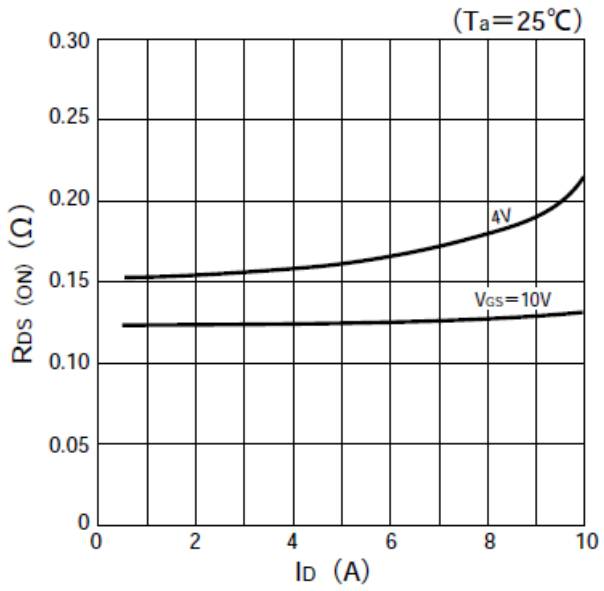


Figure 5 $R_{DS(ON)}$ vs. I_D Characteristics (N-channel)

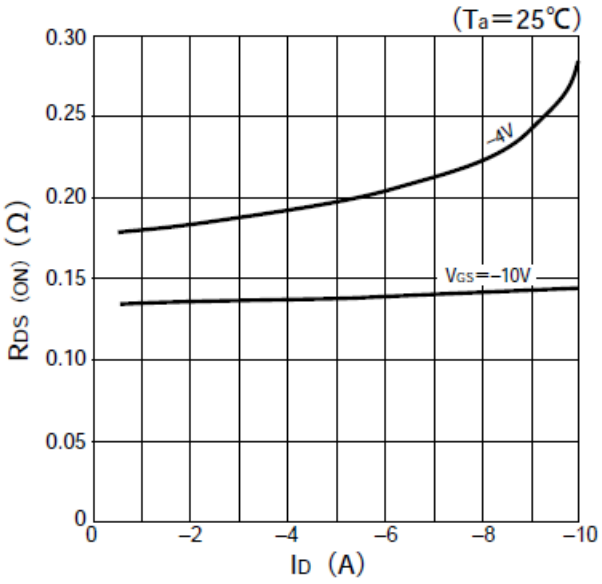


Figure 6 $R_{DS(ON)}$ vs. I_D Characteristics (P-channel)

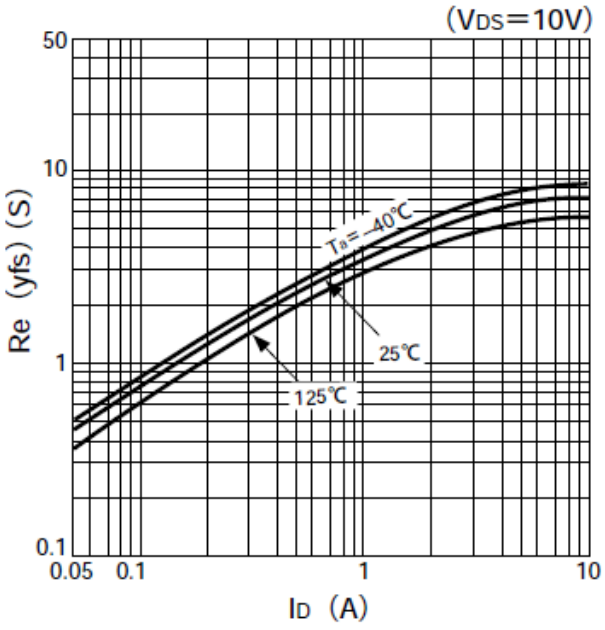


Figure 7 $R_{e(yfs)}$ vs. I_D Characteristics (N-channel)

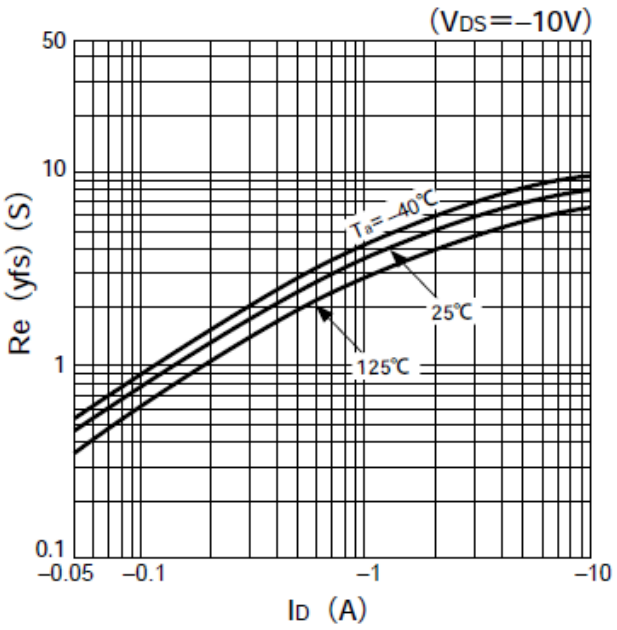


Figure 8 $R_{e(yfs)}$ vs. I_D Characteristics (P-channel)

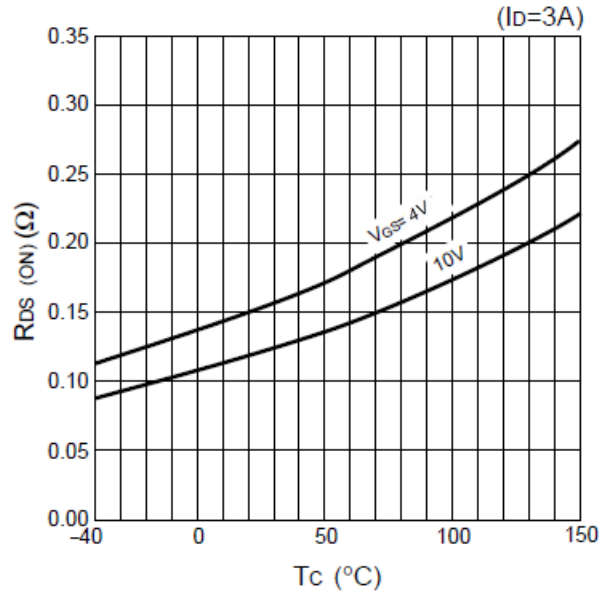


Figure 9 $R_{DS(ON)}$ vs. I_D Characteristics (N-channel)

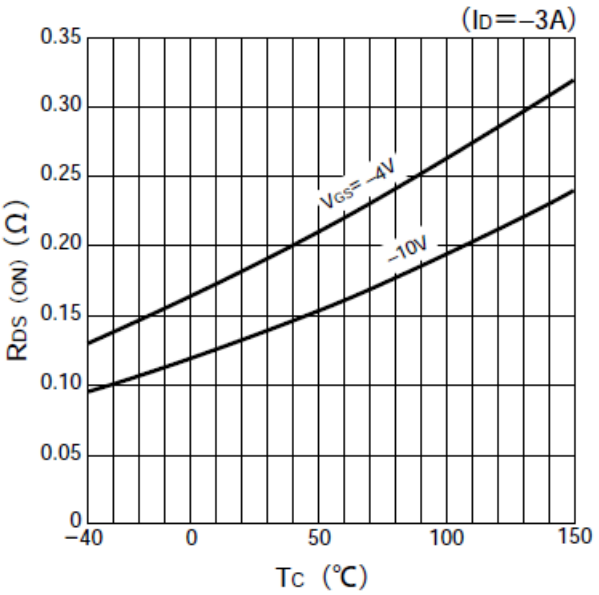


Figure 10 $R_{DS(ON)}$ vs. I_D Characteristics (P-channel)

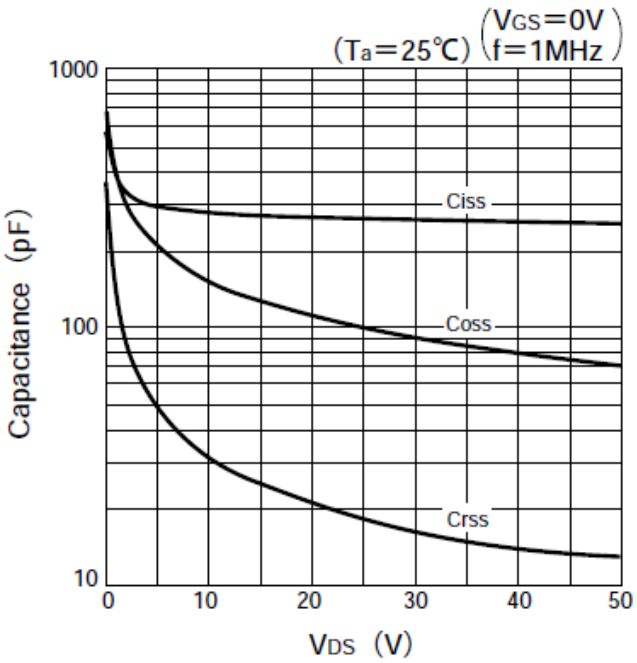


Figure 11 Capacitance vs. V_{DS} Characteristics (N-channel)

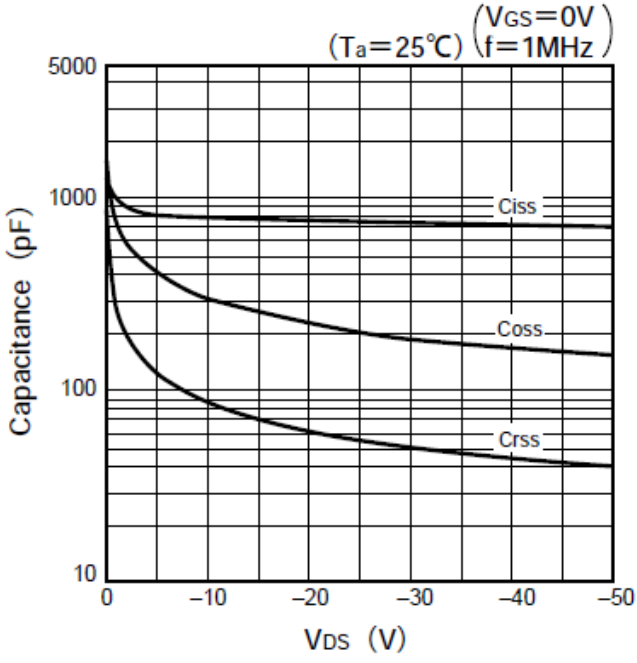


Figure 12 Capacitance vs. V_{DS} Characteristics (P-channel)

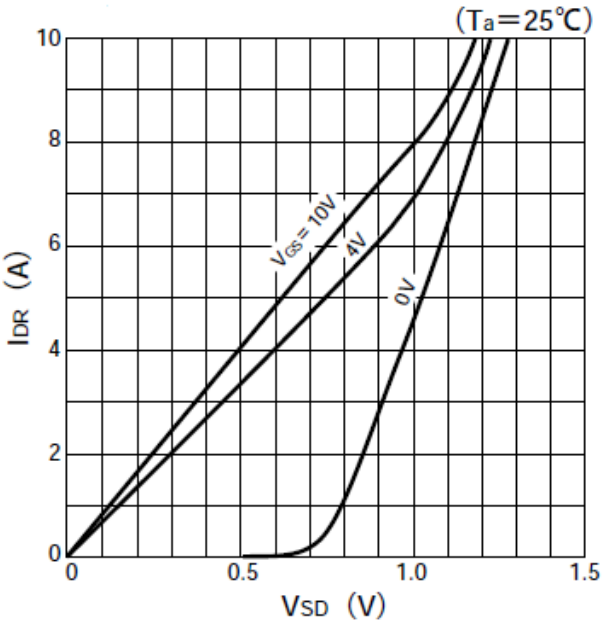


Figure 13 I_{DR} vs. V_{SD} Characteristics (N-channel)

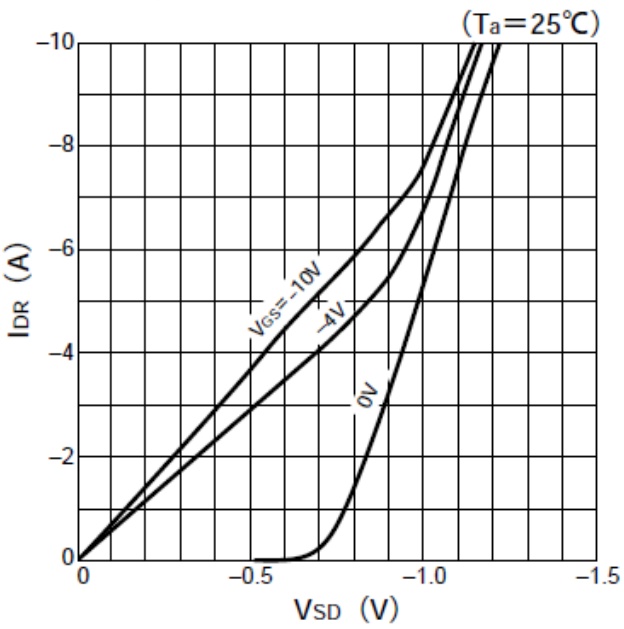


Figure 14 I_{DR} vs. V_{SD} Characteristics (P-channel)

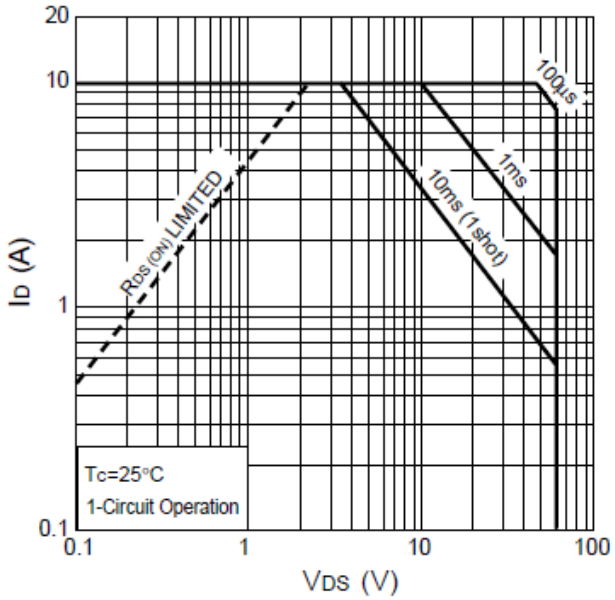


Figure 15 Safe Operating Area (N-channel)

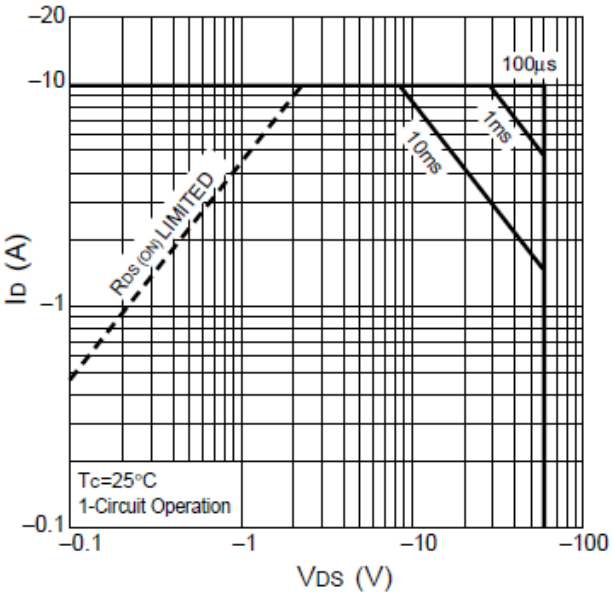


Figure 16 Safe Operating Area (P-channel)

Derating Curve

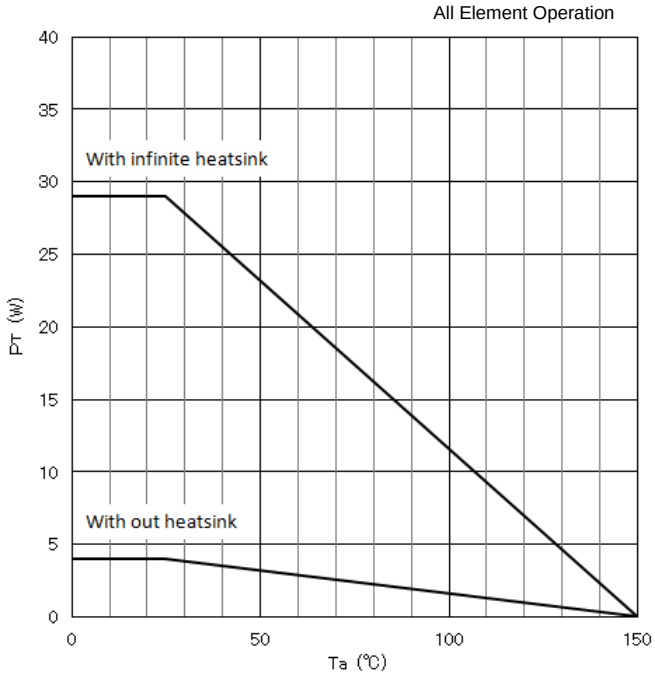
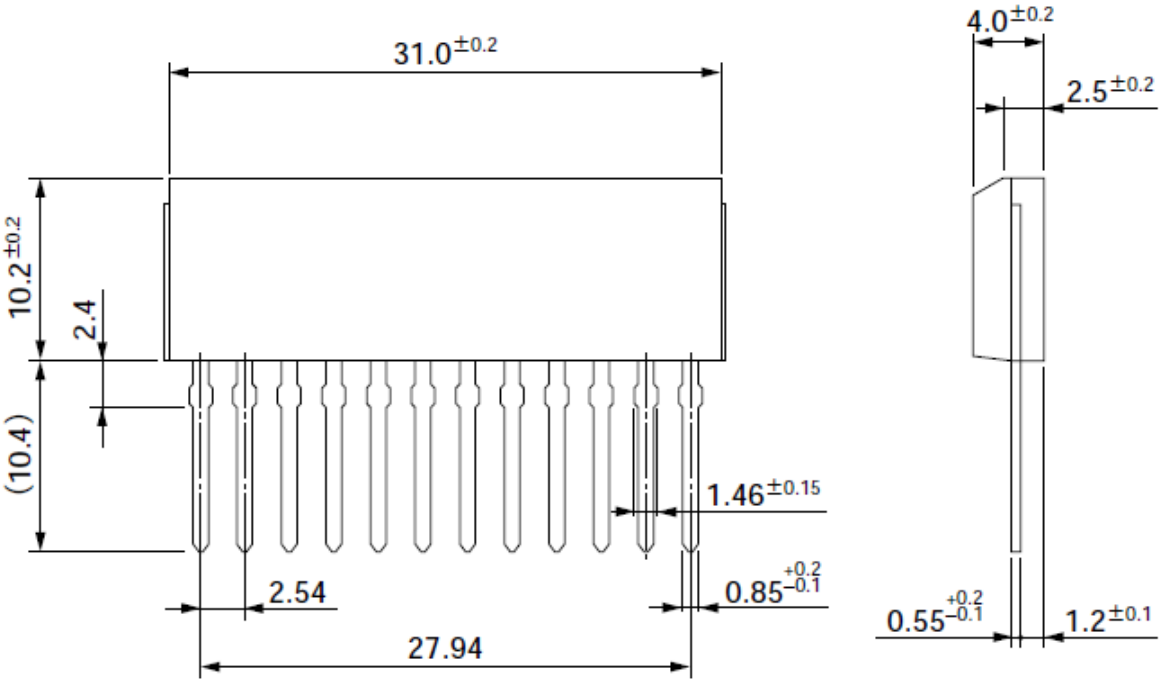


Figure 17 P_T vs. T_A Derating Curve

Package Outline

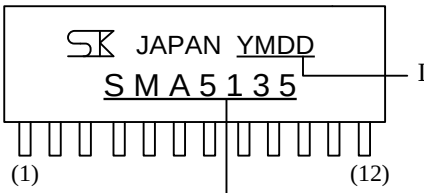
● SIP12(SMA-12)



NOTES:

● Dimension is in millimeters.
● Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Marking Diagram



Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N or D)
DD is the day of the month (01 to 31)

Part Number

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