TPS7H2211-SP Radiation-Hardness-Assured (RHA) 14-V, 3.5-A eFuse

1 Features

- Total ionizing dose (TID) characterized to 100 krad(Si)
  - Radiation hardness assurance availability of 100 krad(Si)
- Single-event effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune to linear energy transfer (LET) = 75 MeV-cm^2/mg*
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized to LET = 75 MeV-cm^2/mg*
- Integrated single channel eFuse
- Input voltage range: 4.5 V to 14 V
- Low on-resistance (R_{ON}) of 60-mΩ maximum at 25°C and VIN = 12 V
- 3.5-A maximum continuous switch current
- Low control input threshold aids in use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V logic
- Configurable rise time (soft start)
- Reverse current protection (RCP)
- Overvoltage protection (OVP)
- Internal current limit (fast-trip)
- Thermal shutdown
- Ceramic package with thermal pad
- Available in military (–55°C to 125°C) temperature range

*See TPS7H2211-SP SEE radiation report for test conditions and full information

2 Applications

- Satellite electrical power system (EPS)
- Cold sparing power supplies (redundancy)
- Power supply sequencing
- Command and data handling
- Communications payload
- Radiation hardened and tolerant power tree

3 Description

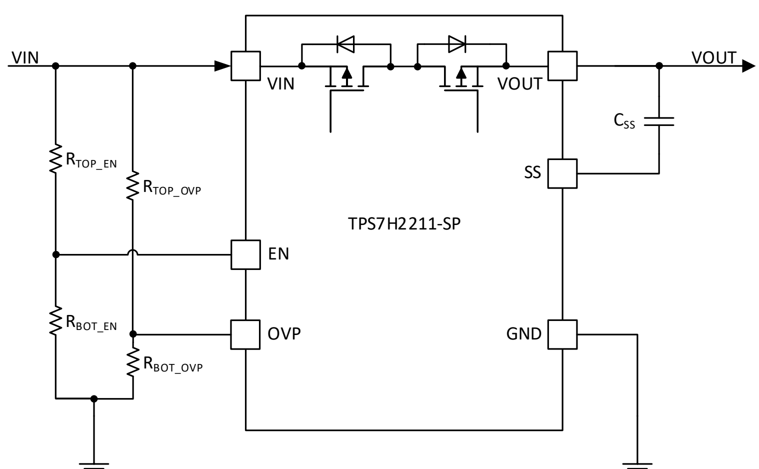
The TPS7H2211-SP is a single channel eFuse (integrated FET load switch with additional features) that provides reverse current protection, overvoltage protection, and a configurable rise time to minimize inrush current (soft start). The device contains P-channel MOSFETs that operate over an input voltage range of 4.5 V to 14 V and supports a maximum continuous current of 3.5 A.

The switch is controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. Overvoltage protection and soft start are programmable with few external components through the OVP and SS pins. The TPS7H2211-SP is available in a ceramic package with an exposed thermal pad allowing for improved thermal performance.

Device Information

ORDERABLE PART NUMBER(1)	GRADE(2)	PACKAGE
5962R1822001VXC	Flight grade QMLV-RHA 100 krad(Si)	16-pin CFP 11.00 × 9.60 mm Mass = 1.56 g(4)
5962-1822001VXC	Flight grade QMLV	
TPS7H2211HKR/EM	Engineering sample(3)	
5962R1822001V9A	Flight grade QMLV-RHA KGD	Known good die 3.66 × 5.75 mm
TPS7H2211Y/EM	Engineering sample(3)	
TPS7H2211EVM-CVAL	Evaluation module	Evaluation board

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.
(4) Mass is accurate to ±10%.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2021) to Revision B (May 2022) **Page**

- Released die versions of the device (5962R1822001V9A and TPS7H2211Y/EM)....1

Changes from Revision * (August 2021) to Revision A (November 2021) **Page**

- Released 5962R1822001VXC device....1
- Changed the device classification from "load switch" to "eFuse" and updated associated verbiage throughout the document....1
- Added additional information about the NC pins and added a default recommendation....3

5 Related Products

DEVICE	VIN RANGE	MAXIMUM OUTPUT CURRENT	PROGRAMMABLE CURRENT LIMIT	CURRENT SENSE
TPS7H2211-SP	4.5 V to 14 V	3.5 A	No	No
TPS7H2201-SP	1.5 V to 7 V	6 A	Yes	Yes

6 Pin Configuration and Functions

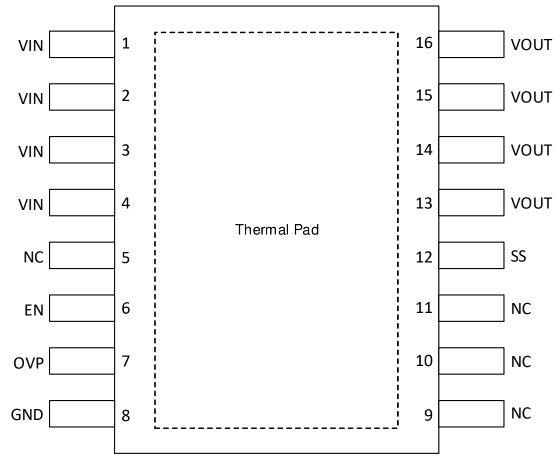


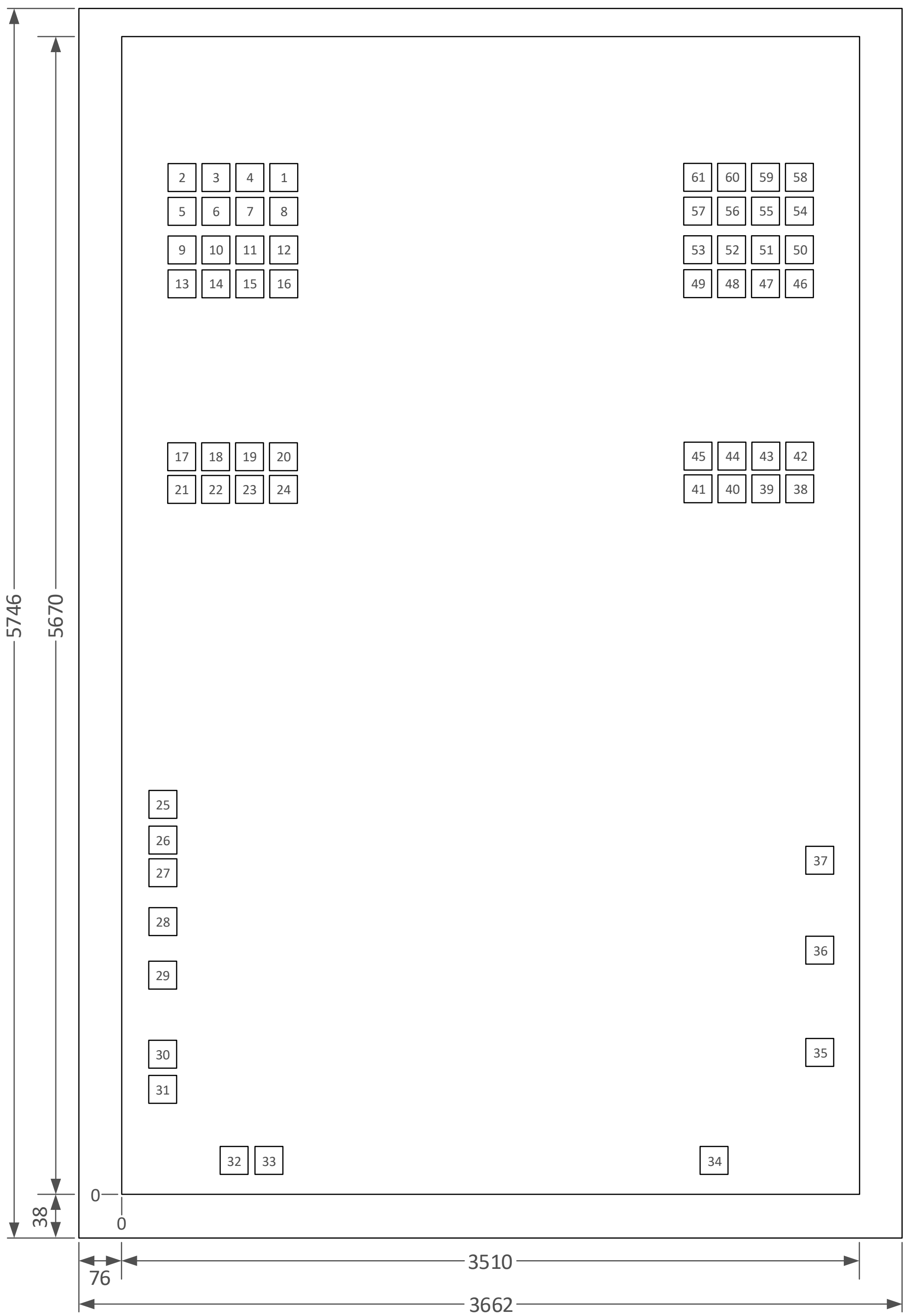
**Figure 6-1. HKR Package
16-Pin CFP With Thermal Pad
(Top View)**

Table 6-1. Pin Functions

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">I/O</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>NO.</th><th>NAME</th></tr>
<tr><td>1</td><td rowspan="4">VIN</td><td rowspan="4">I</td><td rowspan="4">Switch input. An input bypass capacitor is recommended for minimizing VIN dip.</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>6</td><td>EN</td><td>I</td><td>Active high switch control input. Do not float this pin.</td></tr>
<tr><td>7</td><td>OVP</td><td>I</td><td>Overvoltage protection. Set using an external resistor divider. If no OVP is desired, connect this pin to GND. Do not float this pin.</td></tr>
<tr><td>8</td><td>GND</td><td>—</td><td>Device ground.</td></tr>
<tr><td>12</td><td>SS</td><td>I/O</td><td>Soft start (switch slew rate control). If this functionality is not desired, the SS pin must be left disconnected (floating). In all cases be sure to follow the requirements of Section 9.3.3.</td></tr>
<tr><td>13</td><td rowspan="4">VOUT</td><td rowspan="4">O</td><td rowspan="4">Switch output. A minimum 10-μF output capacitor is recommended.</td></tr>
<tr><td>14</td></tr>
<tr><td>15</td></tr>
<tr><td>16</td></tr>
<tr><td>5</td><td rowspan="4">NC</td><td rowspan="4">—</td><td rowspan="4">NC — No connect. These pins are not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.</td></tr>
<tr><td>9</td></tr>
<tr><td>10</td></tr>
<tr><td>11</td></tr>
<tr><td>—</td><td>Thermal Pad</td><td>—</td><td>Thermal pad (exposed center pad) for heat dissipation purposes. The thermal pad is internally connected to the seal ring and GND.</td></tr>
<tr><td>—</td><td>Metal Lid</td><td>—</td><td>The lid is internally connected to the thermal pad and GND through the seal ring.</td></tr>
</table>

Table 6-2. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	AlCu	1050 nm



1. All dimensions in microns (μm).
2. The inner rectangle is the die and the outer rectangle is the die plus scribe lines.

Table 6-3. Bond Pad Coordinates in Microns (µm)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN	1	725.8	5485.5	881.3	5641
VIN	2	169.3	5485.5	324.8	5641
VIN	3	354.8	5485.5	510.3	5641
VIN	4	540.3	5485.5	695.8	5641
VIN	5	169.3	5300	324.8	5455.5
VIN	6	354.8	5300	510.3	5455.5
VIN	7	540.3	5300	695.8	5455.5
VIN	8	725.8	5300	881.3	5455.5
VIN	9	169.3	5087.95	324.8	5243.45
VIN	10	354.8	5087.95	510.3	5243.45
VIN	11	540.3	5087.95	695.8	5243.45
VIN	12	725.8	5087.95	881.3	5243.45
VIN	13	169.3	4902.45	324.8	5057.95
VIN	14	354.8	4902.45	510.3	5057.95
VIN	15	540.3	4902.45	695.8	5057.95
VIN	16	725.8	4902.45	881.3	5057.95
VIN	17	169.3	3947.9	324.8	4103.4
VIN	18	354.8	3947.9	510.3	4103.4
VIN	19	540.3	3947.9	695.8	4103.4
VIN	20	725.8	3947.9	881.3	4103.4
VIN	21	169.3	3762.4	324.8	3917.9
VIN	22	354.8	3762.4	510.3	3917.9
VIN	23	540.3	3762.4	695.8	3917.9
VIN	24	725.8	3762.4	881.3	3917.9
VINA(1)	25	61.1	2025.65	216.6	2181.15
VINA(1)	26	61.1	1836.15	216.6	1991.65
NC	27	61.1	1645.3	216.6	1800.8
NC	28	61.1	1376.35	216.6	1531.85
EN	29	61.1	1080.75	216.6	1236.25
NC	30	61.1	645.9	216.6	801.4
OVP	31	61.1	451.4	216.6	606.9
GND	32	452.45	61.1	607.95	216.6
GND	33	641.95	61.1	797.45	216.6
NC	34	3103.2	61.1	3258.7	216.6
NC	35	3683.4	652.7	3838.9	808.2
NC	36	3683.4	1221.4	3838.9	1376.9
SS	37	3683.4	1715.65	3838.9	1871.15
VOUT	38	3575.15	3762.4	3730.65	3917.9
VOUT	39	3389.65	3762.4	3545.15	3917.9
VOUT	40	3204.15	3762.4	3359.65	3917.9
VOUT	41	3018.65	3762.4	3174.15	3917.9
VOUT	42	3575.15	3947.9	3730.65	4103.4
VOUT	43	3389.65	3947.9	3545.15	4103.4
VOUT	44	3204.15	3947.9	3359.65	4103.4
VOUT	45	3018.65	3947.9	3174.15	4103.4

Table 6-3. Bond Pad Coordinates in Microns (µm) (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VOUT	46	3575.15	4902.45	3730.65	5057.95
VOUT	47	3389.65	4902.45	3545.15	5057.95
VOUT	48	3204.15	4902.45	3359.65	5057.95
VOUT	49	3018.65	4902.45	3174.15	5057.95
VOUT	50	3575.15	5087.95	3730.65	5243.45
VOUT	51	3389.65	5087.95	3545.15	5243.45
VOUT	52	3204.15	5087.95	3359.65	5243.45
VOUT	53	3018.65	5087.95	3174.15	5243.45
VOUT	54	3575.15	5300	3730.65	5455.5
VOUT	55	3389.65	5300	3545.15	5455.5
VOUT	56	3204.15	5300	3359.65	5455.5
VOUT	57	3018.65	5300	3174.15	5455.5
VOUT	58	3575.15	5485.5	3730.65	5641
VOUT	59	3389.65	5485.5	3545.15	5641
VOUT	60	3204.15	5485.5	3359.65	5641
VOUT	61	3018.65	5485.5	3174.15	5641

(1) VINA supplies internal circuitry. Connect VINA to VIN in a single point manner.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted); all voltages referenced to GND(1)

		MIN	MAX	UNIT
VIN	Input voltage pins	–0.5	16	V
VOUT	Output voltage pins	–0.5	16	V
SS	Soft start pin	–0.3	16	V
EN, OVP	Enable and over voltage protection pins	–0.3	7.5	V
I_{IN}, I_{OUT}	Continuous switch current		5.4	A
I_{IN_PLS}, I_{OUT_PLS}	Pulsed switch current (t ≤ 5 μs)		30	A
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC specification JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted); all voltages referenced to GND

		MIN	MAX	UNIT
VIN	Input voltage pins	4.5	14	V
VOUT	Output voltage pins	0	14[1]	V
EN, OVP	Enable and overvoltage pins	0	7	V
VIN_{SR}	Input voltage slew rate		0.015	V/µs
I_{IN}, I_{OUT}	Continuous switch current		3.5	A
T_J	Operating junction temperature[2]	–55	125	°C

(1) This maximum VOUT voltage is only applicable when the device is disabled (EN = Low). When the device is enabled (EN = High), the maximum VOUT voltage is the input voltage, VIN.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A\ (max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

7.4 Thermal Information

THERMAL METRIC[1]		TPS7H2211-SP HKR (CFP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.7	°C/W
$\Psi_{\theta JT}$	Junction-to-top characterization parameter	1.3	°C/W
$\Psi_{\theta JB}$	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating ambient temperature range T_A = –55°C to 125°C, VIN = 4.5 to 14 V, C_{OUT} = 10 µF, and all voltages referenced to GND (unless otherwise noted); includes group E radiation testing at T_A = 25°C for RHA devices(1)

PARAMETER		TEST CONDITIONS		SUB-GROUP (2)	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
VIN_{UVLOR}	Internal VIN UVLO rising			1, 2, 3	3.2	3.4	3.8	V
VIN_{UVLOF}	Internal VIN UVLO falling			1, 2, 3	2.6	2.9	3.2	V
$HYST_{VIN\text{-}UVLO}$	Internal VIN UVLO hysteresis			1, 2, 3		0.55	0.75	V
I_Q	Quiescent current	I_{OUT} = 0 mA, EN = 7 V		1, 2, 3		5	10	mA
I_F	VIN to VOUT forward leakage current	EN = 0 V, VOUT = 0 V, measured VOUT current	VIN = 14 V	1, 2, 3		1	1.3	mA
			VIN = 12 V	1, 2, 3		0.65	0.94	
			VIN = 9 V	1, 2, 3		0.15	0.49	
			VIN = 4.5 V	1, 2, 3		0.04	0.23	
I_{SD} VIN	VIN off-state supply current	EN = 0 V, VOUT = 0 V, measured VIN current	VIN = 14 V	1, 2, 3		6.9	10	mA
			VIN = 12 V	1, 2, 3		5.9	9.5	
			VIN = 9 V	1, 2, 3		4.4	8	
			VIN = 4.5 V	1, 2, 3		3.7	7	
V_{RCP_ENTER}	Reverse current protection enter voltage(3)	EN = 7 V, see Figure 8-1	VIN = 4.5 V	1		390		mV
			VIN = 14 V	1		363		
V_{RCP_EXIT}	Reverse current protection exit voltage(3)	EN = 7 V, see Figure 8-2	VIN = 4.5 V	1		264		mV
			VIN = 14 V	1		249		
t_{RCP}	Reverse current protection response time	EN = 7 V, see Figure 8-1	VIN = 4.5 V	9		208		µs
			VIN = 14 V	9		247		
I_{RCP}	Reverse current protection leakage current	EN = 0 V, VOUT = 0 to 14 V and VOUT > VIN		1, 2, 3		44	250	µA
		EN = 7 V, VIN = 0 V, VOUT = 0 to 14 V		1, 2, 3		37	240	
SOFT START								
I_{SS}	Soft start charge current			1, 2, 3		65	83	µA
ENABLE (EN) INPUT								
V_{IHEN}	EN threshold voltage, rising			1, 2, 3	0.60	0.63	0.68	V
V_{ILEN}	EN threshold voltage, falling			1, 2, 3	0.50	0.52	0.57	V
$HYST_{EN}$	EN hysteresis voltage			1, 2, 3	94	109	139	mV
t_{LOW_OFF}	EN signal low time during cycling	VOUT falls to < 90%, see Figure 8-3		9, 10, 11	20			µs
VIN_{EN}	VIN percentage for enable (4)			1, 2, 3	75%			
I_{EN}	EN pin input leakage current	EN = 7 V, VIN = 14 V		1, 2, 3		2	12	nA
OVERVOLTAGE PROTECTION (OVP)								
V_{OVPR}	OVP threshold voltage, rising			1, 2, 3	1.11	1.15	1.18	V
V_{OVPF}	OVP threshold voltage, falling			1, 2, 3	1.09	1.14	1.17	V
$HYST_{OVP}$	OVP hysteresis voltage	4.6 V < VIN < 14 V		1, 2, 3	5	14	40	mV
I_{OVP}	OVP pin input leakage current	OVP = 7 V		1, 2, 3		1.5	12	nA
CURRENT LIMIT(5)								
I_{L_trip}	Internal current limit trip point	VIN = 12 V, C_{SS} = 2 nF		1		8		A
I_{L_peak}	Fast trip off current limit peak	VIN = 12 V, 10 Ω to 10 mΩ short in 1 µs, switch inductance = 270 nH		1		25		A
t_{fttr}	Fast trip off response time			9		2.3		µs
t_{fto}	Fast trip off off-time	VIN = 12 V, C_{SS} = 2 nF		9		51		µs
THERMAL SHUTDOWN								
Thermal shutdown						155		°C
Thermal shutdown hysteresis						20		°C

7.5 Electrical Characteristics (continued)

over operating ambient temperature range T_A = –55°C to 125°C, VIN = 4.5 to 14 V, C_{OUT} = 10 µF, and all voltages referenced to GND (unless otherwise noted); includes group E radiation testing at T_A = 25°C for RHA devices(1)

PARAMETER		TEST CONDITIONS		SUB-GROUP (2)	MIN	TYP	MAX	UNIT
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance, lead length ≈ 2.5 mm	VIN = 14 V, I_{OUT} = 3.5 A	–55°C	3		41	45	mΩ
			–40°C			43	46	
			25°C	1		54	60	
			85°C			65	71	
			125°C	2		72	79	
		VIN = 12 V, I_{OUT} = 3.5 A	–55°C	3		41	45	
			–40°C			43	46	
			25°C	1		54	60	
			85°C			65	71	
			125°C	2		72	79	
		VIN = 9 V, I_{OUT} = 3.5 A	–55°C	3		41	45	
			–40°C			43	46	
			25°C	1		54	61	
			85°C			65	71	
			125°C	2		72	79	
		VIN = 6 V, I_{OUT} = 3.5 A	–55°C	3		41	45	
			–40°C			43	47	
			25°C	1		54	61	
			85°C			65	71	
			125°C	2		72	79	
		VIN = 4.5 V, I_{OUT} = 3.5 A	–55°C	3		44	48	
			–40°C			47	50	
			25°C	1		59	65	
			85°C			71	76	
			125°C	2		79	84	

(1) See the 5962-18220 SMD (standard microcircuit drawing) for additional information on the RHA devices.
(2) For subgroup definitions, see the Quality Conformance Inspection table
(3) This parameter is not referenced to GND; it is referenced from VOUT to VIN.
(4) VIN must be ≥ 75% of its final value before EN is asserted only if VIN_{SR} > $VOUT_{SR}$.
(5) See Section 9.3.2 for additional information on current limits and how the associated parameters are defined.

7.6 Switching Characteristics

over operating ambient temperature T_A = 25°C, C_{OUT} = 10 µF, C_{SS} = 2 nF, R_{LOAD} = 10 Ω (unless otherwise noted); all voltages referenced to GND

PARAMETER		TEST CONDITIONS	SUBGROUP[1]	MIN	TYP	MAX	UNIT
VIN = 5 V							
t_{ON}	Turn-on time	See Figure 8-4	9		107		µs
t_{OFF}	Turn-off time				56		µs
t_F	VOUT fall time				167		µs
t_{ASSERT}	OVP assert time	See Figure 8-5	9		8		µs
$t_{DEASSERT}$	OVP deassert time				41		µs
VIN = 12 V							
t_{ON}	Turn-on time	See Figure 8-4	9		220		µs
t_{OFF}	Turn-off time				41		µs
t_F	VOUT fall time				139		µs
t_{ASSERT}	OVP assert time	See Figure 8-5	9		6		µs
$t_{DEASSERT}$	OVP deassert time				63		µs

(1) For subgroup definitions, see the Quality Conformance Inspection table

7.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

7.8 Typical Characteristics

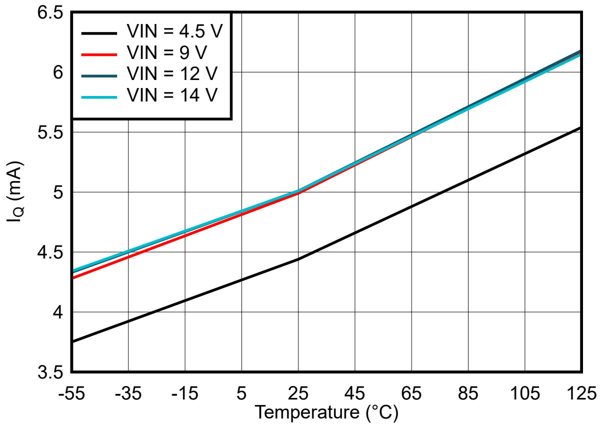


Figure 7-1. I_Q vs Temperature Across VIN

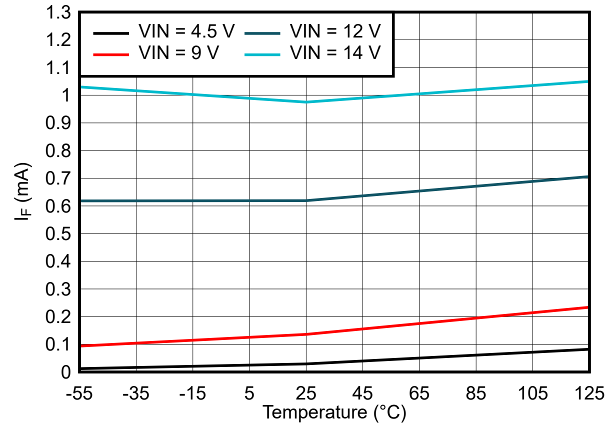


Figure 7-2. I_F vs Temperature Across VIN

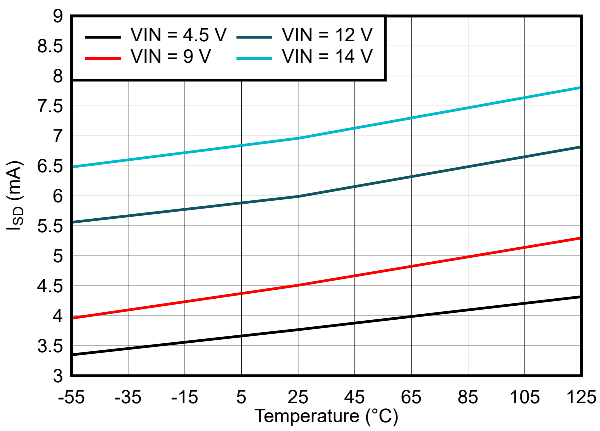
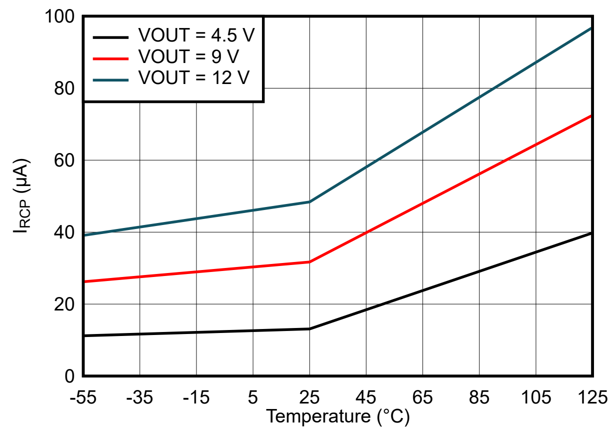
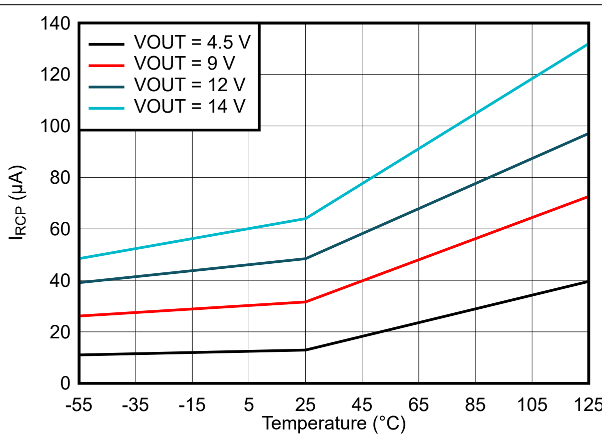


Figure 7-3. I_{SD} vs Temperature Across VIN



VIN = 0 V

Figure 7-4. I_{RCP} vs Temperature Across VOUT With EN = 7 V



VIN = 0 V

Figure 7-5. I_{RCP} vs Temperature Across VOUT With EN = 0 V

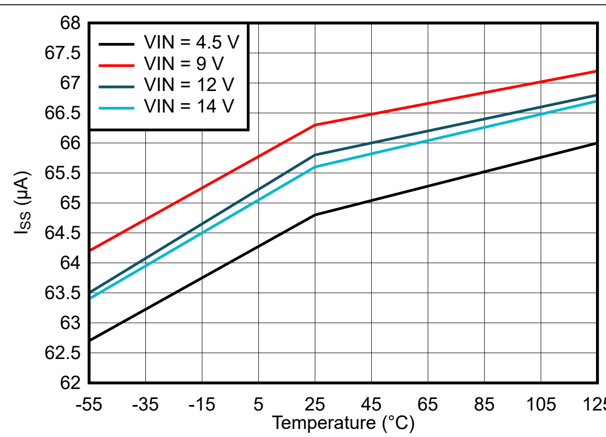
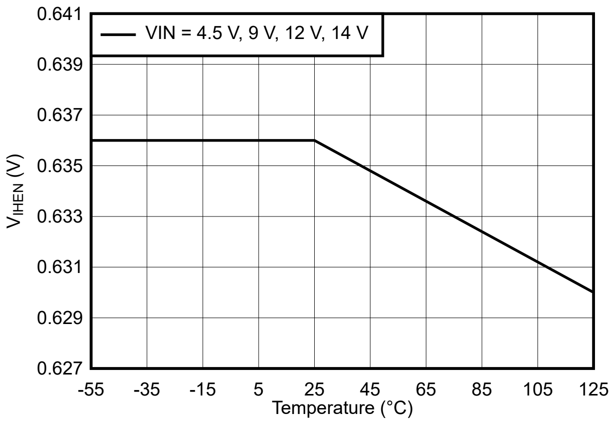
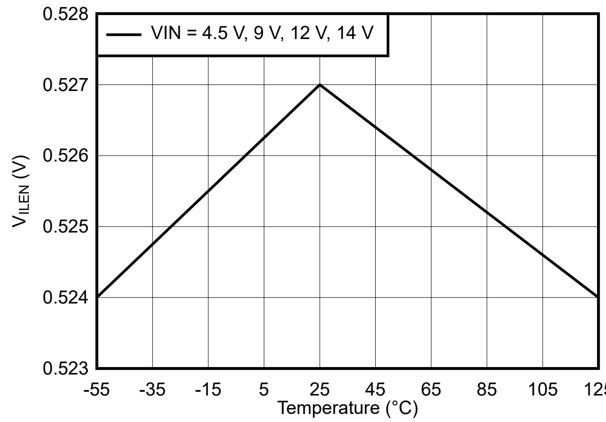


Figure 7-6. I_{SS} vs Temperature Across VIN



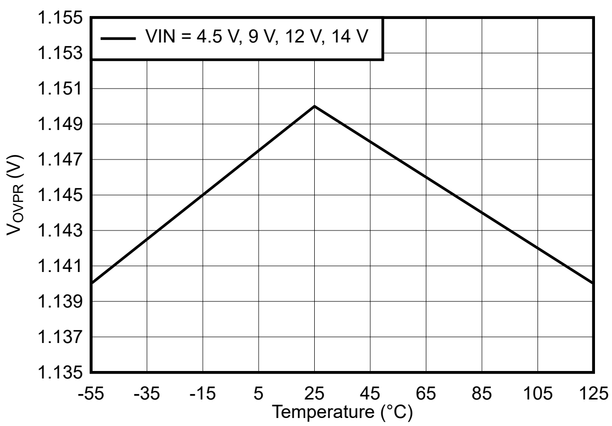
There was no observed VIN dependency across these measured values

Figure 7-7. V_{IHEN} vs Temperature Across VIN



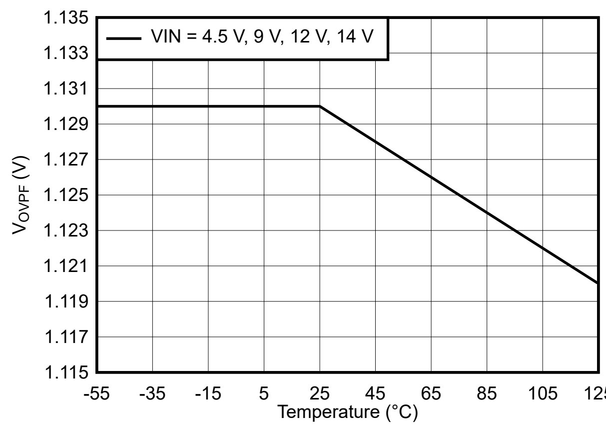
There was no observed VIN dependency across these measured values

Figure 7-8. V_{ILEN} vs Temperature Across VIN



There was no observed VIN dependency across these measured values

Figure 7-9. V_{OVPR} vs Temperature Across VIN



There was no observed VIN dependency across these measured values

Figure 7-10. V_{OVPF} vs Temperature Across VIN

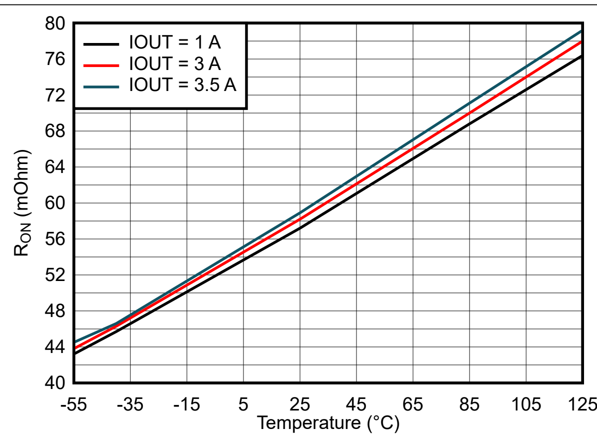


Figure 7-11. On-Resistance vs Temperature Across Loads at VIN = 4.5 V

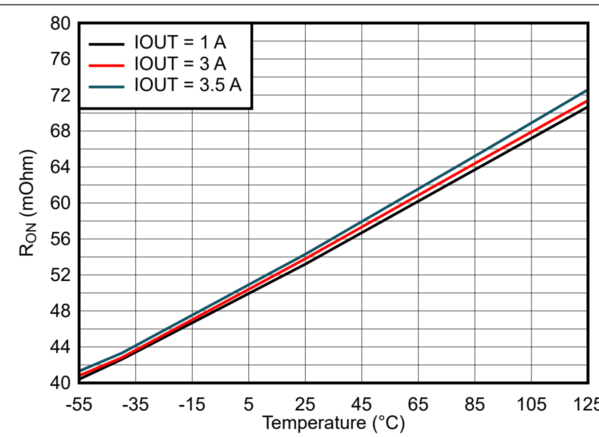


Figure 7-12. On-Resistance vs Temperature Across Loads at VIN = 6 V

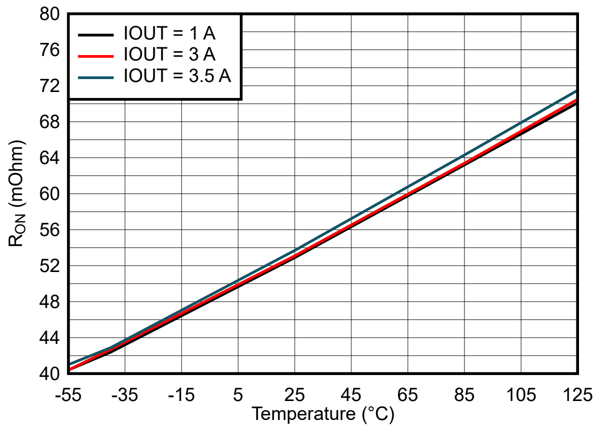


Figure 7-13. On-Resistance vs Temperature Across Loads at VIN = 9 V

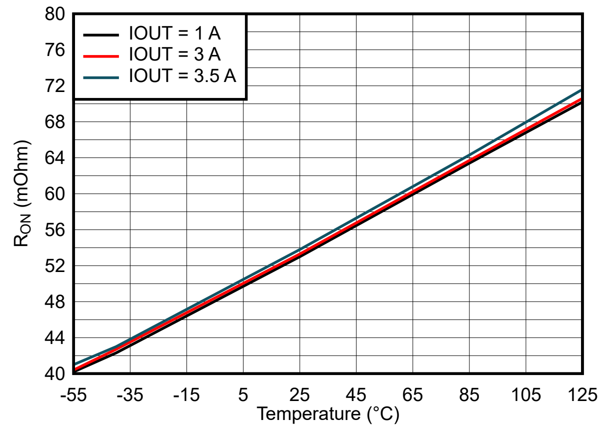


Figure 7-14. On-Resistance vs Temperature Across Loads at VIN = 12 V

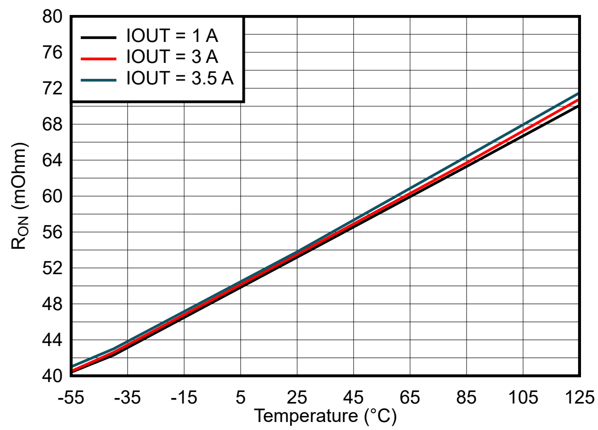
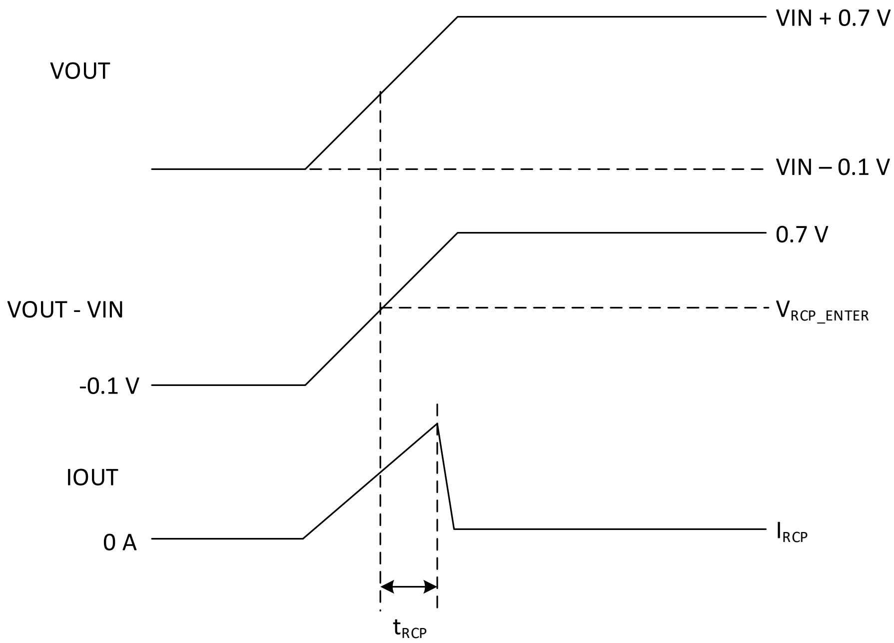


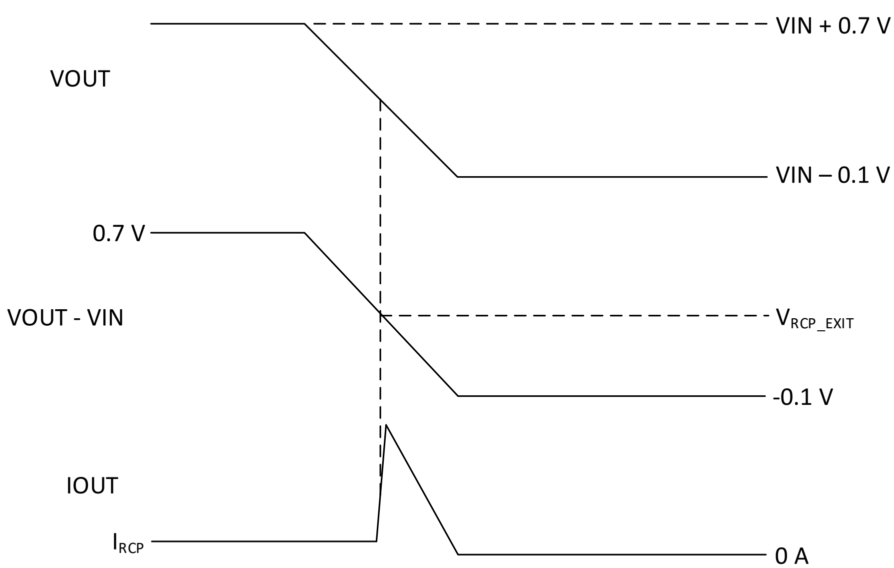
Figure 7-15. On-Resistance vs Temperature Across Loads at VIN = 14 V

8 Parameter Measurement Information



A. VIN is held constant during the test.
B. V_{RCP_ENTER} is referenced from VOUT to VIN. It is the threshold that, when reached, will turn-off the main switch FETs to prevent reverse current flow.

Figure 8-1. Reverse Current Protection Enter (V_{RCP_ENTER}) Test Waveforms



A. VIN is held constant during the test.
B. V_{RCP_EXIT} is referenced from VOUT to VIN. It is the threshold that, when reached, will turn-off the reverse current protection feature.

Figure 8-2. Reverse Current Protection Exit (V_{RCP_EXIT}) Test Waveforms

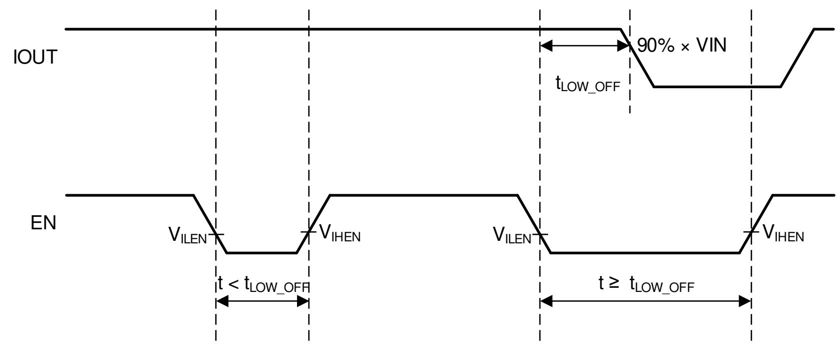


Figure 8-3. EN Signal Low Time to Restart Device (t_{LOW_OFF})

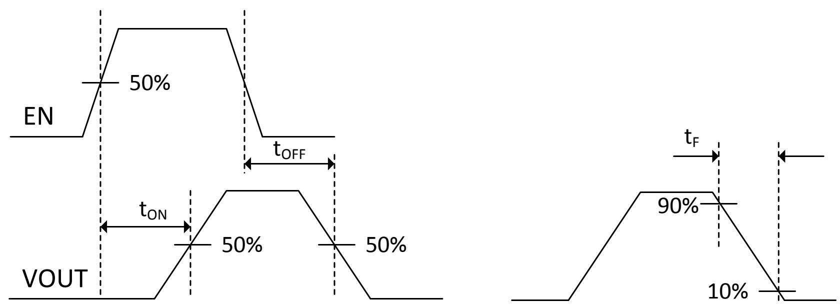
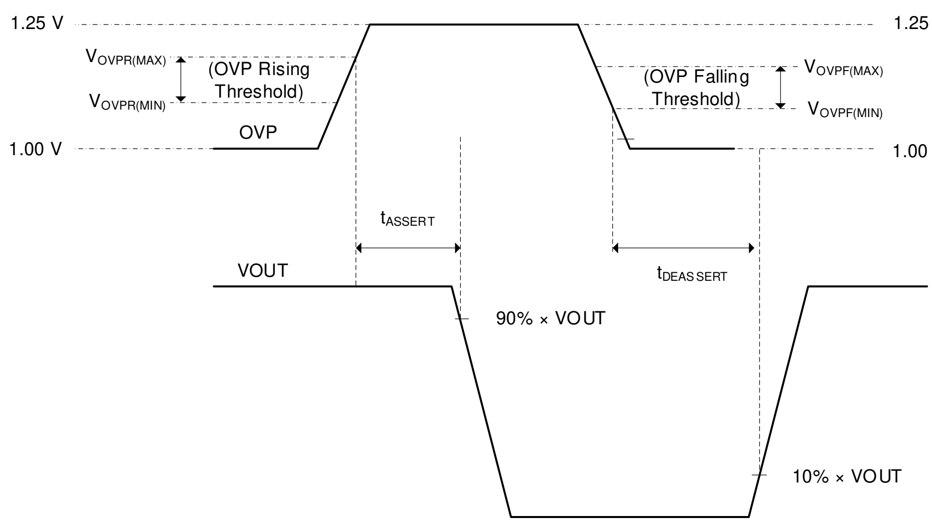


Figure 8-4. Turn-On Time (t_{ON}), Turn-Off Time (t_{OFF}), and VOUT Fall Time (t_F) Waveforms



A. The OVP test signal uses a typical rise time and fall time of 30 ns.

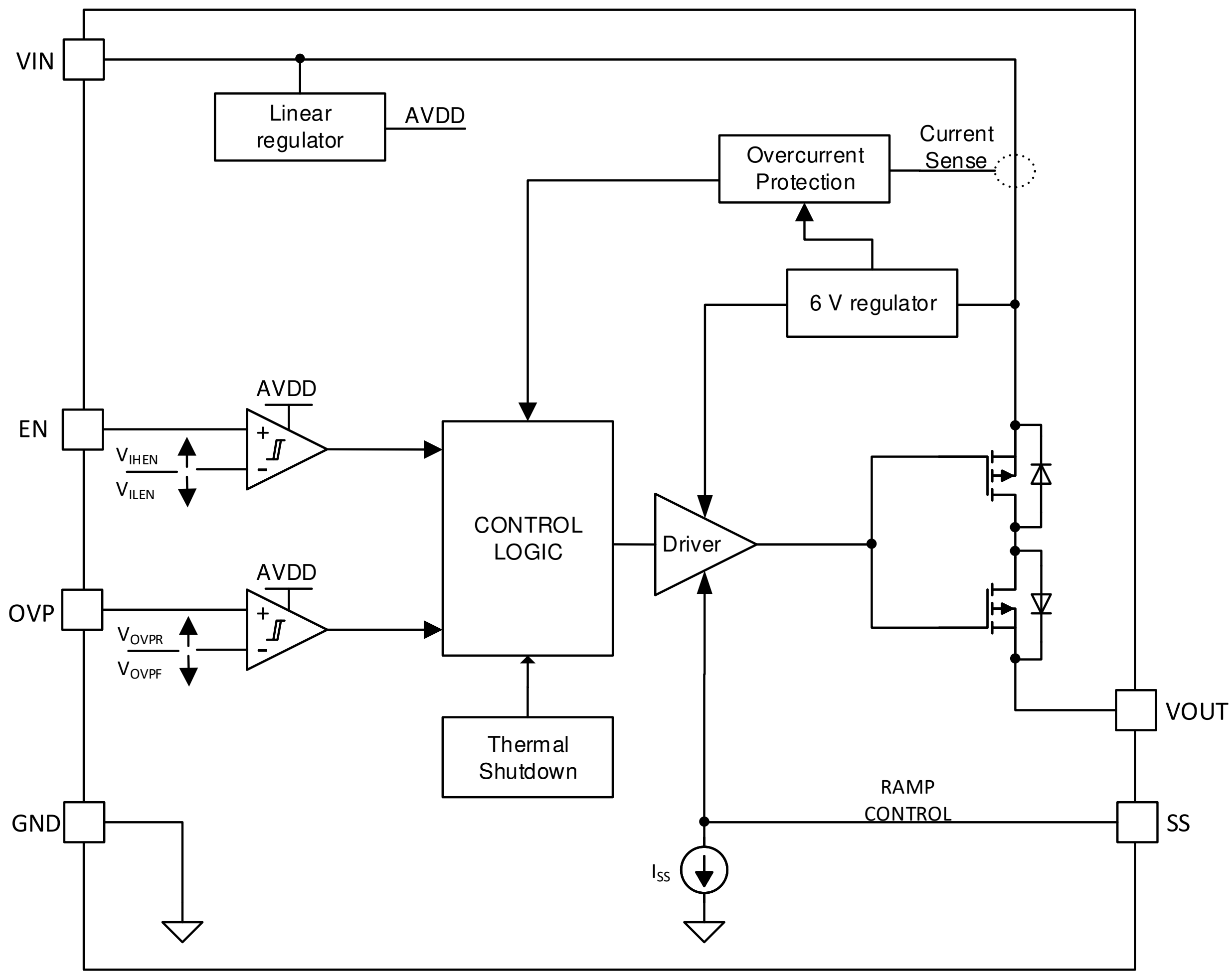
Figure 8-5. OVP Assert (t_{ASSERT}) and OVP Deassert ($t_{DEASSERT}$) Waveforms

9 Detailed Description

9.1 Overview

The TPS7H2211-SP device is a single channel, 3.5-A eFuse with a programmable turn-on slew rate (soft start) and overvoltage protection (OVP). Additionally, the TPS7H2211-SP features reverse current protection capability for power distribution applications. It is available as a radiation hardness assured device to 100 krad(Si).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Enable and Overvoltage Protection

Figure 9-1 shows how resistor dividers from VIN connected to the EN and OVP pins can be used to set the enable and overvoltage trip points.

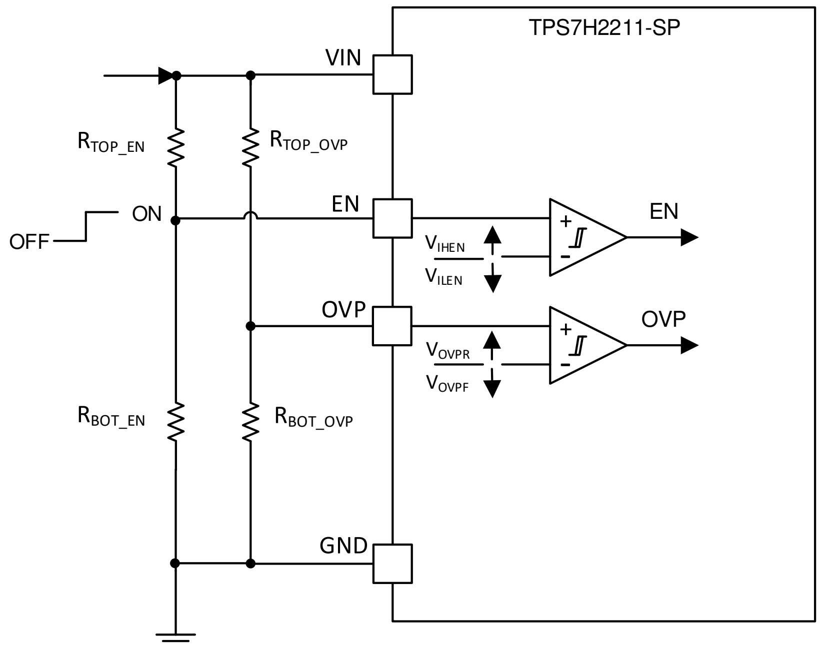


Figure 9-1. Enable and OVP Thresholds Set by Resistor Dividers

The EN pin turns on or turns off the internal switch FETs. An EN voltage greater than V_{IHEN} turns on the switch, and a voltage less than V_{ILEN} turns off the switch. The external resistor divider allows the enable threshold to be configured for a different enable rising voltage (VIN_{EN_RISE}) and a disable falling voltage (VIN_{EN_FALL}) based on the V_{IHEN} and V_{ILEN} specifications respectively. Generally, applications are optimized to configure the enable rising voltage. However, if desired the falling voltage can be configured to use the EN pin as an under voltage protection (UVP) feature.

Typically R_{TOP_EN} is set to 100 kΩ and a value for R_{BOT_EN} is calculated. Section 10.2.2.2.2 shows how these resistor values could be calculated. The enable rising and falling threshold parameters are shown in Figure 9-2, and equations to calculate the resulting rising and falling voltages are shown in Equation 1 and Equation 2 respectively. These equations do not take into account the small EN leakage current which has minimal effect on the results.

Additionally, ensure EN is not asserted before VIN is ≥ 75% of its final value as indicated in the electrical characteristics footnote (see Section 7.5). This is only required if VIN_{SR} > $VOUT_{SR}$. This requirement is to prevent a false overcurrent trigger event.

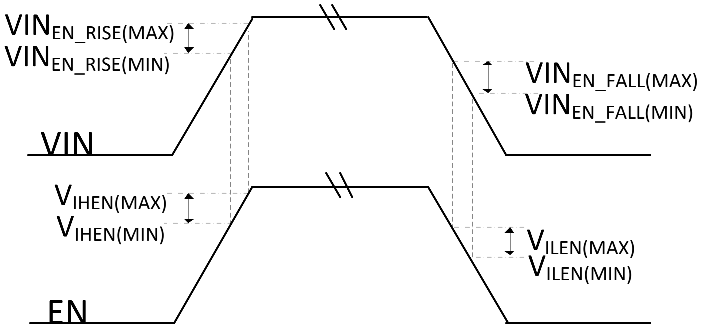


Figure 9-2. Enable Rising and Falling Thresholds

$$VIN_{EN\_RISE} = V_{IHEN} \frac{R_{TOP\_EN} + R_{BOT\_EN}}{R_{BOT\_EN}} \quad (1)$$

$$VIN_{EN\_FALL} = V_{ILEN} \frac{R_{TOP\_EN} + R_{BOT\_EN}}{R_{BOT\_EN}} \quad (2)$$

Similarly, the overvoltage protection (OVP) feature can be configured using a resistor divider from VIN connected to the OVP pin. A voltage at the OVP pin greater than V_{OVPR} will turn off the switch FETs, and a voltage less than V_{OVPF} will keep the switch FETs on. If this feature is not desired, the OVP pin must be grounded.

The OVP feature is intended to protect downstream devices from an overvoltage condition (by turning off the eFuse if the OVP threshold is reached). The OVP feature does not protect the TPS7H2211-SP eFuse itself from higher values of VIN. Follow the 14-V maximum VIN value and the 7-V maximum OVP value in the recommended operating conditions.

Typically R_{TOP_OVP} is set to 100 kΩ and a value for R_{BOT_OVP} is calculated. Section 10.2.1.2.3 shows how these resistor values could be calculated. The OVP rising and falling threshold parameters are shown in Figure 9-3, and equations to calculate the resulting rising and falling voltages are shown in Equation 3 and Equation 4 respectively. These equations do not take into account the small OVP leakage current which has minimal effect on the results.

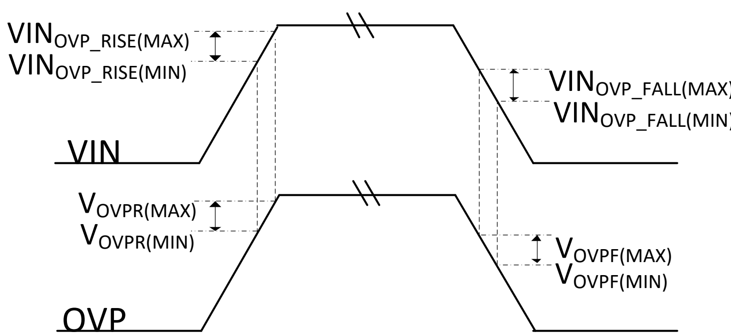


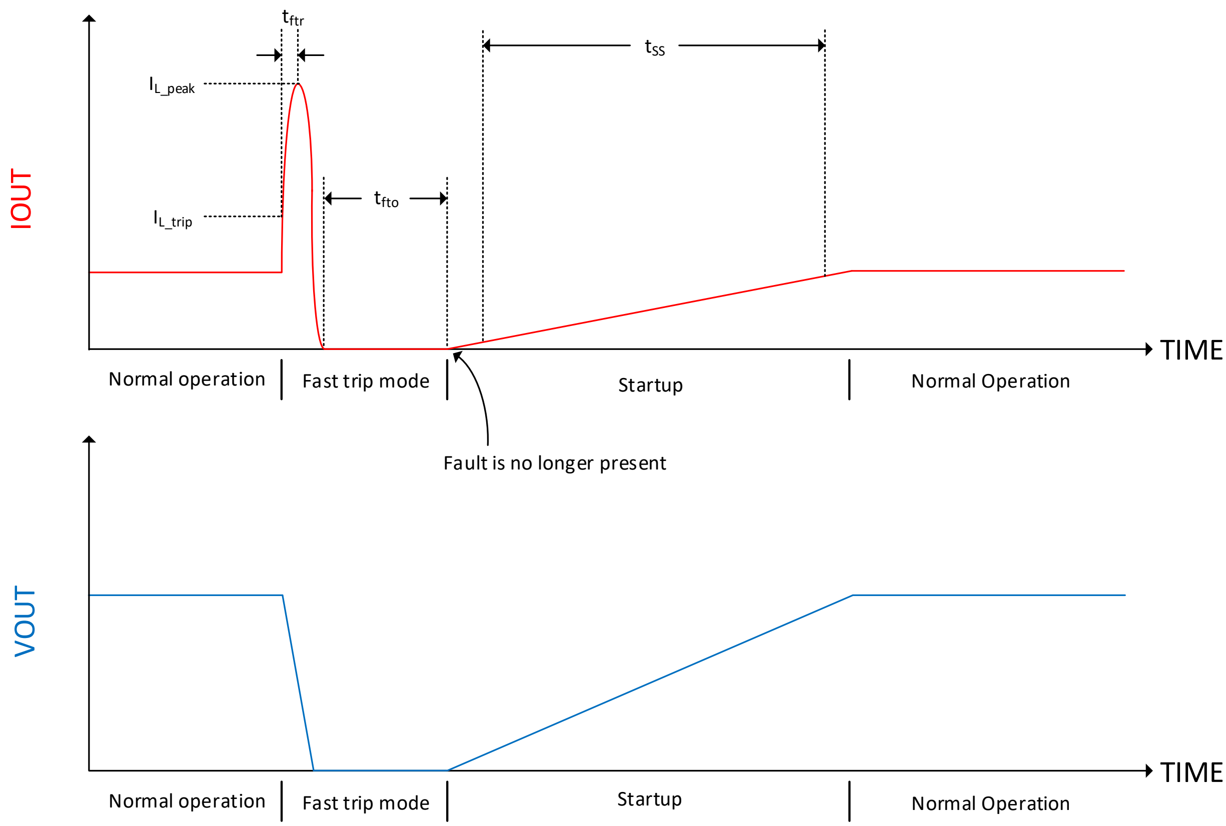
Figure 9-3. OVP Rising and Falling Thresholds

$$VIN_{OVP\_RISE} = V_{OVPR} \frac{R_{TOP\_OVP} + R_{BOT\_OVP}}{R_{BOT\_OVP}} \quad (3)$$

$$VIN_{OVP\_FALL} = V_{OVPF} \frac{R_{TOP\_OVP} + R_{BOT\_OVP}}{R_{BOT\_OVP}} \quad (4)$$

9.3.2 Current Limit

There is an internal current limit intended to protect the TPS7H2211-SP against hard short circuit conditions. Figure 9-4 shows a short circuit condition followed by an immediate recovery. The TPS7H2211-SP internal short circuit protection trips at I_{L_trip}. It takes time t_{ftr}, for the internal circuitry to respond to the short circuit condition. Before the current limit circuitry responds, the current through the switch will continue to rise to a peak value, I_{L_peak}. At this point the current limit circuitry responds and quickly turns off the switch. As there is no active discharge on VOUT, the rate of discharge will depend on external factors such as the short condition and COUT. The switch will stay off for time t_{fto}, before turning-on again.



A. The following values were measured at VIN = 12 V, a parasitic switch inductance nominal value of 270 nH, and R_{OUT} changing from 10 Ω to 10 mΩ in 1 µs:
- I_{L_trip}(typ) = 8.5 A
- t_{ftr}(typ) = 2.3 µs
- I_{L_peak}(typ) = 25 A
- t_{fto}(typ) = 51 µs

Figure 9-4. Single Hard Short and Recovery

As shown in Figure 9-4, the TPS7H2211-SP is designed to quickly respond to a hard fault condition to minimize the current peak. I_{L_trip} and t_{ftr} are highly dependent upon the actual fault conditions.

While Figure 9-4 shows a hard short condition that immediately recovers, Figure 9-5 shows a hard short condition that does not immediately recover. Instead, the device twice enters the fast trip mode before the fault is removed.

CAUTION
A short will repeat indefinitely until the short is removed or until the device is disabled. The TPS7H2211-SP is not intended to remain in this mode indefinitely.

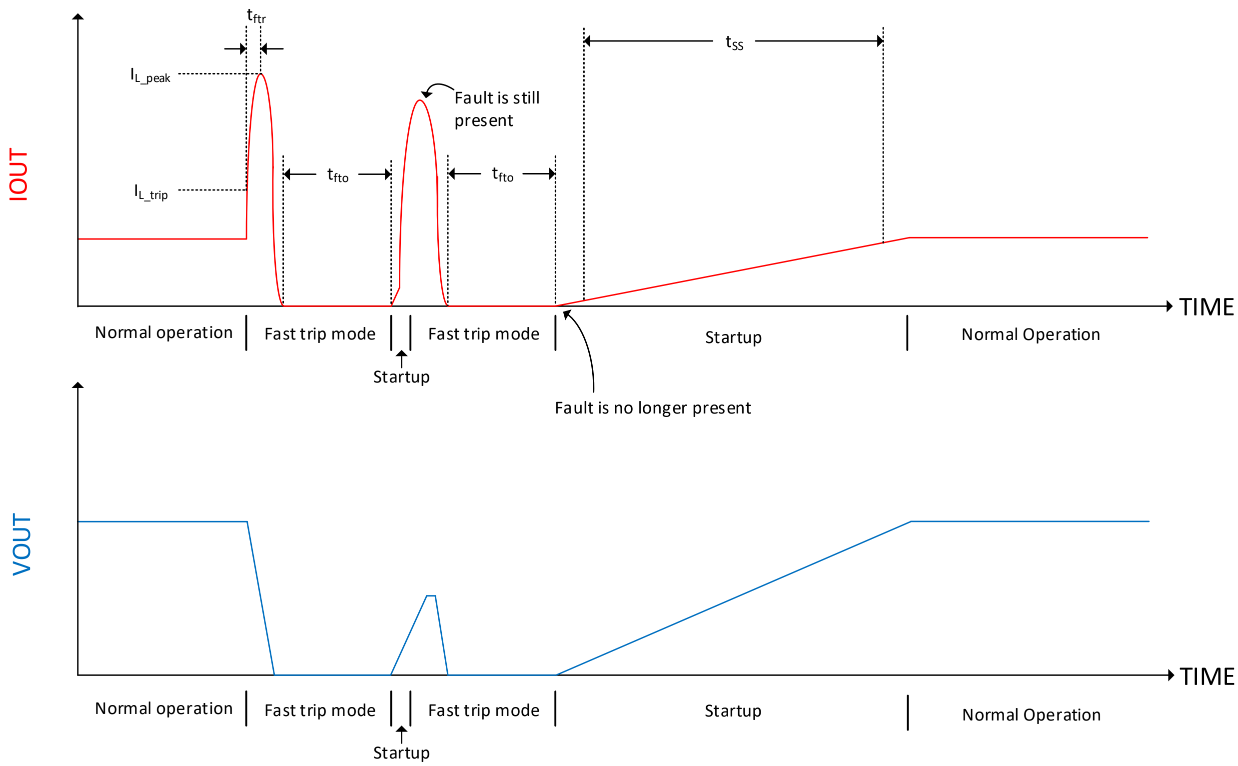


Figure 9-5. Two Hard Shorts and Recovery

9.3.3 Soft Start (Adjustable Rise Time)

An external capacitor, C_{SS}, connected between the VOUT and SS pins, sets t_{SS}, the soft start time. t_{SS} is defined as the time it takes VOUT to rise from 10% to 90% of its final value. Equation 5 calculates the needed C_{SS} capacitor where I_{SS} is the soft start current (typically 65 µA) and VOUT is the final output voltage reached (for example, 12 V).

$$C_{ss} = \frac{t_{SS} \times I_{SS}}{VOUT \times 0.8} \tag{5}$$

In order to avoid false trips due to the internal current limit being triggered during startup, the slew rate $VOUT_{SR}$, must satisfy Equation 6 where I_{L_trip} is the internal current limit trip point (typically 8.5 A), I_{OUT} is the final output current (max of 3.5 A), and C_{OUT} is the output capacitance. In the *Application and Implementation Soft Start Time* section, a suggested derated value for I_{L_TRIP} is shown.

If external current limit circuitry is used, it is recommended to replace the I_{L_trip} value with the minimum trip-point value of the external current limit (assuming this trip-point is less than I_{L_trip}). This is in order to ensure the external current limit circuitry isn't tripped during startup.

$$VOUT_{SR} < \frac{I_{L\_trip} - I_{OUT}}{C_{OUT}} \quad (6)$$

The output slew rate of the eFuse, $VOUT_{SR}$, can be calculated as shown in Equation 7. To determine the worst case slew rate, it is recommended to use the maximum value of I_{SS}, 83 µA, and the minimum value of the selected capacitor. These worst case conditions may also be used to calculate the worst case (fastest) t_{SS} time.

$$VOUT_{SR} = \frac{I_{SS}}{C_{SS}} = \frac{V_{OUT} \times 0.8}{t_{SS}} \quad (7)$$

9.3.4 Parallel Operation

The TPS7H2211-SP can be configured in parallel operation either to increase the current capability, up to nearly 7 A, or to reduce the on-state resistance. In this case, all pins are shared as shown in Figure 9-6.

Since the SS pin sinks current, the combined pins result in a doubled current sink value; consequently the calculated capacitance values must be doubled. The EN and OVP pins have no additional changes from the non-parallel case as they are high impedance inputs.

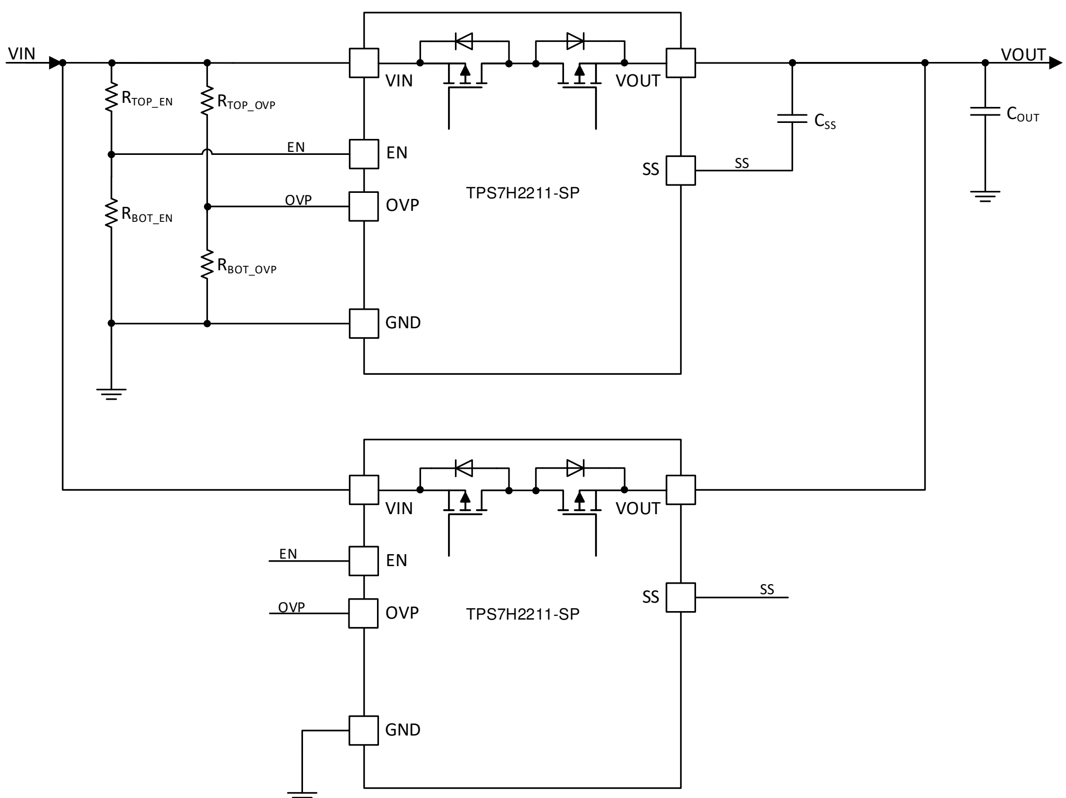


Figure 9-6. Parallel Configuration to Reduce Resistance or Increase Current Capability

9.3.5 Reverse Current Protection

The TPS72211-SP eFuse features back to back FETs to prevent current flow from VIN to VOUT and from VOUT to VIN when the switch is disabled (excluding leakage currents). This supports cold sparing (redundancy) applications. For example, VOUT may be up to 14 V while VIN is between 0 V and 14 V. In all cases, only small leakage current will result.

Additionally, the eFuse features active reverse current protection when the switch is enabled. This protection feature is activated when VOUT rises above VIN by V_{RCP_ENTER} (typically 363 mV at VIN = 14 V) which causes the switch to turn-off. After V_{RCP_ENTER} is reached, it will take time, t_{RCP} (typically 247 µs at VIN = 14 V) for the switch to turn off. Until the switch responds and turns off, there may be high reverse current through the switch. After this time, only a small amount of leakage current, I_{RCP}, will result from VOUT to VIN (typically 40 µA). The switch will again be enabled after VOUT – VIN falls to less than or equal to V_{RCP_EXIT} (typically 249 mV at VIN = 14 V).

The test waveforms for V_{RCP_ENTER} and V_{RCP_EXIT} can be found in Figure 8-1 and Figure 8-2 respectively.

9.3.6 Forward Leakage Current

When VIN is powered but the TPS7H2211-SP is disabled (EN is low), the internal FETs are disabled, creating a high impedance path from VIN to VOUT. However, there are parasitic leakage paths that could cause VOUT to slowly charge. The forward leakage current, I_F, indicates how much current flows from VIN to VOUT during this situation. This is typically 0.65 mA at VIN = 12 V but could be a maximum of 1.3 mA at 14 V.

Some applications may tolerate these leakage mechanisms while some applications may need to pay particular attention to this behavior. It is particularly relevant when VOUT is a high impedance node (and therefore the leakage current goes entirely to charging VOUT instead of being dissipated). By using the basic capacitor equation shown in Equation 8, the time for the voltage to rise to a given value can be theoretically calculated.

$$\Delta t = \Delta V_{OUT} \times C_{OUT} / I_F \quad (8)$$

where

- Δt = time to charge to final value
- ΔV_{OUT} = change in output voltage; for a 0 V starting voltage, use V_{IN}

For example, with a 12-V input voltage and a 220-µF output capacitance, VOUT will typically charge to 12 V in 4.1 seconds (using I_F = 0.65 mA, ΔV_{OUT} = 12 V, C_{OUT} = 220 µF).

If the output voltage must remain below a certain value, a pull-down resistor can be utilized with a value as calculated by Equation 9.

$$VOUT_{LKG\_MAX} = I_F \times R_{PULL\_DOWN} \quad (9)$$

where

- $VOUT_{LKG\_MAX}$ = maximum output voltage due to leakage current, I_F
- R_{PULL_DOWN} = external pull-down resistor from VOUT to GND

For example, placing a 1-kΩ resistor between VOUT and ground will ensure VOUT does not rise above 0.65-V typically or 1.3-V worse case due to the I_F current. It is recommended to ensure the resistor can handle the worst case power dissipation when the switch is enabled and VOUT ≈ VIN.

9.4 Device Functional Modes

Table 9-1 lists the state of the eFuse for a given EN input voltage.

Table 9-1.

EN PIN	SWITCH STATUS
$V_{EN} < V_{ILEN}$	OFF: VOUT = Open
$V_{EN} > V_{IHEN}$	ON: VOUT ≈ VIN

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TPS7H2211-SP device is a single channel, 3.5-A eFuse with configurable features such as overvoltage protection, soft start, and enable. Additionally, the TPS7H2211-SP features reverse current protection for power distribution applications.

10.2 Typical Applications

The following list shows just a few of the multiple applications for the TPS7H2211-SP eFuse. The first two are discussed in further detail.

- Cold sparing (redundancy) for primary and secondary (redundant) voltage rails (common in satellites)
- Protection of loads from upstream latch-up sensitive converters
- Power rail sequencing
- Power multiplexing
- Power system ORing

10.2.1 Application 1: Cold Sparing

In applications where a primary and secondary (redundant) power rails are present, the TPS7H2211-SP readily implements cold sparing because of its reverse current blocking capability. Generally, the primary eFuse will be enabled. If there is a reason to switch to the secondary rail, the primary eFuse will be turned-off and the secondary eFuse will be turned-on. In this cold sparing application, since the eFuse is placed at the input of the point of load regulator, the on-resistance of the switch is not highly critical.

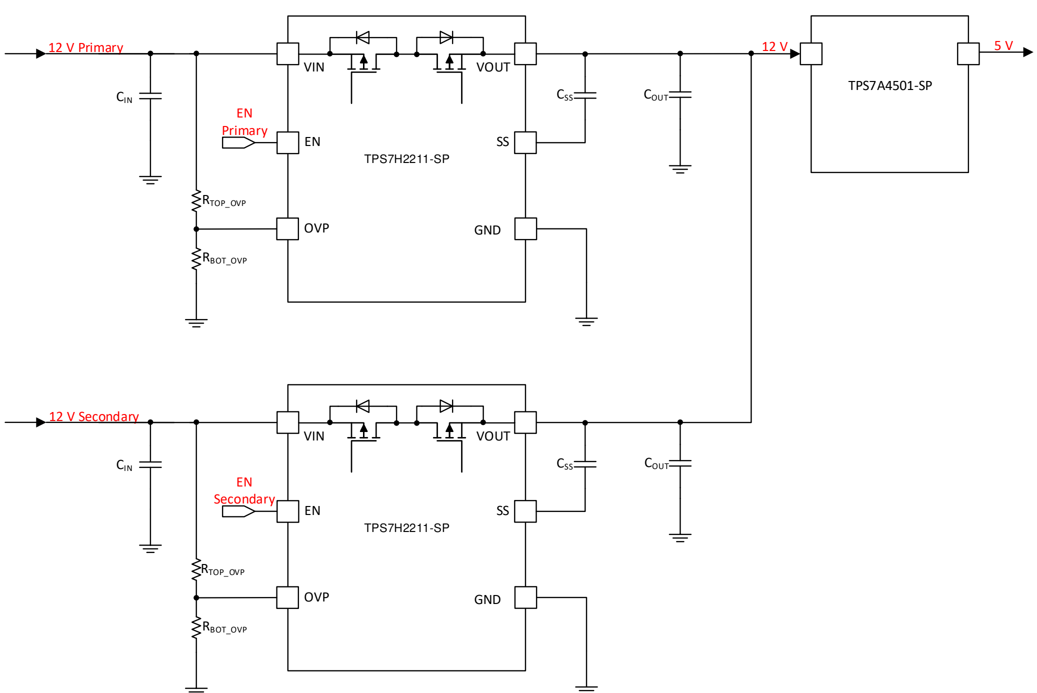


Figure 10-1. Cold Sparing Example Using the TPS7H2211-SP

10.2.1.1 Design Requirements

Table 10-1 shows the design parameters used for this example.

Table 10-1. Design Parameters

DESIGN PARAMETER	REQUIREMENT
VIN, input voltage	12 V ± 5%
VIN_{EN}, turn-on voltage	Not applicable - will control EN pin from central controller
VIN_{OVP_RISE}, overvoltage protection set point	13.5 V
I_{OUT}, switch current	3 A
t_{SS}, VOUT soft start time	10 ms

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Capacitance

At least a 10-μF output capacitor is recommended on VOUT. Additionally, a capacitor on VIN is recommended in order to keep the input stable. However, it is generally advisable to use higher capacitance values to align with the TI EVM (evaluation module) and the radiation testing configuration (mostly relevant for SETs on VOUT as a higher capacitance generally reduces the SETs). A good higher capacitance value is 170.1 μF–specifically, 1 × 150-μF tantalum, 2 × 10-μF ceramic, and 1 × 0.1-μF ceramic capacitors. This is what is selected for this design for both the input and output capacitance.

10.2.1.2.2 Enable Control

The EN pin controls the state of the eFuse. Bringing EN high turns on the switch and bringing EN low turns off the switch. In a cold sparing application, only one of the switches is to be enabled at a given time. This EN signal can be controlled from external circuitry. For example, a microcontroller or FPGA may interface to the eFuses through two GPIO pins. The TPS7H2211-SP is compatible with a variety of logic levels such as 1.1-V logic.

When the primary 12-V rail is to be used, EN of the primary eFuse is set high while the EN of the secondary eFuse remains low. If there is an issue with the primary rail, the secondary rail can instead be used. To make this change, first deassert the EN pin of the primary eFuse. Then assert the EN pin of the secondary eFuse. If both pins are enabled at the same time, reverse current flow in one of the eFuses may result. While there is internal reverse current protection circuitry in the eFuses, it is simple to avoid this problem through proper EN sequencing.

10.2.1.2.3 Overvoltage Protection

The overvoltage protection is set by configuring the R_{BOT_OVP} and R_{TOP_OVP} resistors. The overvoltage protection feature turns off the switch if the input voltage exceeds a predetermined value as described in Section 9.3.1. For this design, the goal is to have the overvoltage protection activate at a nominal voltage of 13.5 V. First set R_{TOP_OVP} = 100 kΩ with a 0.1% tolerance resistor, then use Equation 10 to calculate the nominal value of R_{BOT_OVP}. A nominal 9.31-kΩ 0.1% tolerance resistor best satisfies the equation.

$$R_{BOT\_OVP} = \frac{V_{OVPR(TYP)} \times R_{TOP\_OVP}}{VIN_{OVP\_RISE} - V_{OVPR(TYP)}} \tag{10}$$

where

- $V_{OVPR(TYP)}$ = 1.15 V
- R_{TOP_OVP} = 100 kΩ
- VIN_{OVP_RISE} = 13.5 V

In order to ensure the selected R_{BOT_OVP} value is acceptable for both the minimum and maximum OVP rising threshold, use Equation 11. $VIN_{OVP\_RISE(MIN)}$ is selected as the highest possible value that VIN will reach during nominal operation (to prevent false OVP trips). $VIN_{OVP\_RISE(MAX)}$ may be selected by the user as long as it is within the VIN *Recommended Operating Conditions*. These selections result in an allowable value of R_{BOT_OVP}

between 9.214 kΩ and 9.650 kΩ. The selected 9.31-kΩ 0.1% tolerance resistor satisfies these constraints, even when taking into account its tolerance.

$$\frac{V_{OVPR(MAX)} \times R_{TOP\_OVP} \times (1 + R_{tolerance})}{VIN_{OVP\_RISE(MAX)} - V_{OVPR(MAX)}} \leq R_{BOT\_OVP} \leq \frac{V_{OVPR(MIN)} \times R_{TOP\_OVP} \times (1 - R_{tolerance})}{VIN_{OVP\_RISE(MIN)} - V_{OVPR(MIN)}} \tag{11}$$

where

- $V_{OVPR(MAX)}$ = 1.18 V
- R_{TOP_OVP} = 100 kΩ
- $R_{tolerance}$ = 0.01% = 0.001
- $VIN_{OVP\_RISE(MAX)}$ = 14 V
- $V_{OVPR(MIN)}$ = 1.11 V
- $VIN_{OVP\_RISE(MIN)}$ = VIN × (1 + tolerance) = 12.6 V

Since the OVP pin has hysteresis, the OVP falling threshold will be different than the rising threshold. Therefore, in order to ensure the selected R_{BOT_OVP} value is acceptable for the OVP falling threshold, use Equation 12. $VIN_{OVP\_FALL(MIN)}$ and $VIN_{OVP\_FALL(MAX)}$ values may be selected using the same method as for $VIN_{OVP\_RISE(MIN)}$ and $VIN_{OVP\_RISE(MAX)}$. These selections results in an allowable R_{BOT_OVP} value between of 9.129 kΩ and 9.460 kΩ. The selected 9.31-kΩ 0.1% tolerance resistor also satisfies these constraints, even when taking into account its tolerance.

$$\frac{V_{OVPF(MAX)} \times R_{TOP\_OVP} \times (1 + R_{tolerance})}{VIN_{OVP\_FALL(MAX)} - V_{OVPF(MAX)}} \leq R_{BOT\_OVP} \leq \frac{V_{OVPF(MIN)} \times R_{TOP\_OVP} \times (1 - R_{tolerance})}{VIN_{OVP\_FALL(MIN)} - V_{OVPF(MIN)}} \tag{12}$$

where

- $V_{OVPF(MAX)}$ = 1.17 V
- R_{TOP_OVP} = 100 kΩ
- $R_{tolerance}$ = 0.001
- $VIN_{OVP\_FALL(MAX)}$ = 14 V
- $V_{OVPF(MIN)}$ = 1.09 V
- $VIN_{OVP\_FALL(MIN)}$ = VIN × (1 + tolerance) = 12.6 V

To summarize, using Equation 3 and Equation 4 with R_{TOP_OVP} = 100 kΩ and R_{BOT_OVP} = 9.31 kΩ, the eFuse will nominally go into overvoltage protection mode at 13.50 V and exit at 13.38 V. Taking into account the minimum and maximum OVP pin threshold and resistor tolerances, the switch will enter over voltage protection mode between 13.01 V and 13.88 V and exit between 12.77 V and 13.76 V.

CAUTION

The eFuse input voltage must remain within the recommended operating conditions (which contain a maximum VIN of 14 V). If OVP is configured above 14 V, then the OVP mode should only be used as a last resort feature. The eFuse is not intended to be above 14 V.

10.2.1.2.4 Soft Start Time

The desired 10-ms soft start time is achieved following the procedure in Section 9.3.3. The procedure is replicated below for convenience.

First, use Equation 13 to determine the needed value of C_{SS}. This results in a calculated C_{SS} value of 67.7 nF. A 68-nF ±10% capacitor is selected.

$$C_{ss} = \frac{t_{SS} \times I_{SS}}{VOUT \times 0.8} \tag{13}$$

where

- t_{SS} = 10 ms = 10 × 10^{-3} s
- $I_{SS(TYP)}$ = 65 µA = 65 × 10^{-6} A
- $V_{OUT(NOM)}$ = 12 V

Next determine the resulting slew rate using Equation 14. Using the minimum value for the 10% tolerance C_{SS} and the maximum value for I_{SS} results in the worst case (fastest) slew rate of 1,356 V/s.

$$VOUT_{SR} = \frac{I_{SS}}{C_{SS}} = \frac{V_{OUT} \times 0.8}{t_{SS}} \tag{14}$$

where

- $I_{SS(MAX)}$ = 83 µA = 83 × 10^{-6} A
- C_{SS} = 68 nF × (1 – 10%) = 61.2 × 10^{-9} F

Finally, determine if the resulting slew rate is less than the maximum allowed by Equation 15. I_{L_trip} is typically 8.5 A, but in order to select a conservative value it is suggested to let I_{L_trip} = 5.4 A (which is also the absolute maximum rating for continuous switch current). The 1,356-V/s slew rate is less than the maximum acceptable slew rate of 14,109 V/s. Therefore, this soft start capacitor is acceptable.

$$VOUT_{SR} < \frac{I_{L\_trip} - I_{OUT}}{C_{OUT}} \tag{15}$$

where

- I_{L_trip} = 5.4 A
- $I_{OUT(NOM)}$ = 3.0 A
- C_{OUT} = 170.1 µF = 170.1 × 10^{-6} F

While it is typically trivial to meet the slew rate restrictions, note that for space applications a large output capacitor is often utilized. This results in a lower maximum acceptable slew rate and additional care must be taken in order to ensure the expected slew rate is not too fast.

10.2.1.2.5 Summary

The final component values are shown in Figure 10-2.

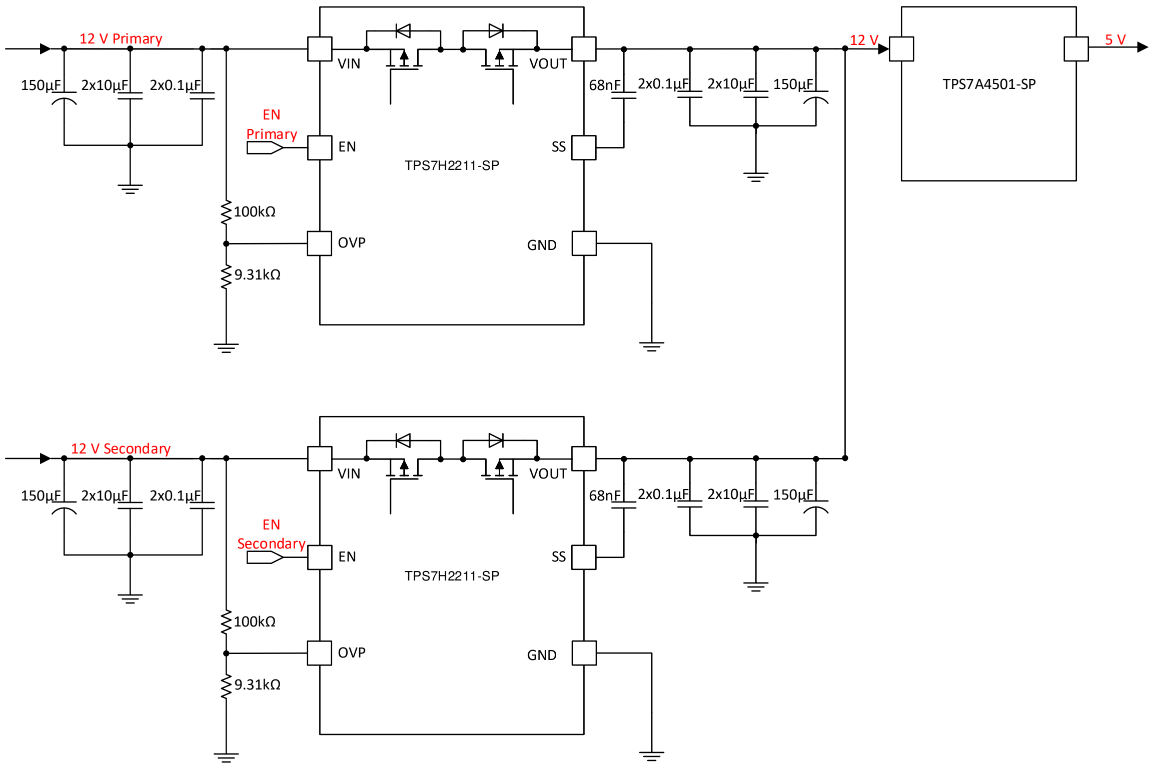


Figure 10-2. Cold Sparing Example With Calculated Component Values

10.2.1.3 Application Curve

Figure 10-3 shows the first eFuse being enabled. Figure 10-4 shows the first eFuse being powered down and the second device being powered up (switch from primary to secondary power). The less time both switches are turned-off, the less droop on VOUT.

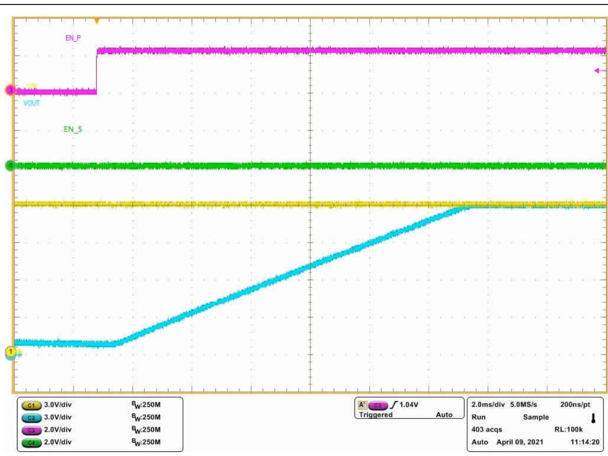


Figure 10-3. Power-Up Behavior of Primary TPS7H2211-SP in a Cold Sparing Application

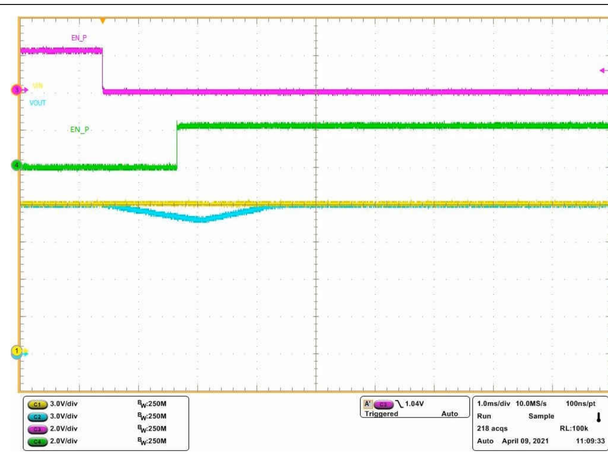


Figure 10-4. Switch From Primary to Secondary TPS7H2211-SP in a Cold Sparing Application

10.2.2 Application 2: Protection

The TPS7H2211-SP can be used to protect a load from an upstream latchup sensitive regulator. The eFuse will provide overvoltage protection (OVP) and under-voltage protection (by using the EN pin). If the upstream regulator fails, the eFuse will disconnect the load from the regulator. The load could then be powered by a redundant supply (see the *Application 1: Cold Sparing* section).

In this configuration, the on-resistance of the switch is more important as it is placed after the point of load regulator. Two eFuses can be placed in parallel to further reduce the on-resistance. In the design example shown here, it was determined only one eFuse was needed.

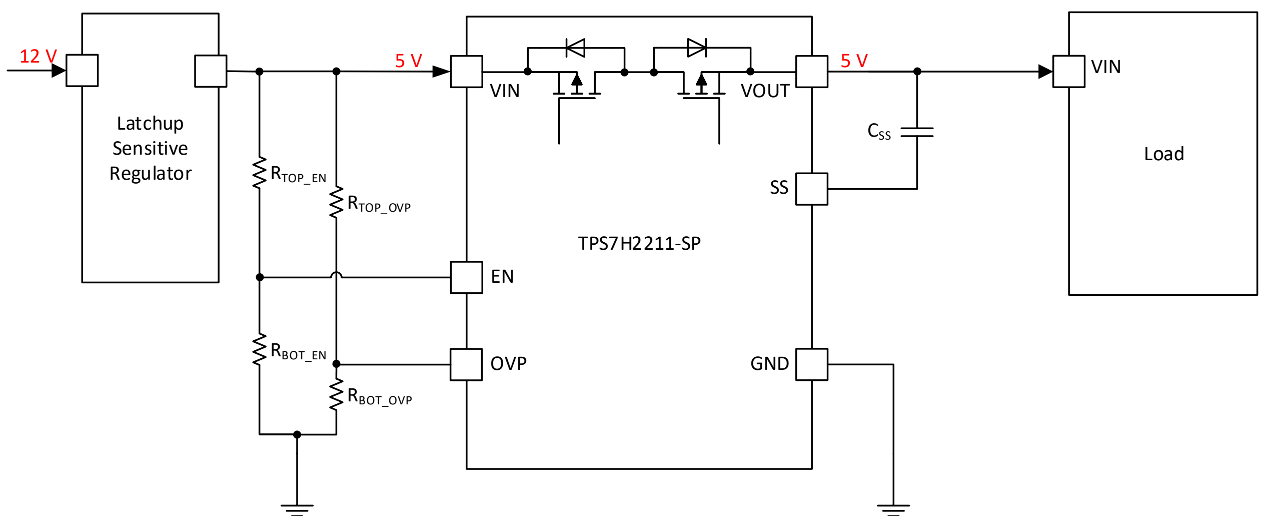


Figure 10-5. Protection Example Using the TPS7H2211-SP

10.2.2.1 Design Requirements

Table 10-2 shows the design parameters used for this example.

Table 10-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VIN, input voltage	5 V ± 2%
VIN_{EN}, turn-on voltage	4.5 V
VIN_{OVP_RISE}, overvoltage protection set point	5.4 V
I_{OUT}, switch current	3 A
t_{SS}, VOUT soft start time	1 ms

10.2.2.2 Detailed Design Procedure

10.2.2.2.1 Capacitance

Similarly to Section 10.2.1.2.1, 170.1 µF of input and output capacitance is selected–specifically, 1 × 150-µF tantalum, 2 × 10-µF ceramic, and 1 × 0.1-µF ceramic capacitors.

10.2.2.2.2 Enable Control

The enable threshold is set by configuring the R_{BOT_EN} and R_{TOP_EN} resistors in order to turn on the switch at the desired input voltage as described in Section 9.3.1. For this design, the goal is to turn on the switch when VIN reaches 4.5 V. First we set R_{TOP_EN} = 100 kΩ with a 0.1% tolerance resistor, and then use Equation 16 to calculate the nominal R_{BOT_EN}. A 16.2-kΩ 0.1% tolerance resistor is found to best satisfy the equation.

$$R_{BOT\_EN} = \frac{V_{IHEN(TYP)} \times R_{TOP\_EN}}{VIN_{EN\_RISE} - V_{IHEN(TYP)}} \quad (16)$$

where

- $V_{IHEN(TYP)}$ = 0.63 V
- R_{TOP_EN} = 100 kΩ
- VIN_{EN_RISE} = 4.5 V

Additionally, it should be ensured the worst case minimum and maximum turn-on voltages are acceptable. The minimum turn-on voltage would ideally be above 4.5 V (the minimum operating voltage). However, in this case that is not possible to achieve, and it is acceptable to allow the minimum turn-on voltage to be lower than 4.5 V (such as 4.2 V). Note however that the device will not be fully operational until at least 4.5 V is reached. This is okay in this case since the VIN voltage will quickly rise to above 4.5 V which puts the device in a fully operational state. The eFuse maximum turn-on voltage must be less than the minimum final VIN value (which is 4.9 V as determined by the 2% tolerance on the 5-V rail). The maximum turn-on voltage can be calculated using Equation 17. It is determined that $VIN_{EN\_RISE(MAX)}$ = 4.89 V which is under 4.9 V.

$$VIN_{EN\_RISE(MAX)} = V_{IHEN(MAX)} \times \frac{R_{TOP\_EN} \times (1 + R_{tolerance}) + R_{BOT\_EN} \times (1 - R_{tolerance})}{R_{BOT\_EN} \times (1 - R_{tolerance})} \quad (17)$$

where

- $V_{IHEN(MAX)}$ = 0.68 V
- R_{TOP_EN} = 100 kΩ
- R_{BOT_EN} = 16.2 kΩ
- $R_{tolerance}$ = 0.1% = 0.001

An alternative method to ensure the selected R_{BOT_EN} value is acceptable for both the minimum and maximum enable thresholds is to select minimum and maximum values for VIN_{EN_RISE} and VIN_{EN_FALL} and ensure Equation 18 and Equation 19 are satisfied.

$$\frac{V_{IHEN(MAX)} \times R_{TOP\_EN} \times (1 + R_{tolerance})}{VIN_{EN\_RISE(MAX)} - V_{IHEN(MAX)}} \le R_{BOT\_EN} \le \frac{V_{IHEN(MIN)} \times R_{TOP\_EN} \times (1 - R_{tolerance})}{VIN_{EN\_RISE(MIN)} - V_{IHEN(MIN)}} \quad (18)$$

$$\frac{V_{ILEN(MAX)} \times R_{TOP\_EN} \times (1 + R_{tolerance})}{VIN_{EN\_FALL(MAX)} - V_{IHLN(MAX)}} \le R_{BOT\_EN} \le \frac{V_{ILEN(MIN)} \times R_{TOP\_EN} \times (1 - R_{tolerance})}{VIN_{EN\_FALL(MIN)} - V_{ILEN(MIN)}} \quad (19)$$

To summarize, using Equation 1 and Equation 2 with R_{TOP_EN} = 100 kΩ and R_{BOT_EN} = 16.2 kΩ, shows the eFuse will nominally turn on at 4.52 V and turn off at 3.73 V. The turn-off voltage is different due to the enable pin hysteresis. Taking into account the maximum and minimum EN pin thresholds and resistor tolerances the switch will turn on between 4.30 V and 4.89 V and turn off between 3.58 V and 4.10 V. To change the turn-off levels requires changing the turn-on levels. The turn-off level will act as an under voltage protection (UVP) feature to protect the downstream circuitry from receiving a sustained voltage under 3.58 V (which could potentially put the circuit in an undefined state).

Additionally, as the turn-on voltage minimum is 4.30 V, this is greater than 75% of the final VIN value (4.30 V > 4.9 V × 0.75 = 3.68 V). Therefore, there is no EN and slew rate related requirements as indicated in the electrical characteristics footnote (see Section 7.5). If the device was enabled under 3.68 V (not advised; this is less than the recommended operating VIN voltage of 4.5 V), the output voltage slew rate must be less than the input voltage slew rate or a false overcurrent trigger may occur.

10.2.2.2.3 Overvoltage Protection

The TPS7H2211-SP eFuse is exceptionally well suited to provide overvoltage protection in this application. This is because even if the upstream regulator fails in a manner that shorts its input to output (12 V), the TPS7H2211-SP eFuse is able to handle up to 14 V at the input with full data sheet specified performance.

The overvoltage protection is set by configuring the R_{BOT_OVP} and R_{TOP_OVP} resistors similarly to Section 10.2.1.2.3. The overvoltage protection feature turns off the switch if the input voltage exceeds a predetermined value. For this design, the goal is to have the overvoltage protection activate at a nominal voltage of 5.4 V. First set R_{TOP_OVP} = 100 kΩ with a 0.1% tolerance resistor, then use Equation 20 to calculate the nominal value of R_{BOT_OVP}. A nominal 27-kΩ 0.1% tolerance resistor best satisfies the equation.

$$R_{BOT\_OVP} = \frac{V_{OVPR(TYP)} \times R_{TOP\_OVP}}{VIN_{OVP\_RISE} - V_{OVPR(TYP)}} \tag{20}$$

where

- $V_{OVPR(TYP)}$ = 1.15 V
- R_{TOP_OVP} = 100 kΩ
- VIN_{OVP_RISE} = 5.4 V

In order to ensure the selected R_{BOT_OVP} value is acceptable for both the minimum and maximum OVP rising threshold, use Equation 21. $VIN_{OVP\_RISE(MIN)}$ is selected as the highest possible value that VIN will reach during nominal operation. $VIN_{OVP\_RISE(MAX)}$ may be selected by the user as long as it is within the VIN *Recommended Operating Conditions*. These selections result in an allowable value of R_{BOT_OVP} between 9.214 kΩ and 27.791 kΩ. The selected 27 kΩ-0.1% tolerance resistor satisfies these constraints, even when taking into account its tolerance.

$$\frac{V_{OVPR(MAX)} \times R_{TOP\_OVP} \times (1 + R_{tolerance})}{VIN_{OVP\_RISE(MAX)} - V_{OVPR(MAX)}} \leq R_{BOT\_OVP} \leq \frac{V_{OVPR(MIN)} \times R_{TOP\_OVP} \times (1 - R_{tolerance})}{VIN_{OVP\_RISE(MIN)} - V_{OVPR(MIN)}} \tag{21}$$

where

- $V_{OVPR(MAX)}$ = 1.18 V
- R_{TOP_OVP} = 100 kΩ
- $R_{tolerance}$ = 0.01% = 0.001
- $VIN_{OVP\_RISE(MAX)}$ = 14 V
- $V_{OVPR(MIN)}$ = 1.11 V
- $VIN_{OVP\_RISE(MIN)}$ = VIN × (1 + tolerance) = 5.1 V

Since the OVP pin has hysteresis, the OVP falling threshold will be different than the rising threshold. Therefore, in order to ensure the selected R_{BOT_OVP} value is acceptable for the OVP falling threshold, use Equation 22. $VIN_{OVP\_FALL(MIN)}$ and $VIN_{OVP\_FALL(MAX)}$ values may be selected using the same method as for $VIN_{OVP\_RISE(MIN)}$ and $VIN_{OVP\_RISE(MAX)}$. These selections results in an allowable R_{BOT_OVP} value between of 9.128 kΩ and 27.154 kΩ. The selected 27 kΩ-0.1% tolerance resistor also satisfies these constraints, even when taking into account its tolerance.

$$\frac{V_{OVPF(MAX)} \times R_{TOP\_OVP} \times (1 + R_{tolerance})}{VIN_{OVP\_FALL(MAX)} - V_{OVPF(MAX)}} \leq R_{BOT\_OVP} \leq \frac{V_{OVPF(MIN)} \times R_{TOP\_OVP} \times (1 - R_{tolerance})}{VIN_{OVP\_FALL(MIN)} - V_{OVPF(MIN)}} \tag{22}$$

where

- $V_{OVPF(MAX)}$ = 1.17 V
- R_{TOP_OVP} = 100 kΩ
- $R_{tolerance}$ = 0.001
- $VIN_{OVP\_FALL(MAX)}$ = 14 V

- $V_{OVPF(MIN)}$ = 1.09 V
- $VIN_{OVP\_FALL(MIN)}$ = VIN × (1 + tolerance) = 5.1 V

To summarize, using Equation 3 and Equation 4 with R_{TOP_OVP} = 100 kΩ and R_{BOT_OVP} = 27 kΩ, the eFuse will nominally go into overvoltage protection mode at 5.41 V and exit at 5.36 V. Taking into account the minimum and maximum OVP pin threshold and resistor tolerances, the switch will enter overvoltage protection mode between 5.21 V and 5.56 V and exit between 5.12 V and 5.51 V.

10.2.2.2.4 Soft Start Time

The desired 1-ms soft start time is achieved following the procedure in Section 9.3.3. The procedure is replicated below for convenience.

First, use Equation 23 to determine the needed value of C_{SS}. This results in a calculated C_{SS} value of 16.3 nF. A 22-nF ±10% capacitor is selected.

$$C_{ss} = \frac{t_{SS} \times I_{SS}}{VOUT \times 0.8} \tag{23}$$

where

- t_{SS} = 1 ms = 1 × 10^{-3} s
- $I_{SS(TYP)}$ = 65 µA = 65 × 10^{-6} A
- $V_{OUT(NOM)}$ = 5 V

Next determine the resulting slew rate using Equation 24. Using the minimum value for the 10% tolerance C_{SS} and the maximum value for I_{SS} results in the worst case (fastest) slew rate of 4,192 V/s.

$$VOUT_{SR} = \frac{I_{SS}}{C_{SS}} = \frac{V_{OUT} \times 0.8}{t_{SS}} \tag{24}$$

where

- $I_{SS(MAX)}$ = 83 µA = 83 × 10^{-6} A
- C_{SS} = 22 nF × (1 – 10%) = 19.8 × 10^{-9} F

Finally, determine if the resulting slew rate is less than the maximum allowed by Equation 25. I_{L_trip} is typically 8.5 A, but in order to select a conservative value it is suggested to let I_{L_trip} = 5.4 A (which is also the absolute maximum rating for continuous switch current). The 2,955-V/s slew rate is less than the maximum acceptable slew rate of 4,192 V/s. Therefore, this soft start capacitor is acceptable.

$$VOUT_{SR} < \frac{I_{L\_trip} - I_{OUT}}{C_{OUT}} \tag{25}$$

where

- I_{L_trip} = 5.4 A
- $I_{OUT(NOM)}$ = 3.0 A
- C_{OUT} = 170.1 µF = 170.1 × 10^{-6} F

While it is typically trivial to meet the slew rate restrictions (as demonstrated here by selecting a relatively fast soft start time), note that for space applications a large output capacitor is often utilized. This results in a lower maximum acceptable slew rate and additional care must be taken in order to ensure the expected slew rate is not too fast.

10.2.2.2.5 Summary

The final calculated values are shown in Figure 10-6.

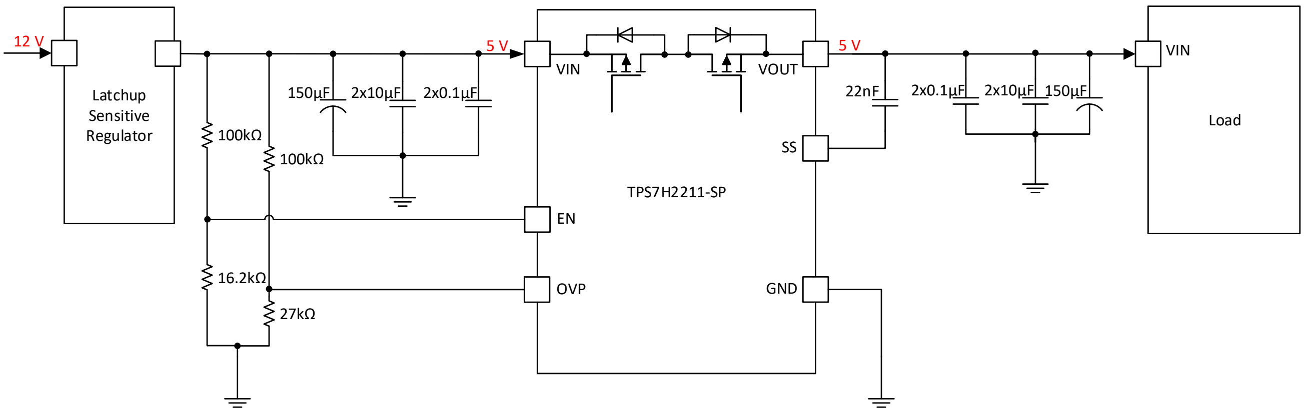


Figure 10-6. Final Schematic With Component Values for the Protection Application

10.2.2.3 Application Curve

Figure 10-7 shows how a 12 V overvoltage event trips the overvoltage protection (OVP) circuitry to protect the downstream load. Figure 10-8 shows how the switch will turn-off if the voltage falls too far.

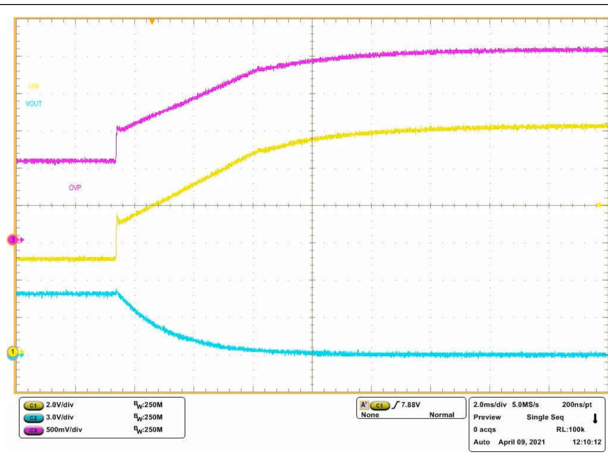


Figure 10-7. Overvoltage Protection of TPS7H2211-SP in Protection Application

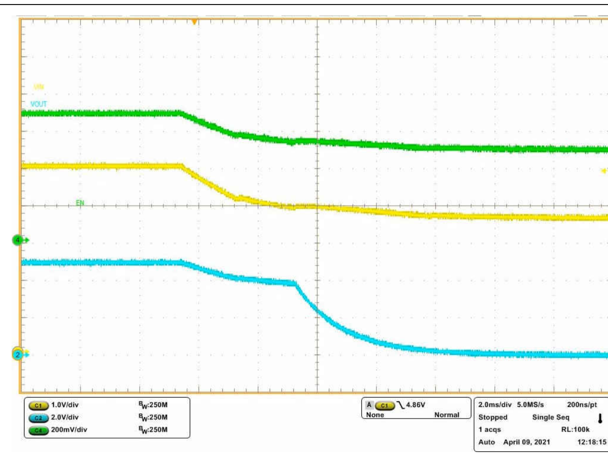


Figure 10-8. Undervoltage Turn-Off of TPS7H2211-SP in Protection Application

11 Power Supply Recommendations

The TPS7H2211-SP is designed to operate from a wide input voltage supply range between 4.5 V to 14 V. This supply voltage must be well regulated and proper local bypass capacitors must be used for proper electrical performance from VIN to GND. Due to stringent requirements for space applications, typically numerous input bypass capacitors are used and the total capacitance is much larger than for commercial applications. The TPS7H2211-SP evaluation module uses 1 × 150-µF tantalum capacitor in parallel with 2 × 10-µF ceramic capacitors and 1 × 0.1-µF ceramic capacitor.

12 Layout

12.1 Layout Guidelines

For best performance, make all traces as short as possible. Place the input and output capacitors close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Use wide traces for VIN, VOUT, and GND to help minimize the parasitic electrical effects. Pay particular attention to minimizing the length of the C_{SS} capacitor connection between VOUT and SS in order to minimize stray inductance.

Use thermal vias for the thermal pad to ensure the device remains at allowable temperatures, especially during fault conditions (such as a short at VOUT). As the thermal pad is internally connected to GND, TI recommends the vias be connected to a large GND plane on the printed circuit board.

12.2 Layout Example

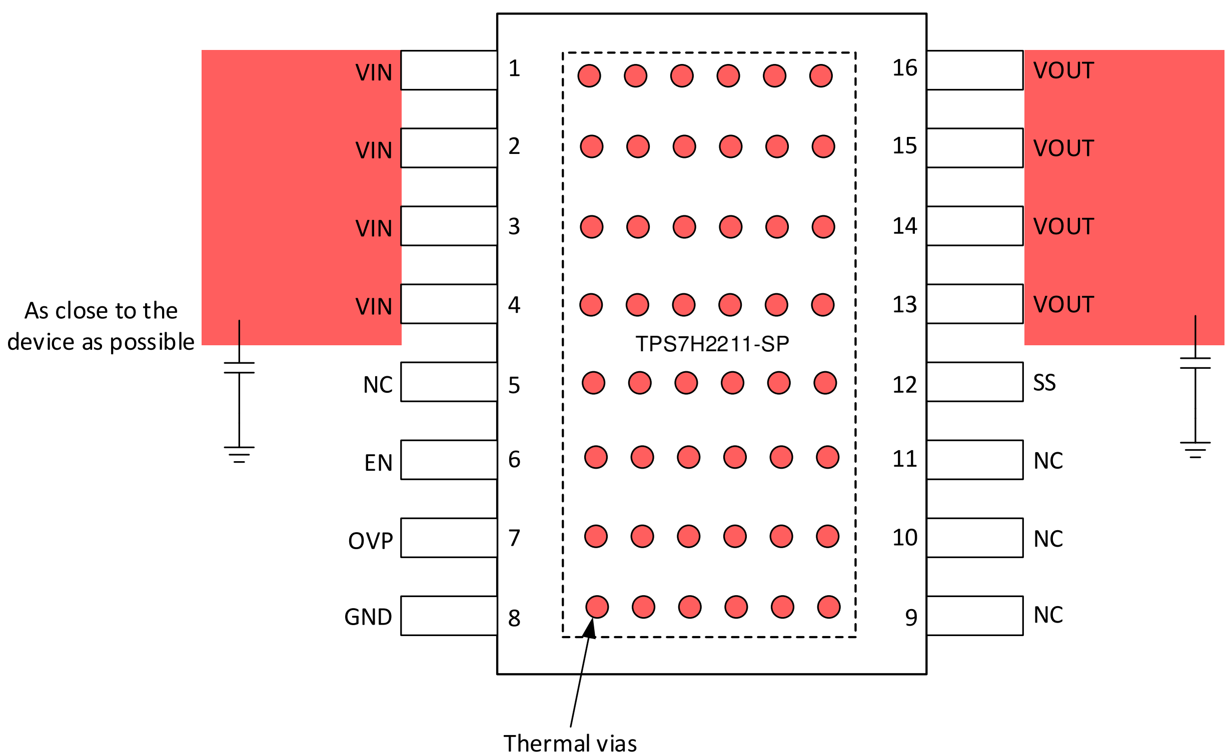


Figure 12-1. Layout Recommendation

13 Device and Documentation Support

13.1 Device Support

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H2211-SP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H2211-SP Single-Event Effects (SEE)* radiation report
- Texas Instruments, *TPS7H2211EVM-CVAL Evaluation Module* user's guide
- Texas Instruments, *Basics of Load Switches* application report
- Texas Instruments, *Basics of eFuses* application report

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1822001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962-1822001VXC TPS7H2211MHKRV	Samples
5962R1822001V9A	ACTIVE	XCEPT	KGD	0	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R1822001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1822001VXC TPS7H2211MHKRV	Samples
TPS7H2211HKR/EM	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H2211HKR/EM EVAL ONLY	Samples
TPS7H2211Y/EM	ACTIVE	XCEPT	KGD	0	5	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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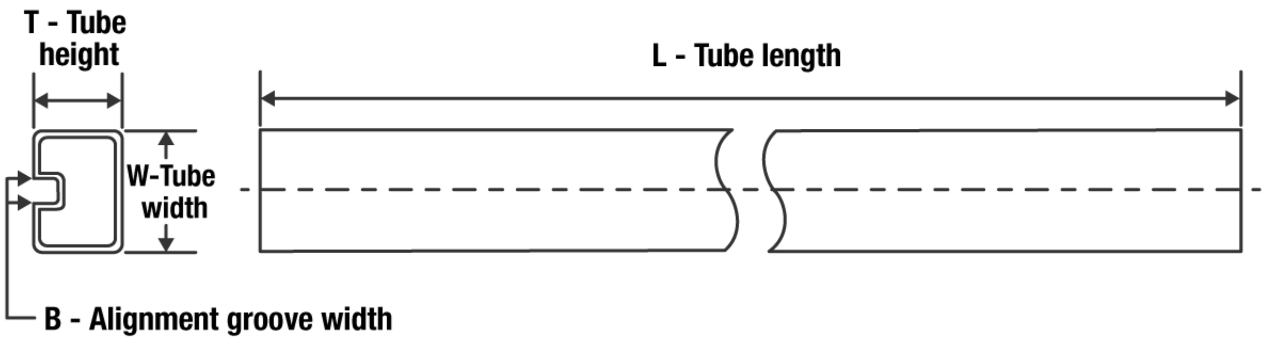
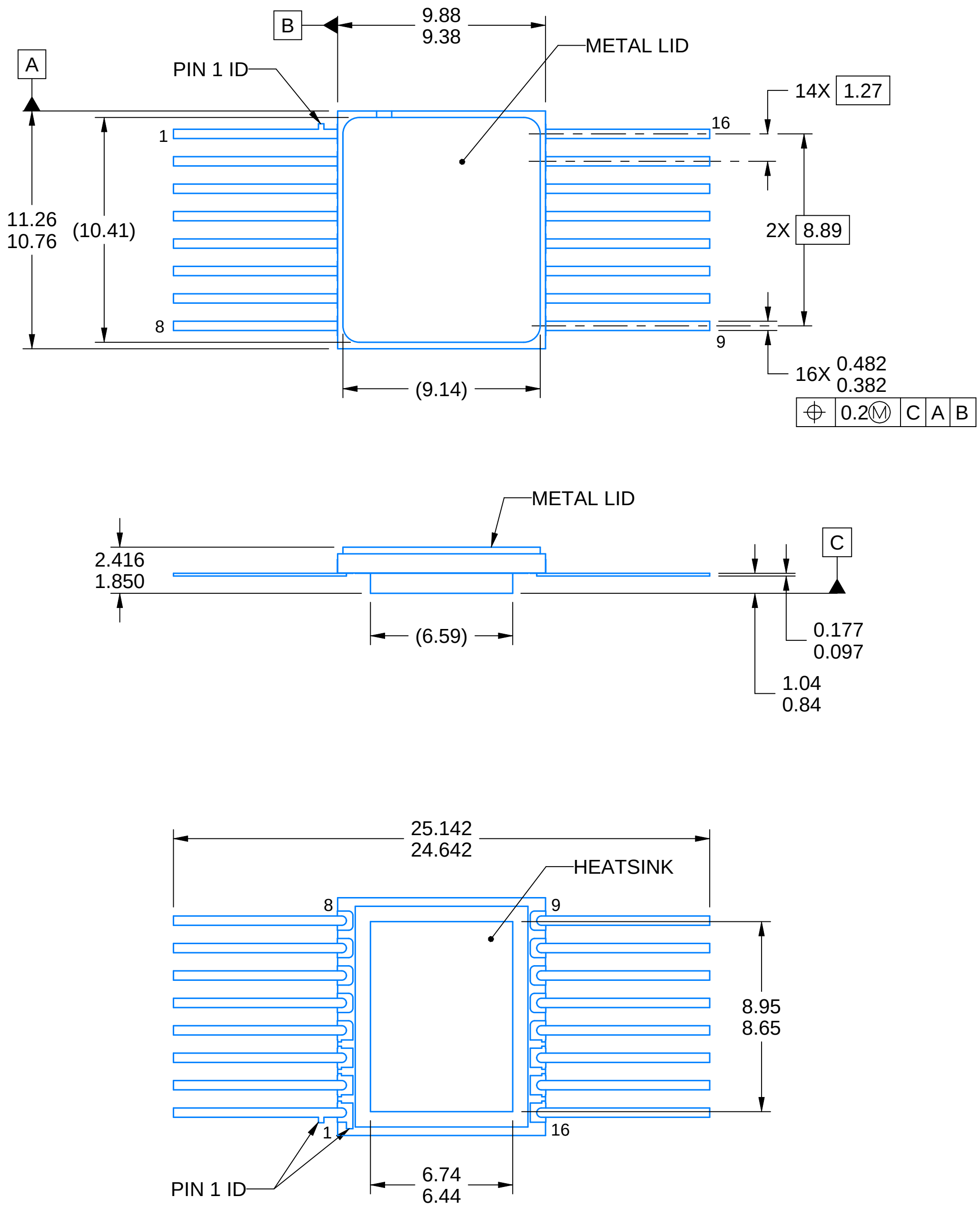
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1822001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
5962R1822001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
TPS7H2211HKR/EM	HKR	CFP	16	1	506.98	26.16	6220	NA



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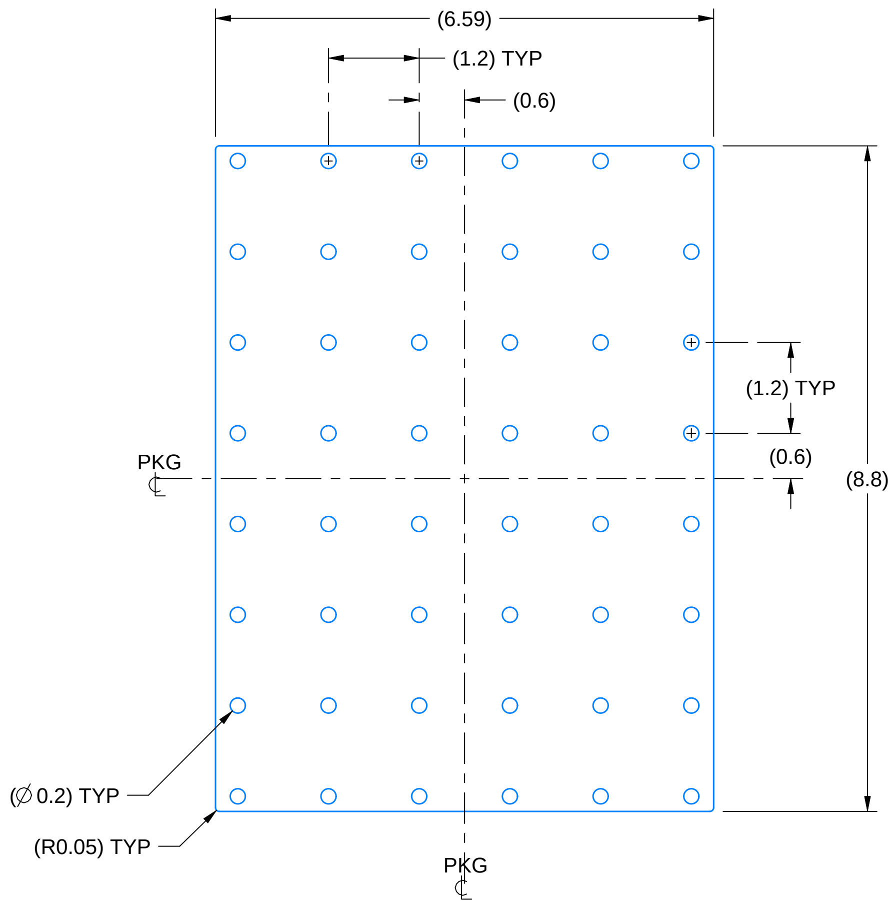
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265