

# PerFET™ Power Transistor

## FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

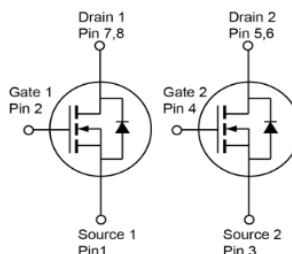
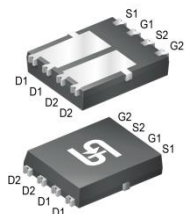
PRODUCT SUMMARY			
PARAMETER	VALUE	UNIT	
$V_{DS}$	40	V	
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	7.6	mΩ
	$V_{GS} = 4.5V$	10.6	
$Q_g$	$V_{GS} = 4.5V$	10.7	nC

## APPLICATIONS

- DC-DC Converters
- Solenoid and Motor Drivers
- Load Switch



PDFN56U Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	40	V	
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V	
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	$I_D$	65	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	$I_D$	34	A
	$T_C = 100^\circ\text{C}$		34	
	$T_A = 25^\circ\text{C}$		15	
Pulsed Drain Current	$I_{DM}$	136	A	
Single Pulse Avalanche Current (Note 2)	$I_{AS}$	17.3	A	
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	45	mJ	
Total Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	55.6	W
	$T_C = 125^\circ\text{C}$		18.5	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$	

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	2.7	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Note:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

<b>ELECTRICAL CHARACTERISTICS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$	$BV_{DSS}$	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1.4	1.8	2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 16\text{V}, V_{DS} = 0\text{V}$	$I_{GSS}$	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$	$I_{DSS}$	--	--	1	$\mu\text{A}$
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 17\text{A}$	$R_{DS(on)}$	--	6.1	7.6	m $\Omega$
	$V_{GS} = 4.5\text{V}, I_D = 17\text{A}$		--	7.7	10.6	
Forward Transconductance (Note 3)	$V_{DS} = 10\text{V}, I_D = 10\text{A}$	$g_{fs}$	--	133.3	--	S
<b>Dynamic</b>						
Total Gate Charge	$V_{GS} = 4.5\text{V}, V_{DS} = 20\text{V},$ $I_D = 15\text{A}$	$Q_g$	--	10.7	--	nC
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 15\text{A}$	$Q_g$	--	22.4	--	
Gate-Source Charge		$Q_{gs}$	--	4.3	--	
Gate-Drain Charge		$Q_{gd}$	--	3.3	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1.0\text{MHz}$	$C_{iss}$	--	1344	--	pF
Output Capacitance		$C_{oss}$	--	248	--	
Reverse Transfer Capacitance		$C_{rss}$	--	15	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	--	1.7	--	$\Omega$
<b>Switching</b> (Note 4)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 15\text{A}, R_G = 3.3\Omega$	$t_{d(on)}$	--	7.3	--	nS
Rise Time		$t_r$	--	50.1	--	
Turn-Off Delay Time		$t_{d(off)}$	--	23.6	--	
Fall Time		$t_f$	--	5.6	--	
<b>Source-Drain Diode</b>						
Diode Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 17\text{A}$	$V_{SD}$	--	--	1.1	V
Reverse Recovery Time	$I_S = 15\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	--	29.4	--	nS
Reverse Recovery Charge		$Q_{rr}$	--	20	--	nC

**Notes:**

- Package current limit.
- $L = 0.3\text{mH}, V_{GS} = 10\text{V}, R_G = 25\Omega,$  Starting  $T_J = 25^\circ\text{C}.$
- Pulse test: Pulse Width  $\leq 300\mu\text{s},$  duty cycle  $\leq 2\%.$
- Switching time is essentially independent of operating temperature.

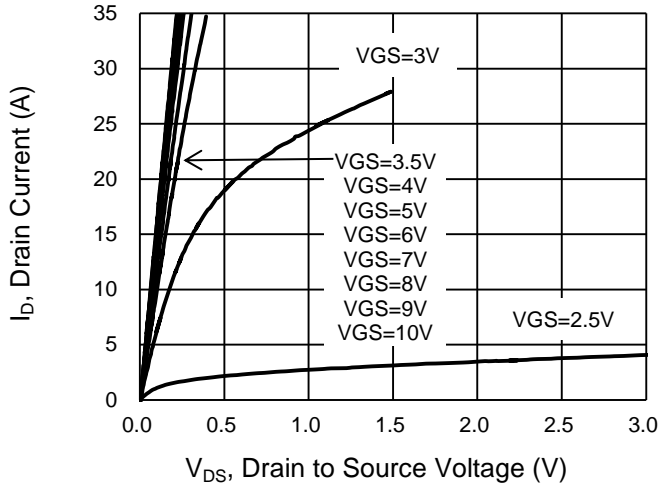
**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TSM076NH04LDCR RLG	PDFN56U Dual	2,500pcs / 13" Reel

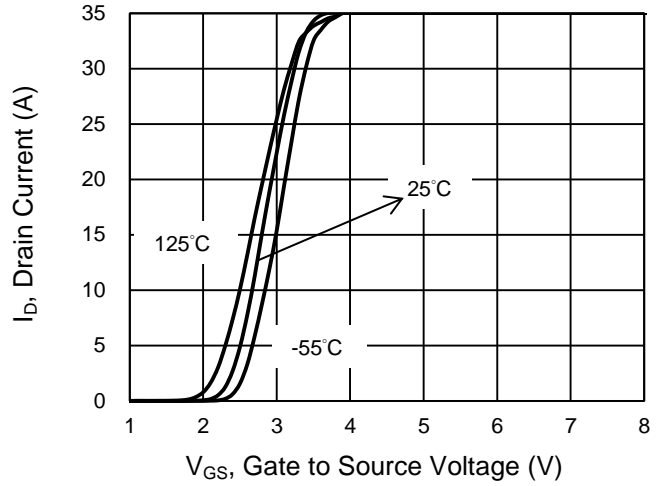
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

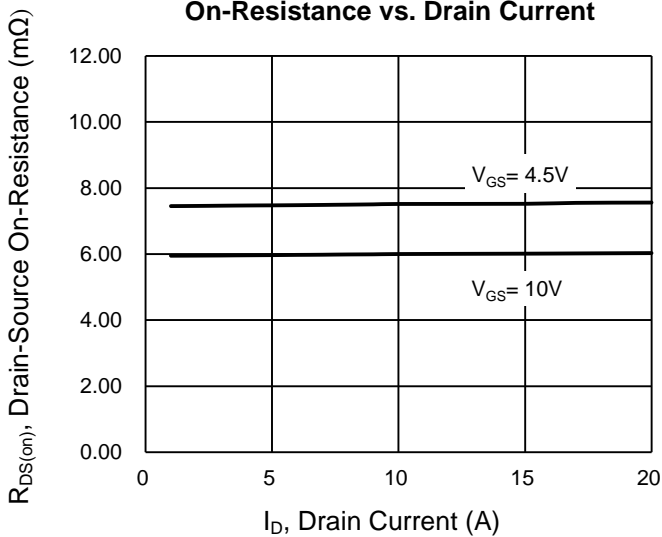
**Output Characteristics**



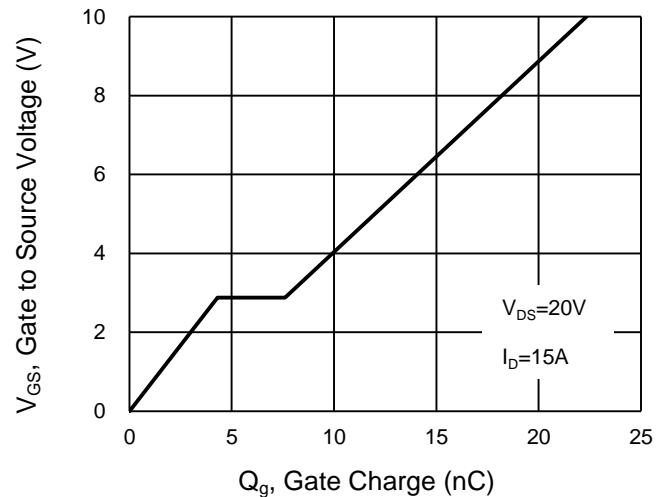
**Transfer Characteristics**



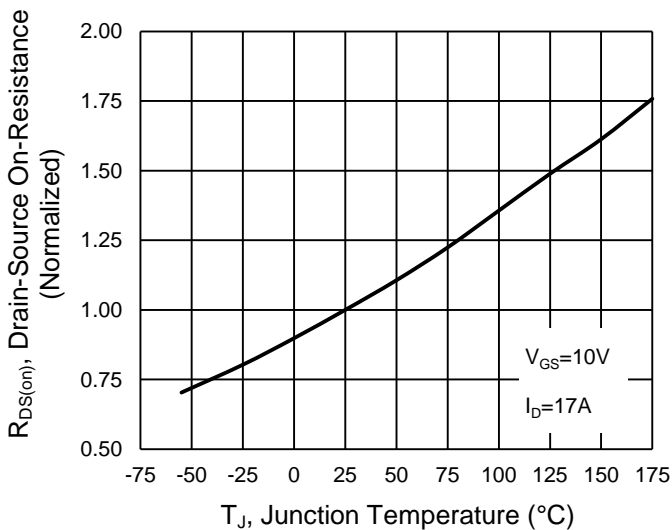
**On-Resistance vs. Drain Current**



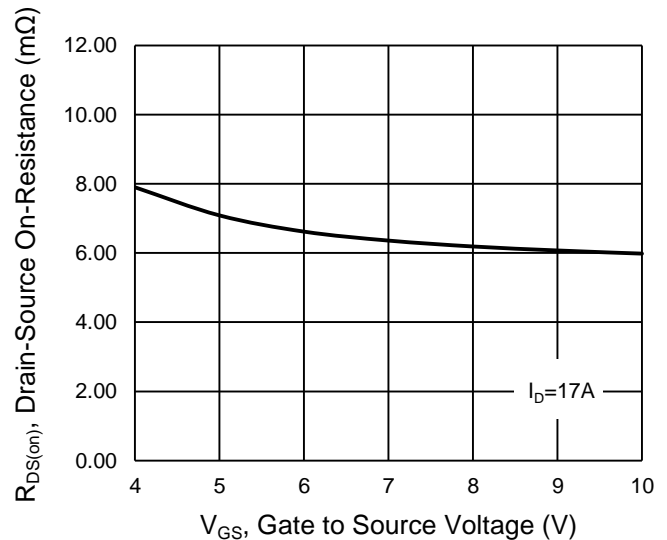
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**

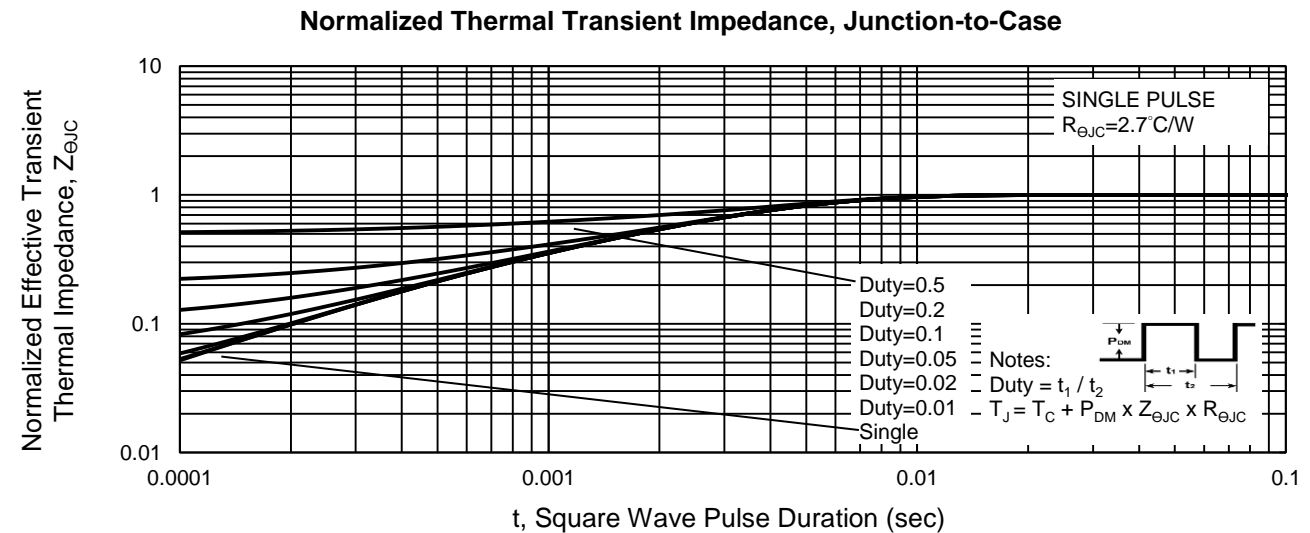
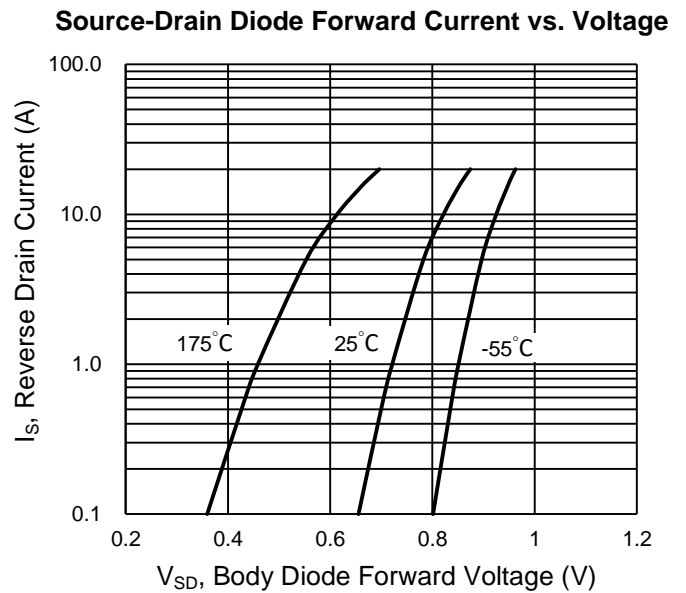
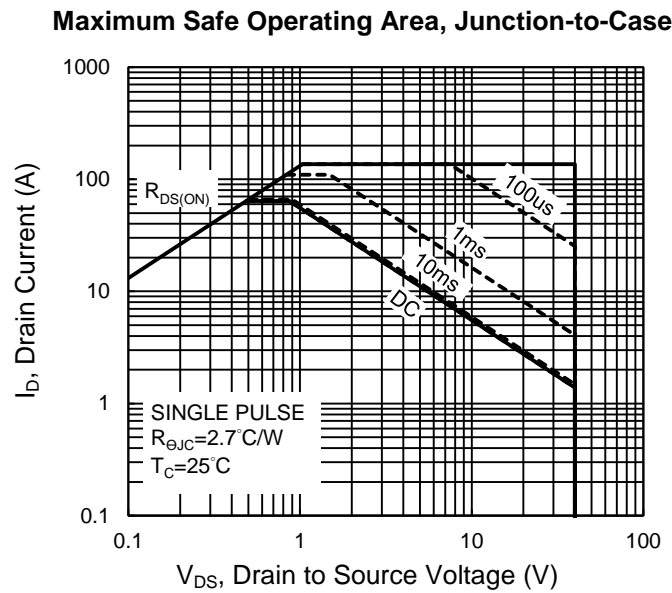
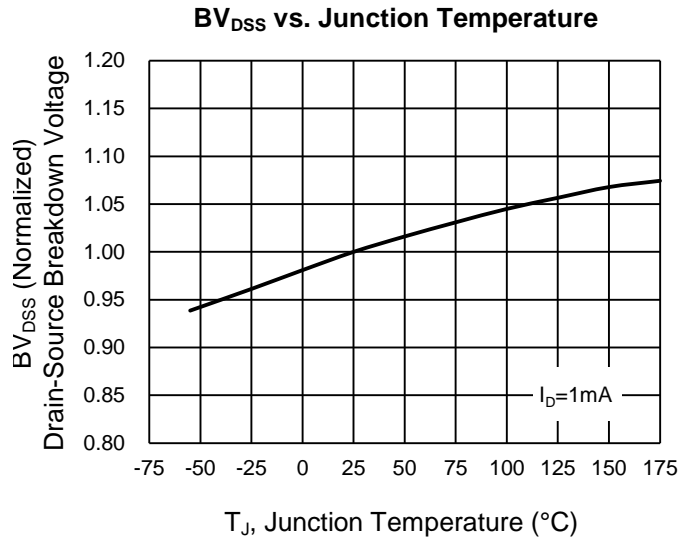
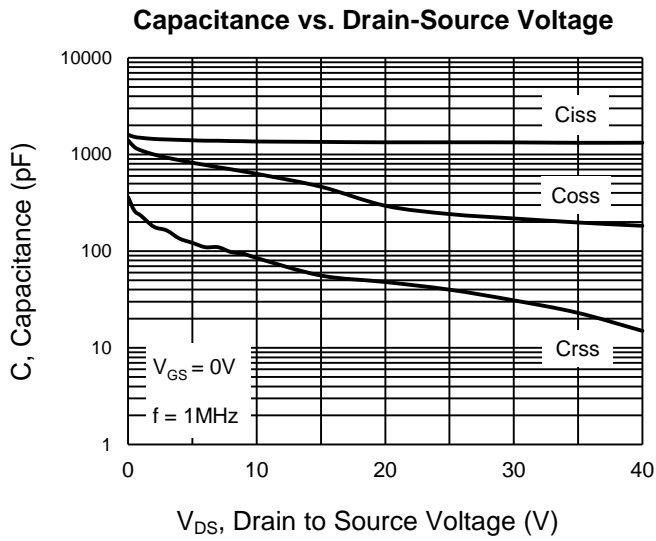


**On-Resistance vs. Gate-Source Voltage**



**CHARACTERISTICS CURVES**

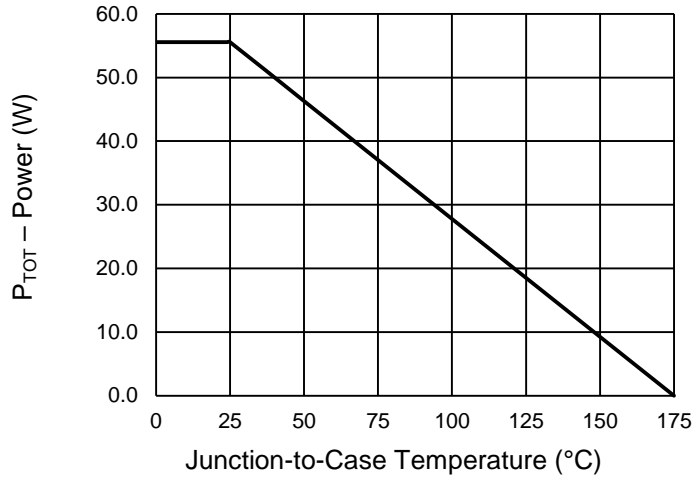
( $T_A = 25^\circ\text{C}$  unless otherwise noted)



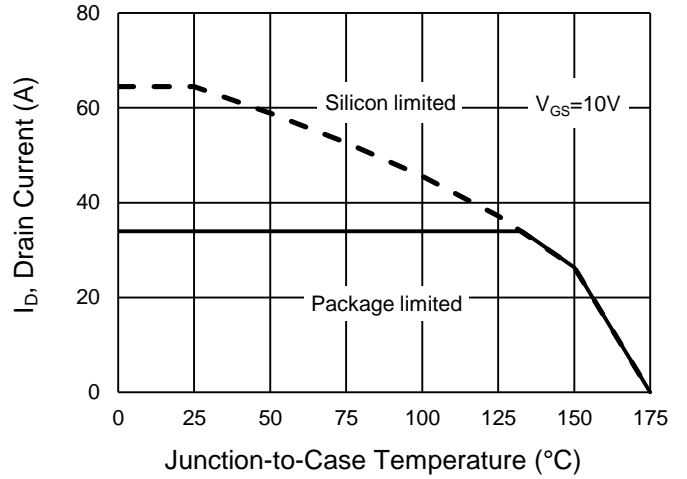
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

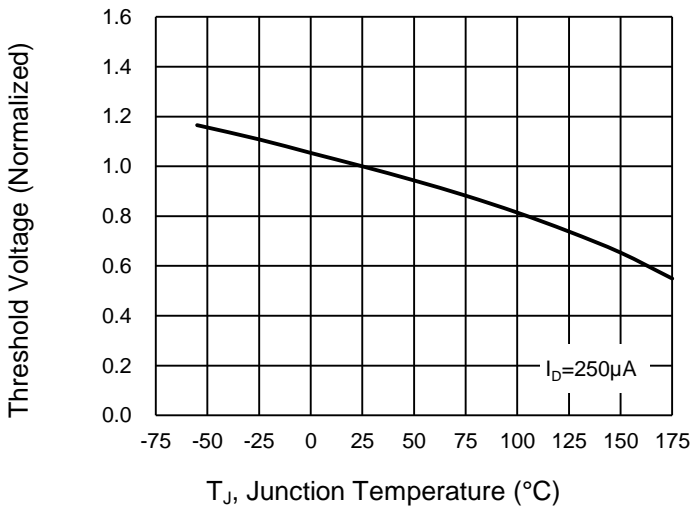
**Power Dissipation**



**Drain Current**

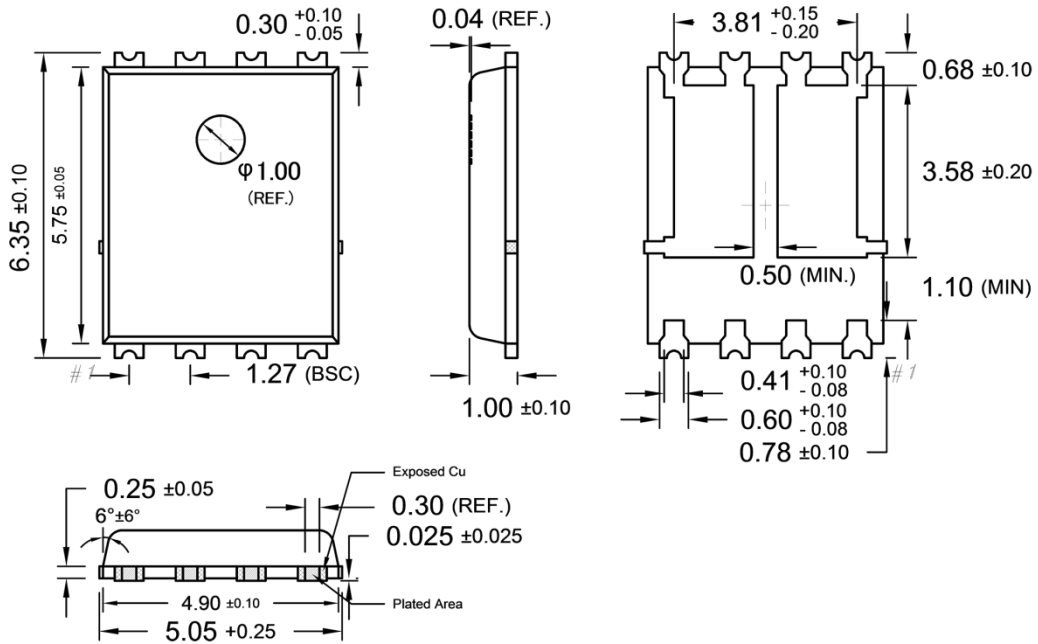


**Normalized gate threshold voltage vs Temperature**

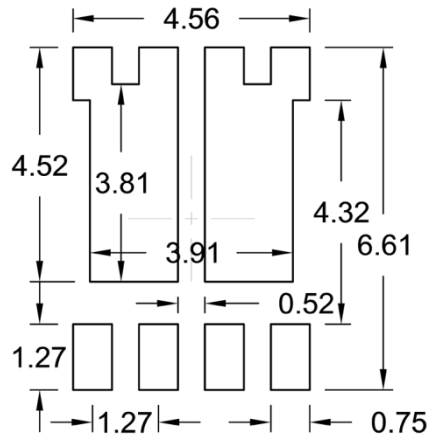


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

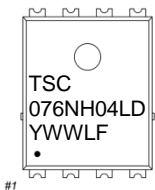
**PDFN56U Dual**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



**MARKING DIAGRAM**



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9,A~Z)
- F** = Factory Code

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