# Si30xxPPT-EVB

## EVALUATION BOARD FOR THE Si30XX

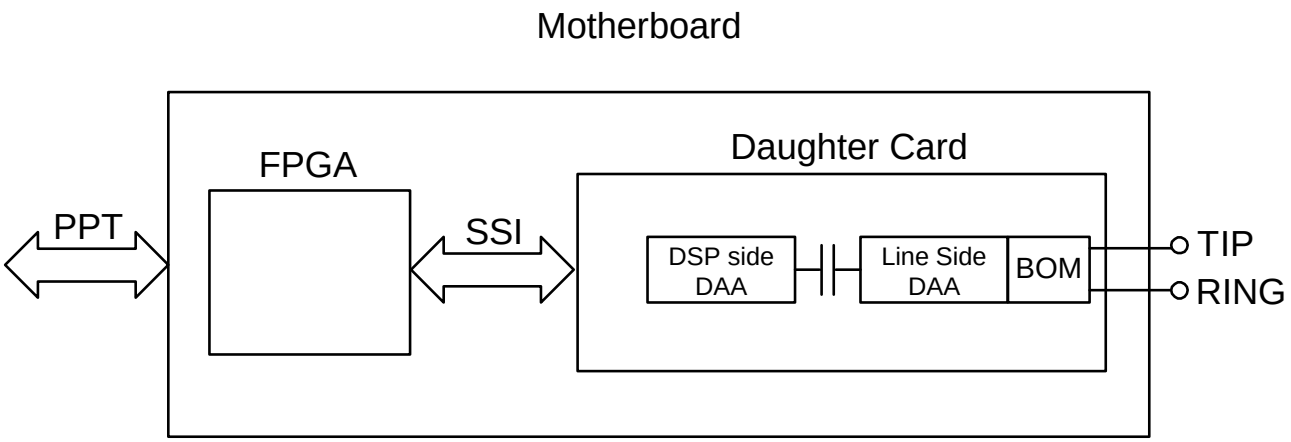
### Description

The Si30xxPPT-EVB provides the telecommunications system engineer an easy way to evaluate the functionality of Silicon Laboratories' Si30xx (Si3034, Si3035, Si3044, Si3056/18, and Si3056/19) integrated voice direct access arrangement (DAA) solution. The digital side of the chipset (Si3021 or Si3056) has a DSP serial interface as well as system-side DAA functionality. In conjunction with the Si3012/14/15 or Si3018/19 global line-side silicon DAA chip, it provides a low-cost, solid-state, globally-compliant voice DAA solution. The Si30xx chipset can be easily controlled from a PC using the supplied application software (requires software Rev 2.0 or above and FPGA Rev 2.0 or above).

### Features

- Ability to read and write DAA registers
- DAC waveform generation from a series of standard waveforms or from a .wav file
- ADC data capture and display in either time or frequency domain
- Recommended layout for key components
- Daisy-chain support

### Functional Block Diagram



## Functional Description

The Si30xxPPT-EVB provides the telecommunications system engineer an easy way to evaluate the Si30xx solution. Silicon Labs' DAAs are integrated direct access arrangements that provide a digital, low-cost, solid-state interface to worldwide telephone lines. Through the patented ISOcap technology, the Si30xx eliminates the need for an analog frond end (AFE), an isolation transformer, relays, opto-isolators, and a 2 to 4-wire hybrid.

The Si30xxPPT-EVB also supports the connection of multiple devices on an SSI interface. The evaluation board provides a straightforward means of evaluating this feature.

The evaluation board consists of the Si30xxPPT-EVB Si-LINK (mother) board and the Si30xxDC_EVB daughter card. A custom ribbon cable is also provided to connect to the parallel port of a PC. Contact a Silicon Laboratories representative for more information.

### Motherboard-Daughter Card Connection

The Si30xxDC-EVB connects to the Si30xxPPT-EVB through two sockets: JP1 and JP2. JP1 is a 3x8 socket connection to the digital signals of the DSP-side chip, as well as to the analog AOUT pin. In addition, a 3.3 V regulated supply is routed to this socket and supplies the power to the digital-side device. JP1 of the daughter card connects to JP2 of the Si30xxPPT-EVB. JP2 is a 2x5 socket connection from the TIP and RING and chassis ground of the line interface to the line-side device. JP2 of the Si30xx DC-EVB connects to JP1 of the Si30xx PPT EVB.

### Power Supply

Power is supplied to the EVB by means of J3 or J4. J3 is a euroblock header that allows for connection to a bench power supply. J4 is a 2.1 mm power jack that allows the use of a wall transformer. A 9 V supply/ 300 mA is typically used, but the onboard voltage regulator also works with a dc voltage between 7.5 V and 20 V. A diode bridge is used to correct polarity. The on-board regulator, U7, provides 5 V to the call progress circuit, the on-board oscillator, and other boards daisy chained to the Si30xxPPT-EVB. This 5 V is further regulated to 3.3 V to power the daughter card and the input/output ports of the FPGA. A third regulator provides 2.5 V for the core voltage of the FPGA.

### Clock Generation

The Si30xx requires an MCLK input. An on-board oscillator (Y1) is used by the FPGA to clock all the subsystems as well as generate and provide the master clock to the DAA. The FPGA is designed to use a 18.432 MHz oscillator (included with the board).

### Optional Call Progress Speaker

The AOUT pin of the digital-side device provides a call monitoring feature. U3 provides 25 dB of signal gain on this output. The AOUT pin has an output impedance of 10 kW. R9 and R10 form a voltage divider that provides a gain of –24.4 dB. This divider is necessary so the LM386, which is operating from a +5 V supply, is not overdriven. The LM386 is a cost-effective low-power amplifier capable of driving many different buzzers or speakers. In the case of cascaded evaluation boards, the AOUT signal is local to each board.

### Reset Circuit

The Si30xx requires an active low pulse on RESET following powerup and whenever all registers need to be reset. For development purposes, the Si30xxPPT-EVB includes a reset push button, SW1, that is used by the FPGA to generate a reset pulse of the DAA.

If multiple boards are cascaded together, the reset signal should be generated by the master board. Using the SW1 pushbutton on slave boards does not reset that slave board.

### Serial Modes

The Si30xx supports several different serial modes for a glueless interface to many standard DSP and ASIC serial ports. The serial mode of the Si30xx can be selected by JP3 and JP4.

### Line Connection

J1 is provided to connect the EVB to a standard RJ-11 connector. The system cannot execute an off-hook command without the phone line connected. This condition can be detected by examining the FDT bit of register 12 or by simply observing that there is no dial tone on the DSP or ASIC.

### PC Parallel Port

JP13 connects through the Silicon Labs custom ribbon cable to the parallel port of the PC. The parallel port connection allows the designer to read and write the DAA register using the evaluation software included with the Si30xxPPT-EVB.

## Configuring the Si30xxPPT-EVB

The S30xxPPT-EVB is used to interface the Si30xx chipset to a PC or other audio system for easy evaluation. It uses an FPGA to translate the parallel port interface to the SSI bus to communicate to the Si30xx. The audio data and control data are communicated from the controlling PC using the aforementioned software. This mode allows the user to evaluate the DAA without any lab equipment other than a PC.

When in mode 0, the negative edge of FSYNC indicates the starting of the frame, and FSYNC is low until the end of data transfer. By selecting mode 1 operation, the rising edge of FSYNC indicates the start of the frame, but is only high for one cycle. To evaluate the Si30xx's multiple device operation, chain the slave boards with JP3 and JP4 set to mode 2. See Table 1 for a description of these operating modes.

**Table 1. Mode Configuration**

| Mode | M1 | M2 | Description |
|---|---|---|---|
| 0 | 0 | 0 | FSYNC frames data |
| 1 | 0 | 1 | FSYNC pulse starts data frame |
| 2 | 1 | 0 | Slave mode |
| 3 | 1 | 1 | Reserved |

The Si30xxPPT-EVB has the ability to interface in two different modes of the SSI bus: 5-bit address space operation is used for the Si3034/35/44, and 7-bit address space operation is used for the Si3056. Table 2 shows how to configure the Si30xxPPT-EVB to operate in a desired SSI operational mode.

**Table 2. SSI Operational Mode Configuration**

| Mode | Sel0 | Description |
|---|---|---|
| 5-bit Addr | 0 | For Si3021 digital side |
| 7-bit Addr | 1 | For Si3056 digital side |

## Evaluation Software

The Si30xxPPT-EVB includes an easy-to-use graphical interface for controlling the evaluation platform. This software allows the system designer to characterize the Si30xx DAA performance without constructing any custom hardware. The evaluation software includes the following features:

- Ability to read and write DAA registers using the SSI bus
- DAC waveform generation from a series of standard waveforms or from a .wav file
- ADC data capture and display in either time or frequency domain using the SSI bus
- Daisy-chain support
- Transmit and receive path attenuation and gain settings
- Ring detection
- Loop current measurement

### PC System Requirements

The application software for the Si30xxPPT-EVB has the following system requirements:

- Windows98 or Windows2000
- Available parallel port
  - EPP or ECP parallel port mode for Windows 98
  - EPP parallel port mode for Windows 2000
- 450 MHz Pentium II or greater recommended
- 64 MB of memory or greater recommended

### Installation

The supplied CD contains the Si30xxPPT-EVB windows driver files as well as a setup utility for installing the evaluation software.

To install the Si30xxPPT-EVB software, run the installation program on the "Silicon Laboratories Wireline Software CD." The path for the installation program is Si30xx Evaluation Software\setup.exe. The installer guides the user through the installation process for Si30xxPPT-EVB.exe and the LabVIEW Run-Time engine.

## Using the Si30xxPPT-EVB Application Software

A shortcut for starting the application software that controls the Si30xxPPT-EVB is installed in the Windows Start Menu under the Programs folder in the "Si30xx Evaluation Software" folder.

### Application Menus

Three pulldown menus are used to configure the operation of the software:

- **Run**:
  - Exit: Stops the program
  - Save: Stores the audio waveform into .wav files
- **Configure**:
  - Configure DAA: Display hardware status and user configuration. User can set advanced software options.
  - Reset DAA: Resets DAA and executes basic initialization sequences on Reg 1, Reg 6–10, and Reg 14.
- **Design Tool**
  - Register Map: Displays Register Map of Si30xx
  - Signal Flow Diagram: Displays Signal Flow Diagram of Si30xx.
  - Transhybrid Loss Calculation: Calculate transhybrid loss over frequency
  - Ringing: Helps user program ring validation registers.
- **Help**: Displays information about the evaluation board

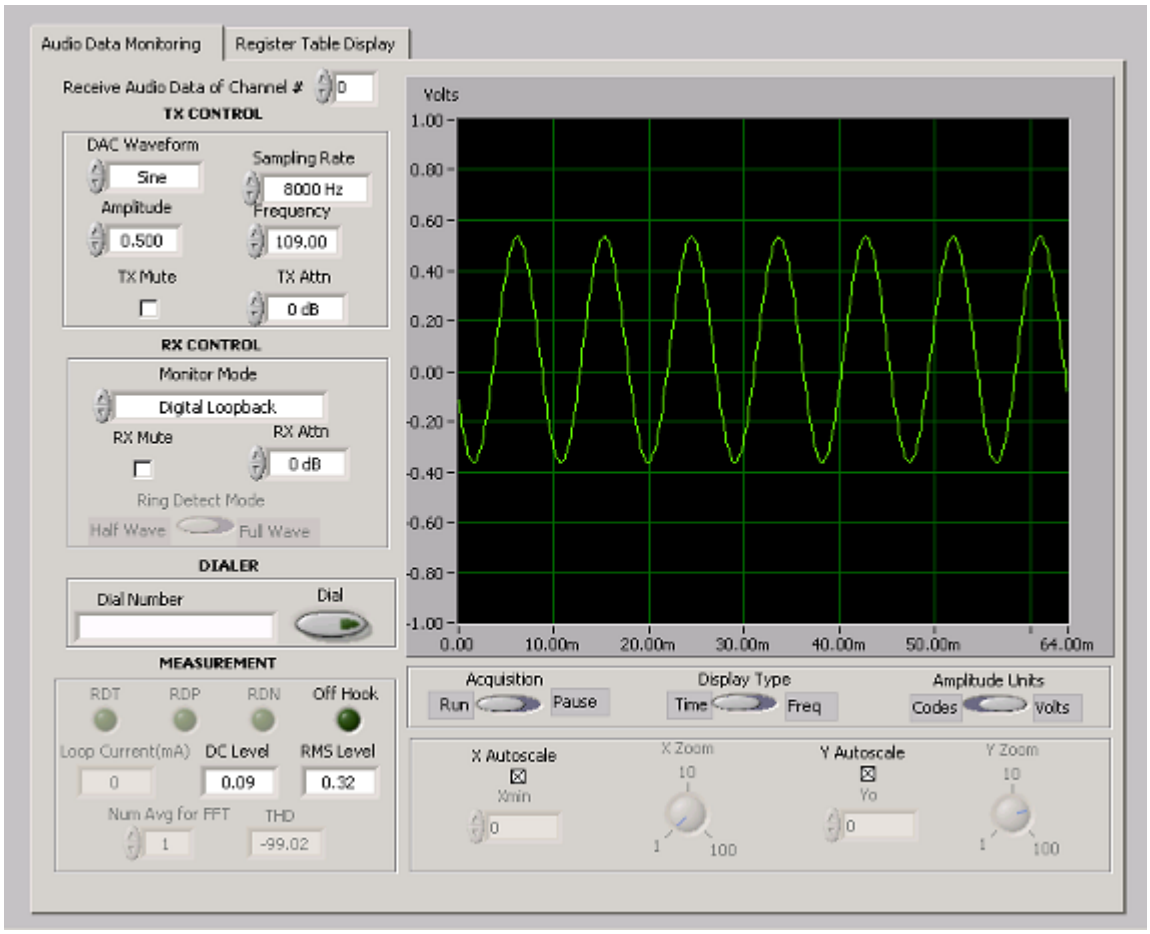



**Figure 1. Si30xxPPT-EVB Evaluation Software in the Audio Data Monitoring View**

## Audio Data Monitoring View

The audio data monitoring view is discussed in the following sections.

**Receive Audio Data of Channel#**

Allows selection of channel to control and view. The Audio Data Monitoring view allows the generation of DAC data and the capture and display of ADC data. Operation of the front panel in Line Monitoring view is detailed in the following list. See Figure 1.

**TX Control**

- **DAC Waveform**: Selects the waveform to be generated by the DAC. The waveform types are as follows: dc, Sine, Square, Ramp, and .wav file.
- **TX Gain (dB)**: Selects the transmit path gain/ attenuation.
- **TX Mute:** Mutes the transmit path.
- **Sampling Rate:** Sets the sampling rate of the DAA and performs writes to corresponding registers.
- **Amplitude**: Sets the amplitude of the DAC waveform in either volts or the units of DAC codes. The units are determined by the Amplitude Units control.
- **Frequency**: Selects the frequency (Hz) of the waveform to generate. The actual waveform frequency may vary slightly from the entered value. This variation is due to the requirement to fit an integer number of samples into the transmit buffer. The control is updated to reflect the actual waveform frequency generated. The equation for calculating the frequency of the waveform is as follows:

  Actual Frequency = round ((Waveform Frequency/DAC Sample Rate) x BufferSize) x (DAC Sample Rate/ BufferSize)

**RX Control**

- **Monitor Mode**: Allows the selection of several data modes. Digital Loopback mode routes the DAC data back to the receive path. On-hook mode configures the DAA to the on-hook mode. Off-hook mode configures the DAA to the off-hook mode. On-hook line monitoring mode configures the DAA to the line monitoring state.
- **RX Gain/Attn (dB):** Selects the receive path gain/ attenuation.
- **RX Mute:** Mutes the receive path
- **Ring Detect Mode:** Allows selection of full-wave or half-wave ring detection.

**Dialer**

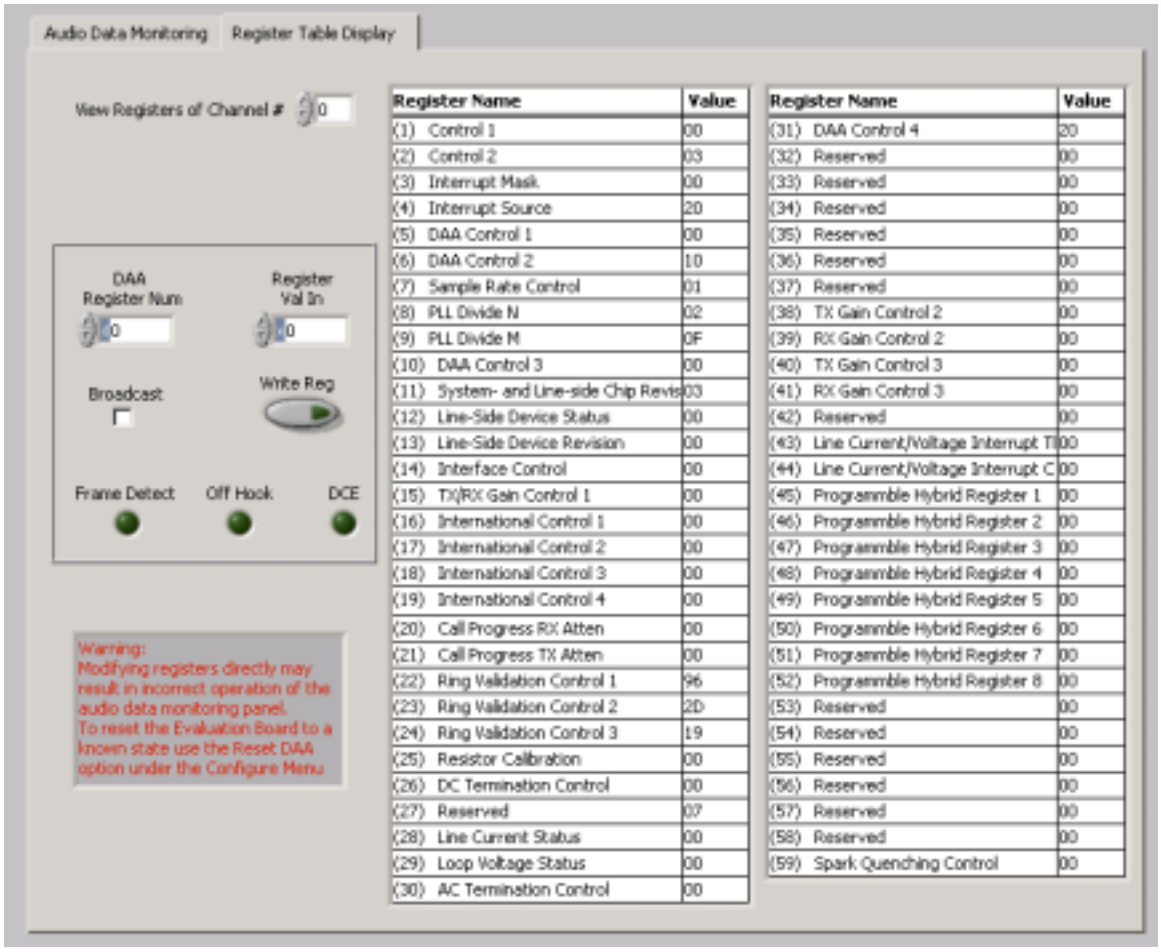
- **Dial Number:** Inputs dial number.
- **Dial:** Executes dial.

**Measurement**

- **Loop Current**: Displays the loop current when in off-hook mode.
- **Ring Detect Bits**: Displays the state of the ring detect bits when in on-hook mode.
- **Off-Hook**: Indicates that the DAA is in the off-hook state.
- **DC Level/SINAD**: Displays either the dc level of the time domain waveform or the SINAD of the frequency domain waveform.
- **RMS Level/Frequency**: Displays either the RMS level of the time domain waveform or the frequency of the largest peak in the frequency domain waveform.
- **Num Avg for FFT**: When in FFT display, the software automatically averages waveforms. This panel selects the number of averages to take.

**Wave Display Controls**

- **Display Type**: Selects how the ADC data is displayed on the Waveform Graph (time or frequency domain).
- **Amplitude Units**: Sets the amplitude units for the Waveform Graph and Amplitude control to either volts or codes.
- **Acquisition**: Used to run or pause the CODEC data stream. Upon pausing the acquisition of the data, it displays measurement values regardless of the status of “display measurement” under the configure menu.
- **X Autoscale**: Automatically scales the X-axis of the graph to fit the entire waveform.
- **Y Autoscale**: Automatically scales the Y-axis to fit the entire vertical range of the waveform.
- **Xmin**: Sets the origin of the X-axis when the X Autoscale is disabled.
- **X Zoom**: Used to zoom a portion of the displayed waveform when X Autoscale is disabled. The waveform starts at Xmin and 1/X Zoom of the total waveform is displayed.
- **Yo**: Sets the origin of the Y-axis when Y Autoscale is disabled. Half of the waveform is displayed above Yo, and half is displayed below Yo.




| Register Name | Value |
|---|---|
| (1) Control 1 | 00 |
| (2) Control 2 | 03 |
| (3) Interrupt Mask | 00 |
| (4) Interrupt Source | 20 |
| (5) DAA Control 1 | 00 |
| (6) DAA Control 2 | 10 |
| (7) Sample Rate Control | 01 |
| (8) PLL Divide N | 02 |
| (9) PLL Divide M | 0F |
| (10) DAA Control 3 | 00 |
| (11) System- and Line-side Chip Revis | 03 |
| (12) Line-Side Device Status | 00 |
| (13) Line-Side Device Revision | 00 |
| (14) Interface Control | 00 |
| (15) TX/RX Gain Control 1 | 00 |
| (16) International Control 1 | 00 |
| (17) International Control 2 | 00 |
| (18) International Control 3 | 00 |
| (19) International Control 4 | 00 |
| (20) Call Progress RX Atten | 00 |
| (21) Call Progress TX Atten | 00 |
| (22) Ring Validation Control 1 | 96 |
| (23) Ring Validation Control 2 | 2D |
| (24) Ring Validation Control 3 | 19 |
| (25) Resistor Calibration | 00 |
| (26) DC Termination Control | 00 |
| (27) Reserved | 07 |
| (28) Line Current Status | 00 |
| (29) Loop Voltage Status | 00 |
| (30) AC Termination Control | 00 |

| Register Name | Value |
|---|---|
| (31) DAA Control 4 | 20 |
| (32) Reserved | 00 |
| (33) Reserved | 00 |
| (34) Reserved | 00 |
| (35) Reserved | 00 |
| (36) Reserved | 00 |
| (37) Reserved | 00 |
| (38) TX Gain Control 2 | 00 |
| (39) RX Gain Control 2 | 00 |
| (40) TX Gain Control 3 | 00 |
| (41) RX Gain Control 3 | 00 |
| (42) Reserved | 00 |
| (43) Line Current/Voltage Interrupt T | 00 |
| (44) Line Current/Voltage Interrupt C | 00 |
| (45) Programmble Hybrid Register 1 | 00 |
| (46) Programmble Hybrid Register 2 | 00 |
| (47) Programmble Hybrid Register 3 | 00 |
| (48) Programmble Hybrid Register 4 | 00 |
| (49) Programmble Hybrid Register 5 | 00 |
| (50) Programmble Hybrid Register 6 | 00 |
| (51) Programmble Hybrid Register 7 | 00 |
| (52) Programmble Hybrid Register 8 | 00 |
| (53) Reserved | 00 |
| (54) Reserved | 00 |
| (55) Reserved | 00 |
| (56) Reserved | 00 |
| (57) Reserved | 00 |
| (58) Reserved | 00 |
| (59) Spark Quenching Control | 00 |

**Figure 2. Si3056 System-Side Device Signal Flow Diagram**

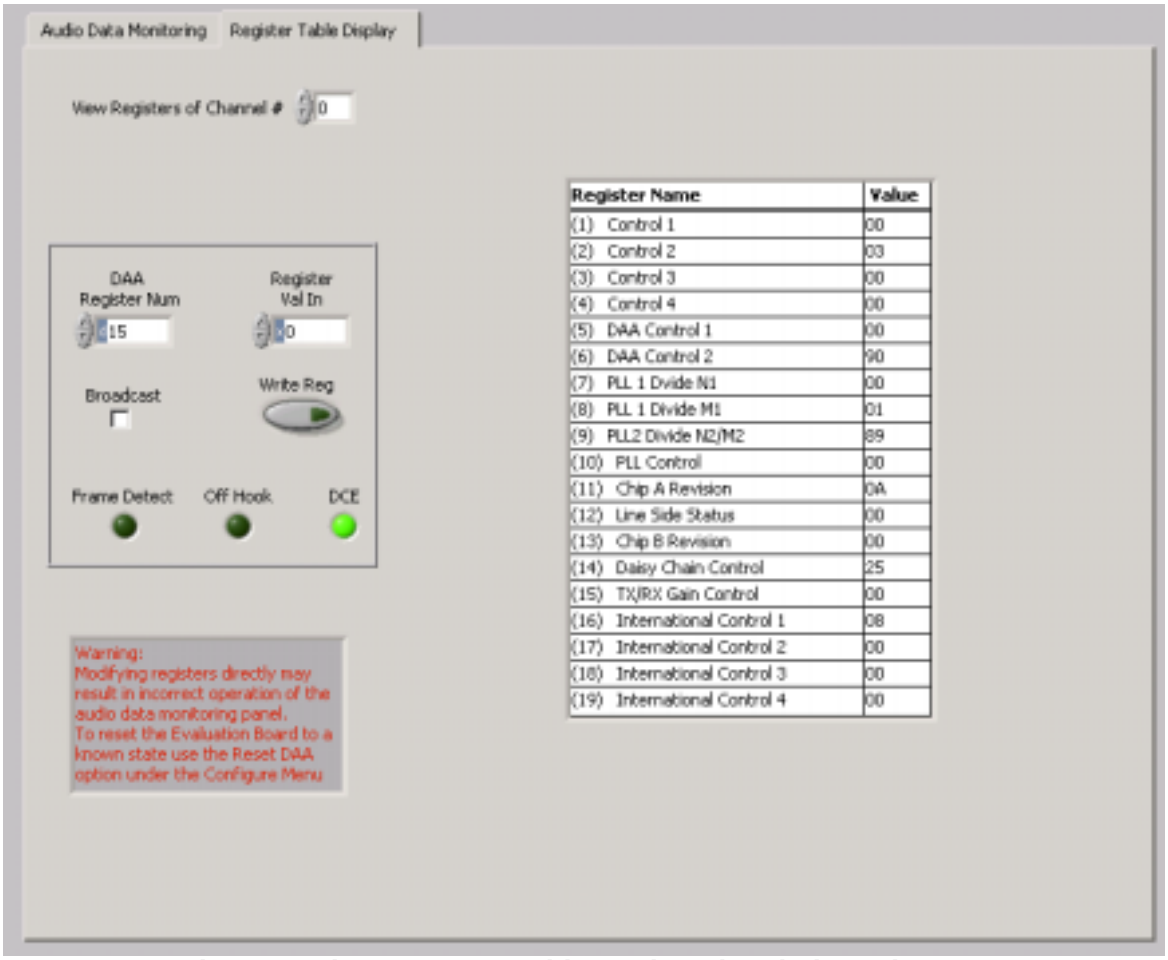



**Figure 3. Si3021 System-Side Device Signal Flow Diagram**

## Register Table Display View

The DAA Register view allows the Si30xx DAA registers to be read or written. The user interface for the DAA Register view is shown in Figure 2 for the Si3056 and Figure 3 for the Si3021. Operation of the front panel in the DAA Register view is detailed in the following list:

- **Table**: This table displays the contents of the Si30xx DAA registers in realtime.
- **DAA Reg Num**: The Si30xx DAA register number to write (in decimal).
- **DAA Reg Value**: The contents to write to the register selected by the DAA Reg Num control (in hexadecimal).
- **Write DAA Regs**: Causes the contents of the DAA Reg Value control to be written to the DAA Reg Num register.
- **Broadcast**: Turns on the broadcast bit (SPI only).
- **FDT**: Shows the status of the FDT bit, which indicates that the Si30xx is communicating with the Si3019.
- **Off-Hook**: Shows the status of the off-hook bit, DAA Register 5, bit 1.
- **DCE**: Shows the status of the daisy chain enable bit, DAA Register 14, bit 0.

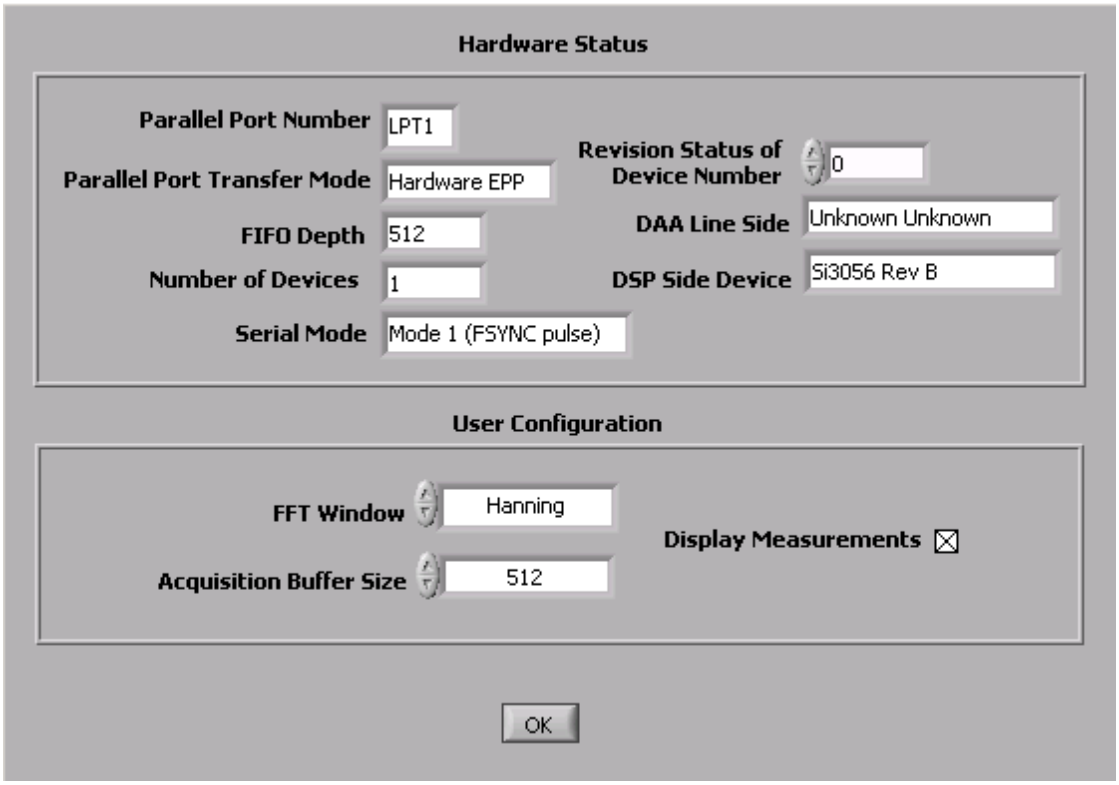



**Figure 4. Configure DAA Panel**

## Advanced Configuration

Advanced configuration of the application software is accomplished by using the “Configure DAA” selection in the “Configure” menu. The configuration panel is shown in Figure 4. The panel contents are detailed in the following list:

- **FFT Window**: The FFT window applied to the time domain data before calculating the FFT.
- **Acquisition Buffer Size**: This is the size of the buffer, in samples, that is acquired and displayed on the Line Monitoring mode waveform graph. The buffer size can be set between 1024 and 65536 samples in increments of 512 samples.
- **Display Measurement**: Takes realtime measurements of audio waveform.

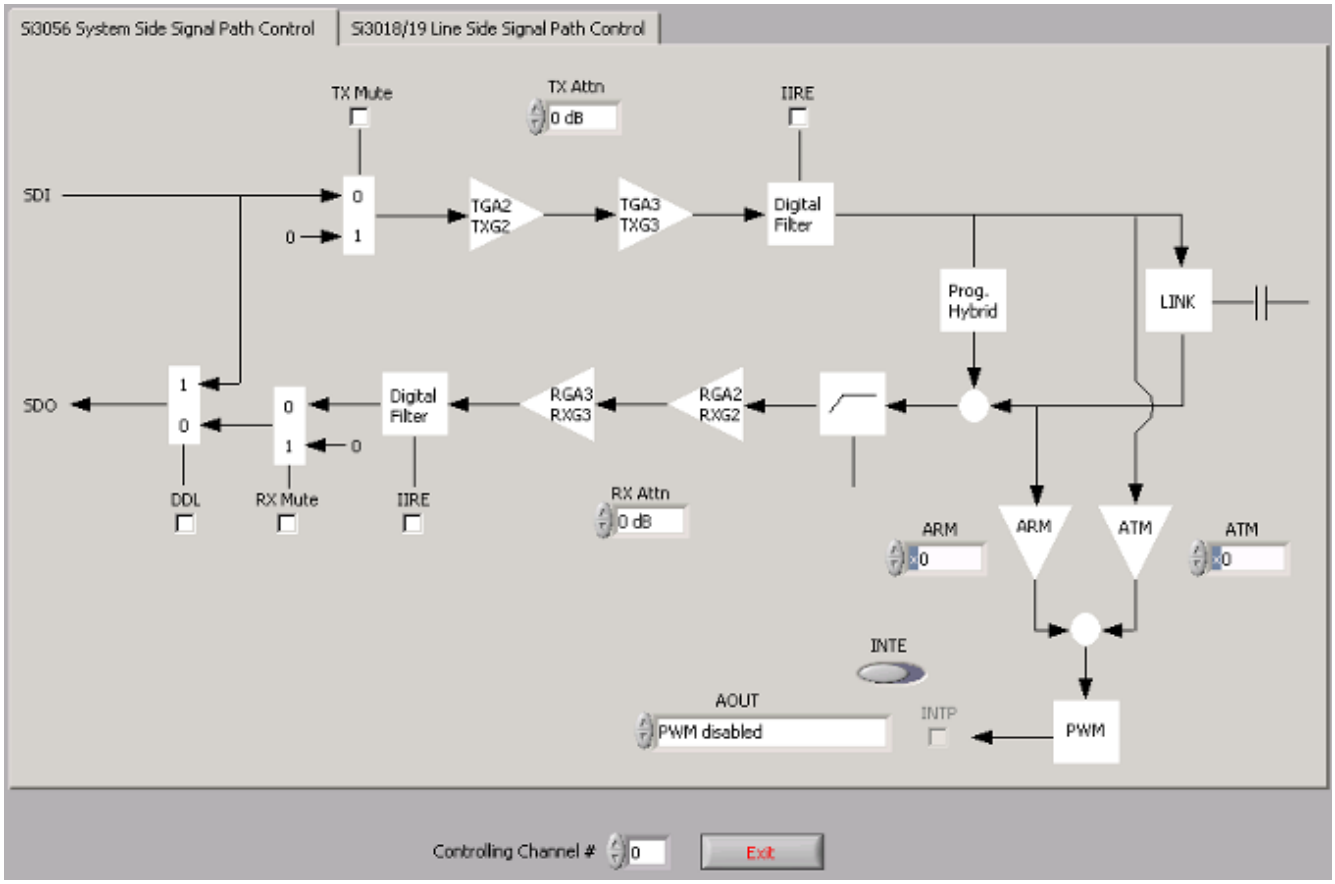



**Figure 5. Si30xx Signal Flow Diagram for the Si3056**

## Signal Flow Diagrams

The signal flow diagrams of the Si30xx application software for the Si3056 device, shown in Figure 5 and Figure 6, assist users with programming DAA.

## Si30xx Signal Path Control

- **TX Mute:** Turns on/off the TXM bit on DAA Register 15, bit 7.
- **TX Gain:** Writes to ATX on DAA Register 15 or TGA2, TXG2, TGA3, and TXG3 on DAA Register 38 and 40.
- **IIRE:** Turns on/off IIRE bit on Register 16, bit 4.
- **DDL:** Turns on/off DDL bit on Register 10, bit 1.
- **RX Mute:** Turns on/off RXM bit on Register 15, bit 0.
- **RX Gain:** Writes to ARX on DAA Register 15 or RGA2, RXG2, RGA3, and RXG3 on DAA Register 39 and 41.
- **FILT:** Turns on/off FILT bit on Register 31, bit 1 (Bit is available for Si3019 line-side device only).
- **ARM:** Writes to ARM on Register 20.
- **ATM:** Writes to ATM on Register 21.
- **INTE:** Turns on/off INTE bit on Register 2, bit 7.
- **INTP:** Turns on/off INTP bit on Register 2, bit 6.
- **AOUT:** Writes to PWMM and PWEM on Register 1.

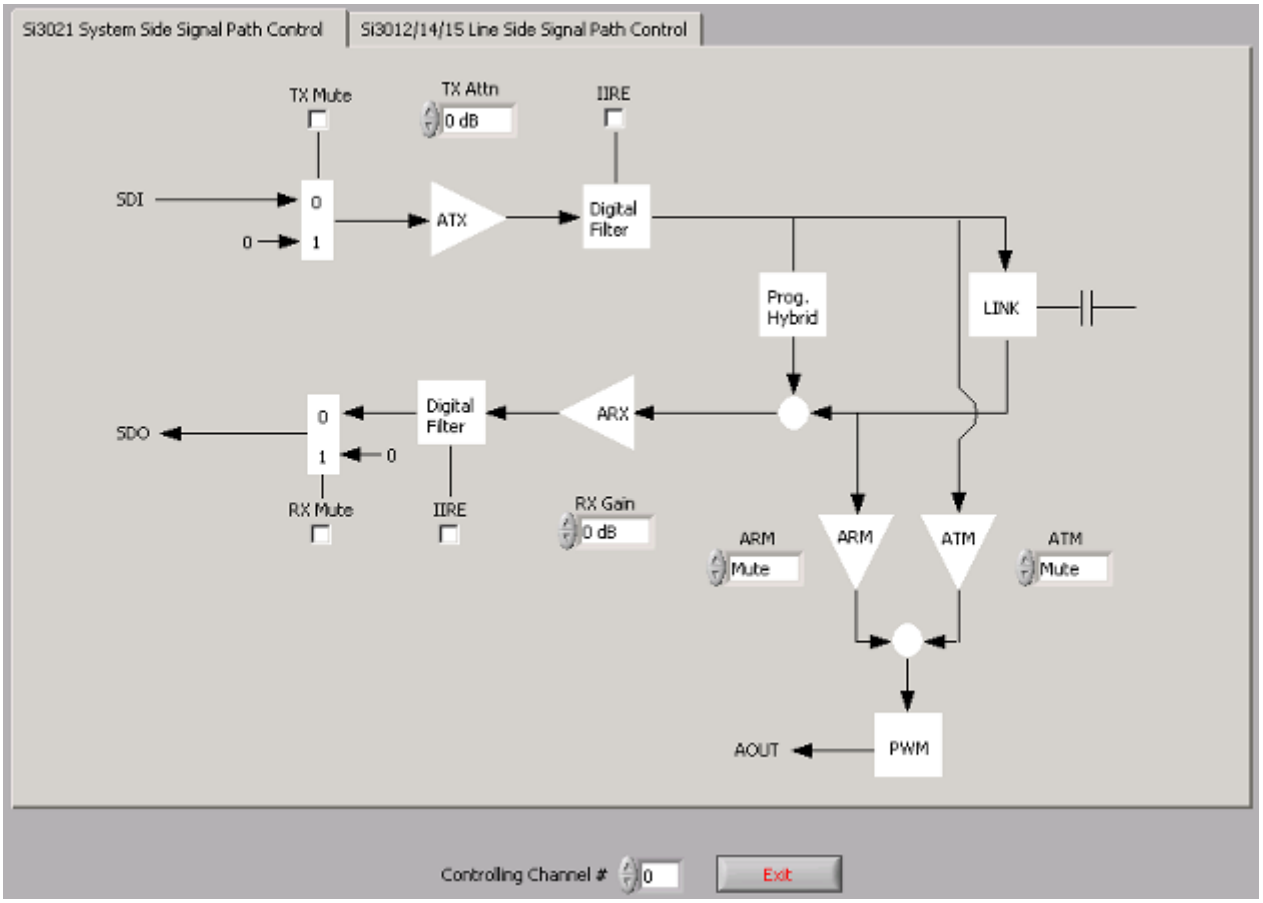



**Figure 6. Si30xx Signal Flow Diagram for Si3021**

## Signal Flow Diagrams

The signal flow diagrams of the application software shown in Figure 6 assist users with programming DAA.

## Si30xx Signal Path Control

- **TX Mute:** Turns on/off the TXM bit on DAA Register 15, bit 7.
- **TX Gain:** Writes to TGA2, TXG2, TGA3, and TXG3 on DAA Register 38 and 40.
- **IIRE:** Turns on/off IIRE bit on Register 16, bit 4.
- **RX Mute:** Turns on/off RXM bit on Register 15, bit 0.
- **RX Gain:** Writes to RGA2, RXG2, RGA3, and RXG3 on DAA Register 39 and 41.
- **ARM:** Writes to ARM on Register 20.
- **ATM:** Writes to ATM on Register 21.
- **AOUT:** Writes to PWMM and PWEM on Register 1 Si3019 Signal Path Control.

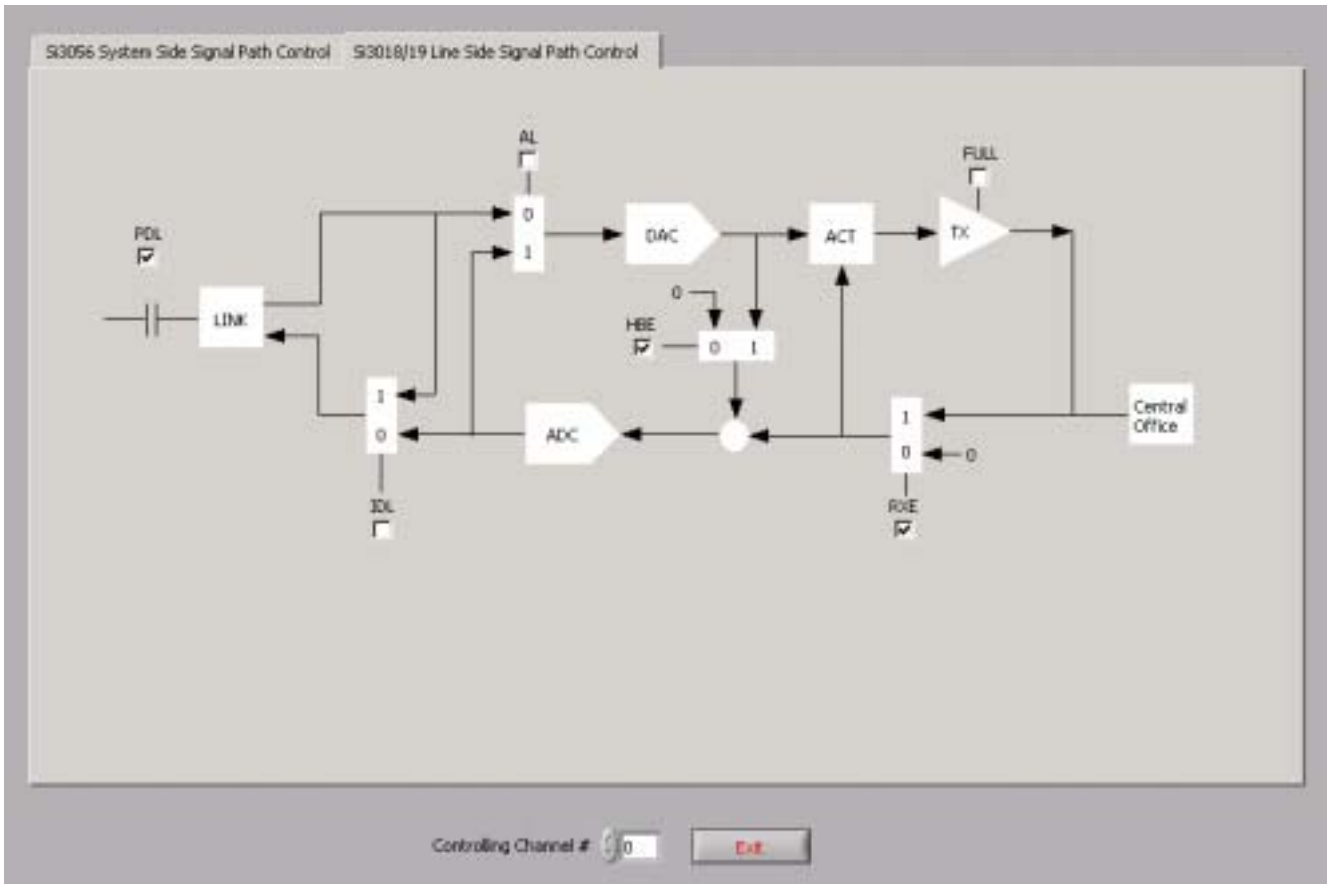



**Figure 7. Si3018/19 Line-side Device Signal Flow Diagram**

## Line-Side Device Signal Path Control

- AL: Turns on/off AL bit on Register 2, bit 3.
- HBE: Turns on/off HBE bit on Register 2, bit 1.
- RXE: Turns on/off RXE bit on Register 2, bit 0.
- IDL: Turns on/off IDL bit on Register 1, bit 1.

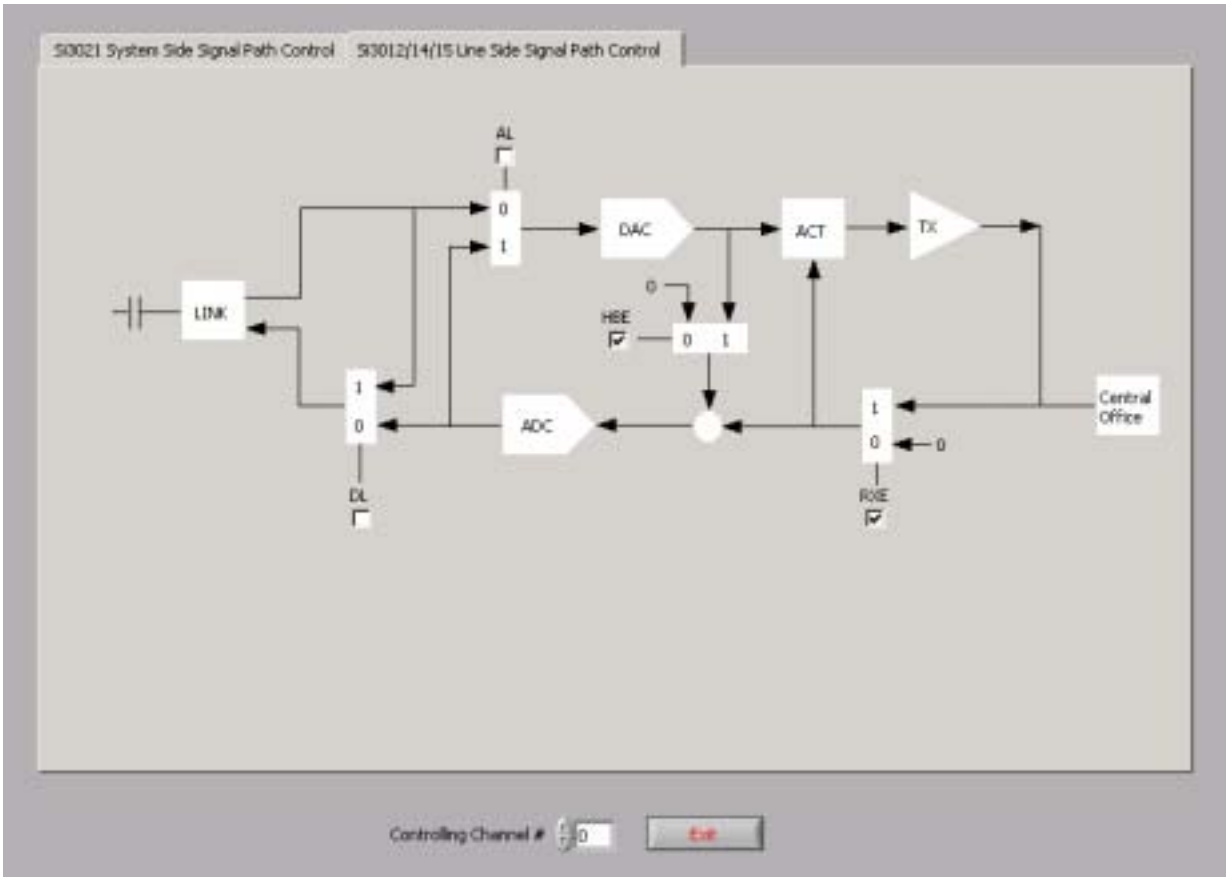



**Figure 8. Si3012/14/15 Line Side Device Signal Flow Diagram**

## Line-Side Device Signal Path Control

- AL: Turns on/off AL bit on Register 2, bit 3.
- HBE: Turns on/off HBE bit on Register 2, bit 1.
- RXE: Turns on/off RXE bit on Register 2, bit 0.
- IDL/DL: Turns on/off IDL/DL bit on Register 1, bit 1.
- PDL: Turns on/off PDL bit on Register 6, bit 4.
- FULL: Turns on/off FULL bit on Register 31, bit 7.

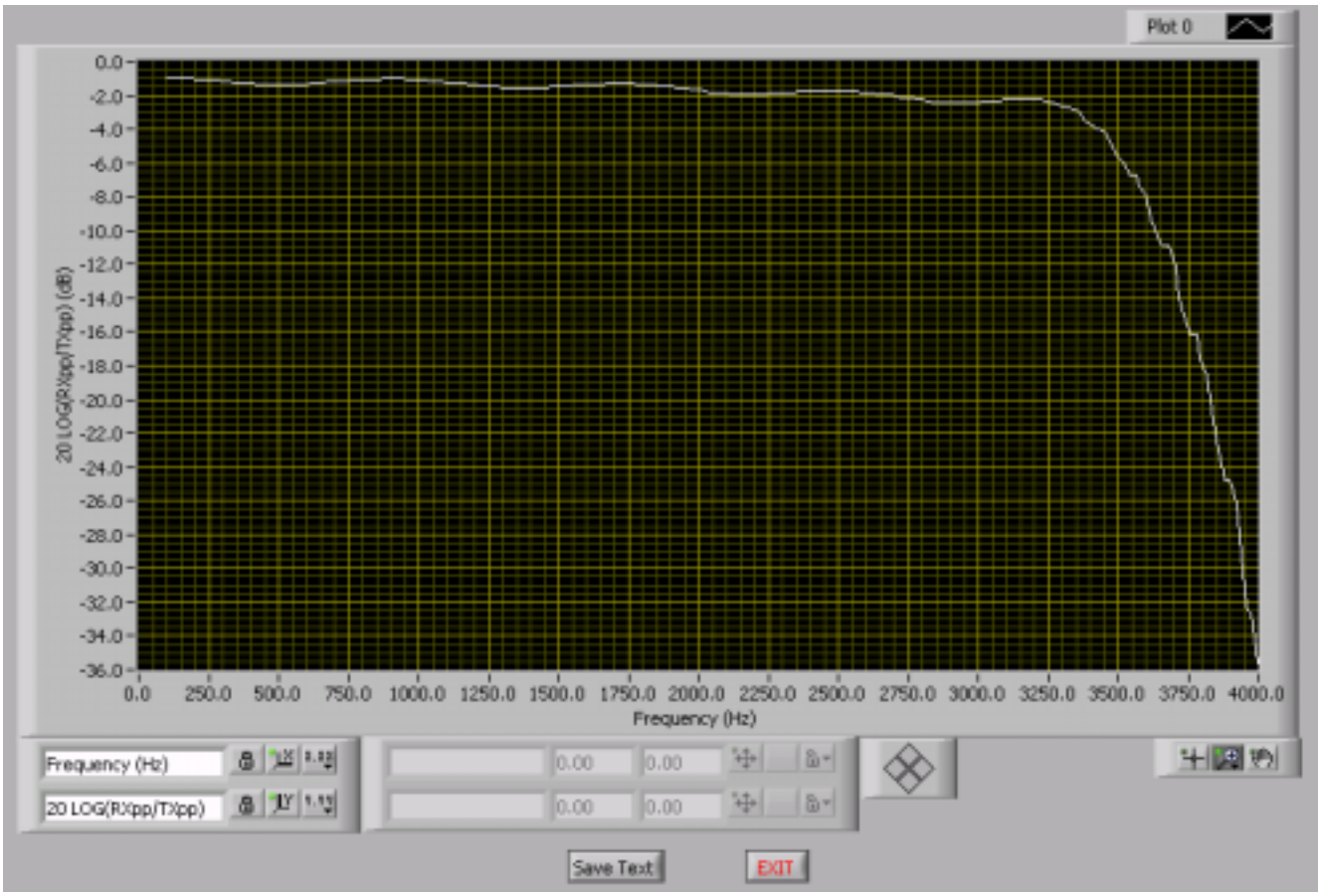



**Figure 9. Transhybrid Loss**

## Transhybrid Loss Calculation

When “Transhybrid Loss Calculation” is selected, the Si3050PPT-EVB software will drive a signal with different frequencies and measure the transhybrid loss based on the following equation: TL = 20Log(TXpk-pk/RXpk-pk). Frequencies used to measure this start from100 Hz to 4000 Hz in 20 Hz steps.

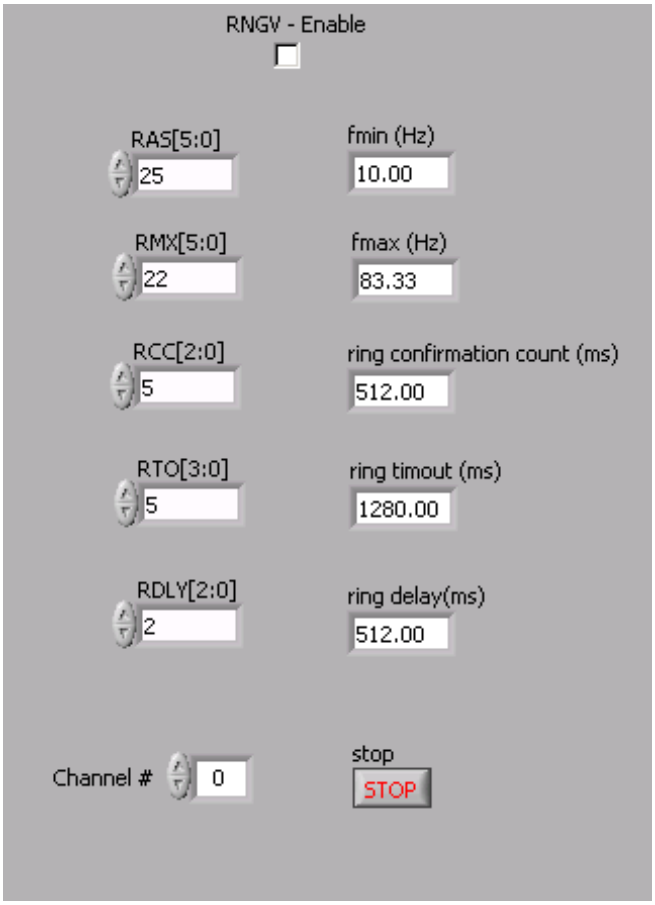



**Figure 10. Ringing**

## Ringing

- RNGV-Enable: Turns on/off RNGV bit on Register 24, bit7
- RAS[5:0]: Update RAS bits on Register 24
- RMX[5:0]: Update RMX bits on Register 22
- RCC[2:0]: Update RCC bits on Register 23
- RTO[3:0]: Update RTO bits on Register 23
- RDLY[2:0]: Update RDLY bits on Register 22 & 23
- Fmin(Hz): Calculate fmin based on RAS bits
- Fmin(Hz): Calculate fmax based on RAS bits and RMX bits
- Ring confirmation count (ms): Shows ring confirmation count based on RCC bits
- Ring timeout(ms): Displays ring timeout based on RTO bits
- Ring delay(ms): displays ring delay based on RDLY bits

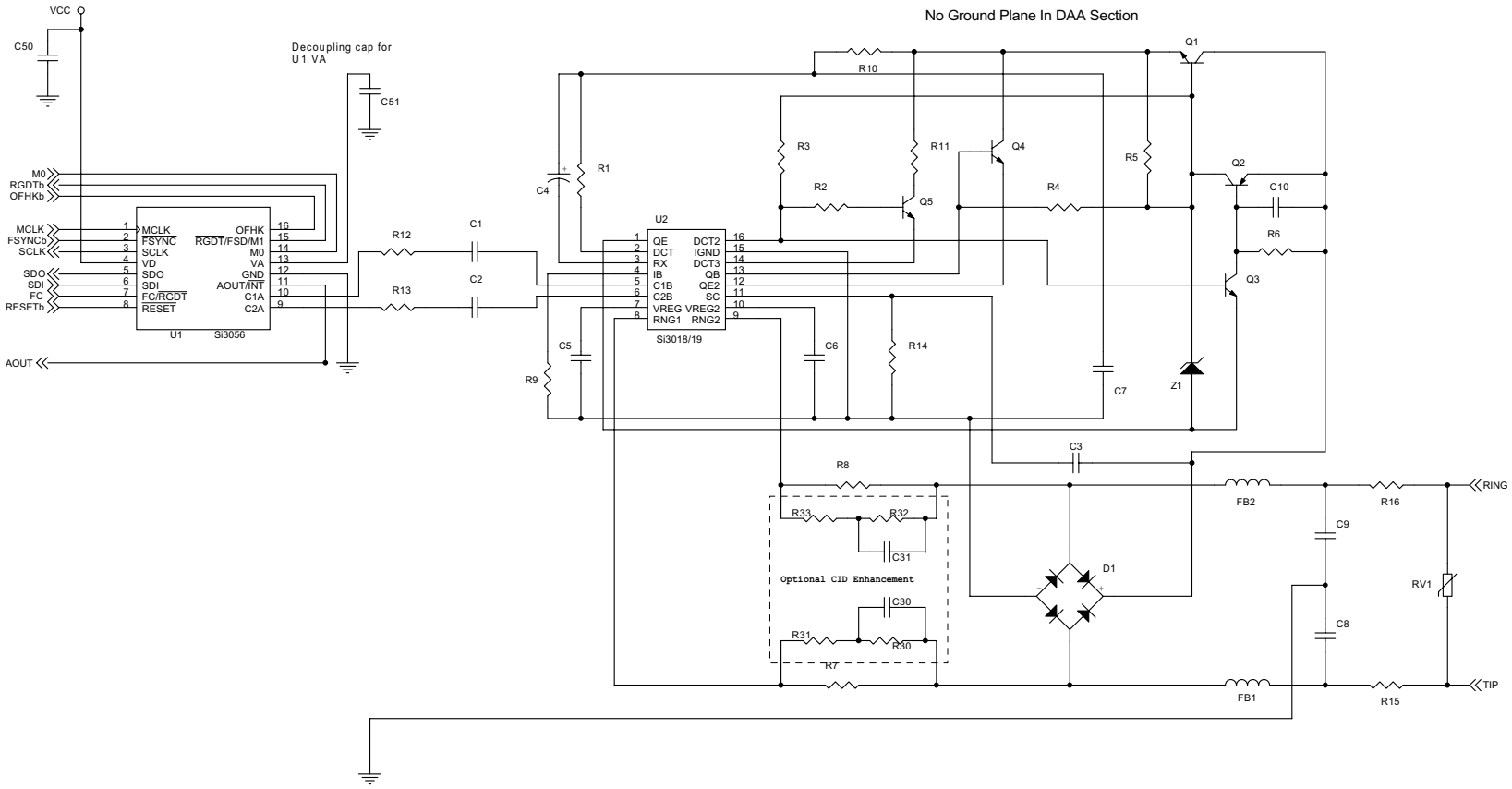



**Figure 11. Si3034/35/44 Daughter Card Schematic (1 of 2)**

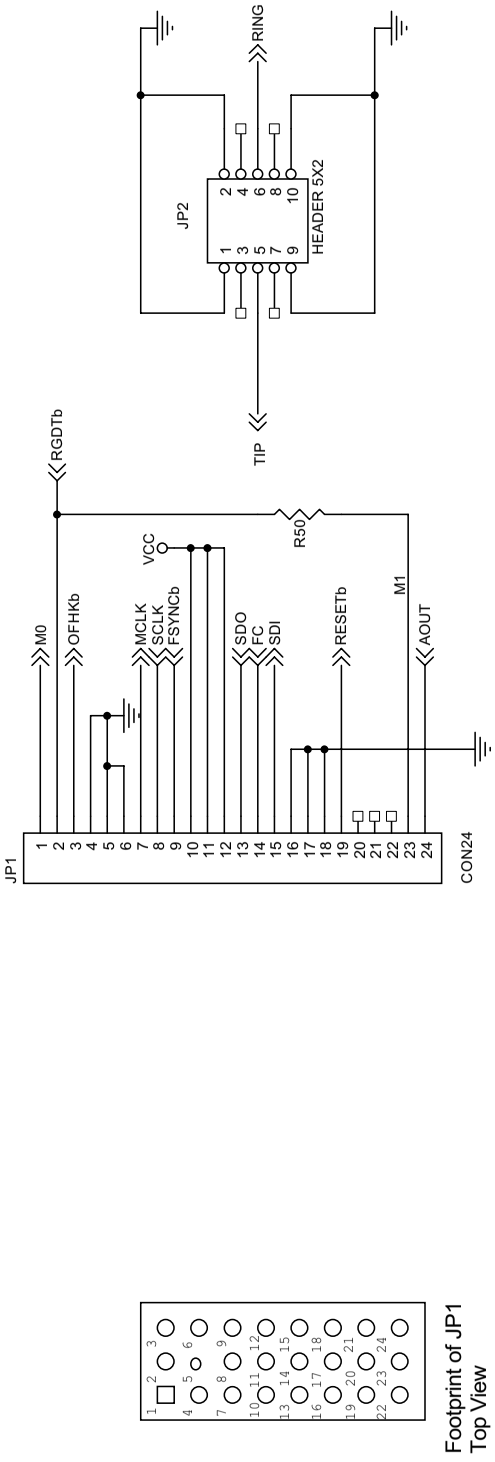



**Figure 12. Si3034/35/44 Daughter Card Schematic (2 of 2)**

## Bill of Materials: Si3034-EVB Daughter Card

| Quantity | Reference | Part |
|---|---|---|
| 2 | C4,C1 | 150 pF, 3 kV, ±20%, 1812, , C1808X7R302-151MNE, Venkel |
| 1 | C3 | 0.22 uF, 25 V, ±20%, 0805, , C0805X7R250-224MNE, Venkel |
| 1 | C5 | 0.1 uF, 50 V, ±20%, Case A, , TA050TCM104-MAL, Venkel |
| 3 | C6,C10,C16 | 0.1 uF, 16 V, ±10%, 0603, , C0603X7R160-104KNE, Venkel |
| 2 | C7,C8 | 560 pF, 250 V, ±10%, 0805, , C0805X7R251-561KNE, Venkel |
| 1 | C9 | 10 nF, 250 V, ±20%, 0805, , C0805X7R251-103KNE, Venkel |
| 4 | R4,C11,R21,C30 | NI, , , 0603, , , |
| 1 | C12 | 0.22 uF, 35 V, ±10%, Case A, , TA035TCM224-KAL, Venkel |
| 1 | C13 | 0.47 uF, 25 V, ±10%, 0805, , C0805X7R250-474KNE, Venkel |
| 1 | C14 | 0.68 uF, 16 V, ±10%, 1206, , 1206YC684KATMA, AVX |
| 2 | C18,C19 | 3.9 nF, 16 V, ±10%, 0603, , C0603X7R160-392KNE, Venkel |
| 1 | C20 | 0.01 uF, 16 V, ±20%, 0603, , C0603X7R160-103KNE, Venkel |
| 1 | C22 | 1800 pF, 50 V, ±10%, 0603, , C0603X7R500-182KNE, Venkel |
| 1 | C23 | NI, , , Case A, , , |
| 2 | C24,C25 | 1000 pF, 3 kV, ±10%, 1812, , C1808X7R302-102KNE, Venkel |
| 4 | R22,R23,C28,C29 | NI, , , 0805, , , |
| 2 | D1,D2 | Dual Diode, 225 mA, 300 V, SOT-23, , CMPD2004S, Central Semiconductor |
| 2 | D3,D4 | BAV99, 300 mA, 100 V, SOT-23, , BAV99, Diodes Inc. |
| 2 | FB1,FB2 | Ferrite Bead, , , 1206, , BLM31A601S, Murata |
| 1 | JP1 | CON24, , , 8x3 100 mil, , SSW-108-01-T-T, |
| 1 | JP2 | HEADER 5X2, , , 5x2 100 mil, , SSW-105-01-T-D, |
| 2 | L2,L1 | 330 uH, 150 mA, , Thru Hole, , EL0607-331J, TDK |
| 2 | Q3,Q1 | NPN, 300 V, , SOT-23, , MMBTA42LT1, Motorola |
| 1 | Q2 | PNP, 300 V, , SOT-23, , MMBTA92LT1, Motorola |
| 1 | Q4 | NPN, 80 V, , SOT-223, , BCP56T1, Motorola |
| 1 | RV1 | SiDactor, 275 V, 100 A, SOD 6, , P3100SB, Teccor |
| 1 | RV2 | NI, , , Thru-Hole, , , |
| 1 | R1 | NI, , , 2010, , , |
| 1 | R2 | 402, 1/8 W, ±1%, 1206, , CR1206-8W-4020FT, Venkel |
| 1 | R3 | NI, , , 0805, , , Venkel |
| 1 | R5 | 36 K, 1/16 W, ±5%, 0603, , CR0603-16W-363JT, Venkel |
| 1 | R6 | 120 K, 1/16 W, ±5%, 0603, , CR0603-16W-124JT, Venkel |
| 6 | R7,R8,R15,R16,R17,R19 | 4.87 K, 1/4 W, ±1%, 1206, , CR1206-4W-4871FT, Venkel |
| 2 | R10,R9 | 56 K, 1/10 W, ±5%, 0805, , CR0805-10W-563JT, Venkel |
| 1 | R11 | 10 K, 1/10 W, ±1%, 0603, , CR0603-16W-1002FT, Venkel |
| 1 | R12 | 78.7, 1/16 W, ±1%, 0603, , CR0603-16W-78R7FT, Venkel |
| 1 | R13 | 215, 1/16 W, ±1%, 0603, , CR0603-16W-2150FT, Venkel |
| 1 | R18 | 2.2 K, 1/10 W, ±5%, 0805, , CR0805-10W-222JT, Venkel |
| 1 | R24 | 150, 1/10 W, ±5%, 0603, , CR0603-10W-150JT, Venkel |
| 2 | R25,R26 | NI, , , 0805, , , |
| 2 | R28,R27 | 10, 1/10 W, ±5%, RC05, , CR0805-10W-100JT, Venkel |
| 1 | R29 | NI, , , 0603, , , |
| 1 | R30 | 0, 1/10 W, ±5%, 0603, , CR0603-10W-000JT, Venkel |
| 1 | U1 | Si3021, , , 16SOIC, , Si3021-KS Rev. C, Silicon Labs |
| 1 | U2 | Si301x, , , 16SOIC, , Si3014-KS Rev. C, Silicon Labs |
| 1 | Z1 | Zener Diode, 43 V, , SOD-80, , ZMM43, General Semi |
| 2 | Z4,Z5 | Zener Diode, 5.6 V, 500 mW, SOD123, , MMSZ5232B, Diodes Inc. |

## Bill of Materials: Si3035-EVB Daughter Card

| Quantity | Reference | Part |
|---|---|---|
| 2 | C4,C1 | 150 pF, 3 kV, ±20%, 1812, , C1808X7R302-151MNE, Venkel |
| 1 | C3 | 0.22 uF, 25 V, ±20%, 0805, , C0805X7R250-224MNE, Venkel |
| 1 | C5 | 1.0 uF, 16 V, ±20%, Case A, , TA016TCM105-MAL, Venkel |
| 3 | C6,C10,C16 | 0.1 uF, 16 V, ±10%, 0603, , C0603X7R160-104KNE, Venkel |
| 6 | R3,C7,C8,C13,R25,R26 | NI, , , 0805, , , |
| 3 | C9,C28,C29 | 15 nF, 250 V, ±20%, 0805, , C0805X7R251-153KNE, Venkel |
| 1 | C11 | 39 nF, 16 V, ±10%, 0603, , C0603X7R160-393KNE, Venkel |
| 1 | C12 | NI, , , Case A, , , |
| 7 | R7,R8,C14,R15,R16,R17, | NI, , , 1206, , , |
| | R19 | |
| 9 | R12,R13,C18,C19,C20,C22, | NI, , , 0603, , , |
| | R24,R30,C30 | |
| 1 | C23 | NI, 35V, ±10%, Case A, , TA035TCM105-KAL, Venkel |
| 2 | C24,C25 | 1000 pF, 3 kV, ±10%, 1812, , C1808X7R302-102KNE, Venkel |
| 2 | D1,D2 | Dual Diode, 225 mA, 300 V, SOT-23, , CMPD2004S, Central Semiconductor |
| 2 | D3,D4 | BAV99, 300 mA, 100 V, SOT-23, , BAV99, Diodes Inc. |
| 2 | FB1,FB2 | Ferrite Bead, , , 1206, , BLM31A601S, MuRata |
| 1 | JP1 | CON24, , , 8x3 100 mil, , SSW-108-01-T-T, |
| 1 | JP2 | HEADER 5X2, , , 5x2 100 mil, , SSW-105-01-T-D, |
| 2 | L2,L1 | 0 ohm,, , Thru Hole, , Wire Jumper |
| 2 | Q3,Q1 | NPN, 300 V, , SOT-23, , MMBTA42LT1, Motorola |
| 1 | Q2 | PNP, 300 V, , SOT-23, , MMBTA92LT1, Motorola |
| 1 | Q4 | NI, , , SOT-223, , , |
| 1 | RV1 | SiDactor, 275 V, 100 A, SOD 6, , P3100SB, Teccor |
| 1 | RV2 | MOV, 240 V, 1250 A, Thru-Hole, , ERZ-V07D241, Panasonic |
| 1 | R1 | 51, 1/2 W, ±5%, 2010, , C2010-2W-510JT, Venkel |
| 1 | R2 | 15, 1/4 W, ±5%, 1206, , CR1206-4W-150JT, Venkel |
| 2 | R4,R21 | 301, 1/16 W, ±1%, 0603, , CR0603-16W-3010FT, Venkel |
| 2 | R6,R5 | 36 K, 1/16 W, ±5%, 0603, , CR0603-16W-363JT, Venkel |
| 2 | R10,R9 | 2 K, 1/10 W, ±5%, 0805, , CR0805-10W-202JT, Venkel |
| 1 | R11 | NI, 16 V, ±10%, 0603, , C0603X7R160-272KNE, Venkel |
| 1 | R18 | 300, 1/10 W, ±5%, 0805, , CR0805-10W-301JT, Venkel |
| 2 | R23,R22 | 20 K, 1/10 W, ±5%, 0805, , CR0805-10W-203JT, Venkel |
| 2 | R28,R27 | 10, 1/10 W, ±5%, RC05, , CR0805-10W-100JT, Venkel |
| 1 | R29 | 0, 1/10 W, ±5%, 0603, , CR0603-10W-000JT, Venkel |
| 1 | U1 | Si3021, , , 16SOIC, , Si3021-KS Rev. C, Silicon Labs |
| 1 | U2 | Si3012/5, , , 16SOIC, , Si3012-KS Rev. G, Silicon Labs |
| 1 | Z1 | Zener Diode, 18 V, , SOD-80, , ZMM18, General Semi |
| 2 | Z4,Z5 | Zener Diode, 5.6 V, 500 mW, SOD123, , MMSZ5232B, General Semi |

## Bill of Materials: Si3044-EVB Daughter Card

| Quantity | Reference | Part |
|---|---|---|
| 2 | C4,C1 | 150 pF, 3 kV, ±20%, 1812, , C1808X7R302-151MNE, Venkel |
| 1 | C3 | 0.22 uF, 25 V, ±20%, 0805, , C0805X7R250-224MNE, Venkel |
| 1 | C5 | 0.1 uF, 50 V, ±20%, Case A, , TA050TCM104-MAL, Venkel |
| 3 | C6,C10,C16 | 0.1 uF, 16 V, ±10%, 0603, , C0603X7R160-104KNE, Venkel |
| 2 | C7,C8 | 560 pF, 250 V, ±10%, 0805, , C0805X7R251-561KNE, Venkel |
| 1 | C9 | 10 nF, 250 V, ±20%, 0805, , C0805X7R251-103KNE, Venkel |
| 4 | R4,C11,R21,C30 | NI, , , 0603, , , |
| 1 | C12 | 1.0 uF, 35 V, ±10%, Case A, , TA035TCM105-KAL, Venkel |
| 1 | C13 | 0.22 uF, 25 V, ±10%, 0805, , C0805X7R250-224KNE, Venkel |
| 1 | C14 | 0.68 uF, 16 V, ±10%, 1206, , 1206YC684KATMA, AVX |
| 2 | C18,C19 | 3.9 nF, 16 V, ±10%, 0603, , C0603X7R160-392KNE, Venkel |
| 1 | C20 | 0.01 uF, 16 V, ±20%, 0603, , C0603X7R160-103KNE, Venkel |
| 1 | C22 | 1800 pF, 50 V, ±10%, 0603, , C0603X7R500-182KNE, Venkel |
| 1 | C23 | NI, , , Case A, , , |
| 2 | C24,C25 | 1000 pF, 3 kV, ±10%, 1812, , C1808X7R302-102KNE, Venkel |
| 4 | R22,R23,C28,C29 | NI, , , 0805, , , |
| 2 | D1,D2 | Dual Diode, 225 mA, 300 V, SOT-23, , CMPD2004S, Central Semiconductor |
| 2 | D3,D4 | BAV99, 300 mA, 100 V, SOT-23, , BAV99, Diodes Inc. |
| 2 | FB1,FB2 | Ferrite Bead, , , 1206, , BLM31A601S, Murata |
| 1 | JP1 | CON24, , , 8x3 100 mil, , SSW-108-01-T-T, |
| 1 | JP2 | HEADER 5X2, , , 5x2 100 mil, , SSW-105-01-T-D, |
| 2 | L2,L1 | 330 uH, 150 mA, , Thru Hole, , EL0607-331J, TDK |
| 2 | Q3,Q1 | NPN, 300 V, , SOT-23, , MMBTA42LT1, Motorola |
| 1 | Q2 | PNP, 300 V, , SOT-23, , MMBTA92LT1, Motorola |
| 1 | Q4 | NPN, 80 V, , SOT-223, , BCP56T1, Motorola |
| 1 | RV1 | SiDactor, 275 V, 100 A, SOD 6, , P3100SB, Teccor |
| 1 | RV2 | NI, , , Thru-Hole, , , |
| 1 | R1 | NI, , , 2010, , , |
| 1 | R2 | 402, 1/8 W, ±1%, 1206, , CR1206-8W-4020FT, Venkel |
| 1 | R3 | NI, , , 0805, , , Venkel |
| 1 | R5 | 100 K, 1/16 W, ±1%, 0603, , CR0603-16W-104FT, Venkel |
| 1 | R6 | 120 K, 1/16 W, ±5%, 0603, , CR0603-16W-124JT, Venkel |
| 6 | R7,R8,R15,R16,R17,R19 | 5.36 K, 1/4 W, ±1%, 1206, , CR1206-4W-5361FT, Venkel |
| 2 | R10,R9 | 56 K, 1/10 W, ±5%, 0805, , CR0805-10W-563JT, Venkel |
| 1 | R11 | 9.31 K, 1/10 W, ±1%, 0603, , CR0603-16W-9311FT, Venkel |
| 1 | R12 | 78.7, 1/16 W, ±1%, 0603, , CR0603-16W-78R7FT, Venkel |
| 1 | R13 | 215, 1/16 W, ±1%, 0603, , CR0603-16W-2150FT, Venkel |
| 1 | R18 | 2.2 K, 1/10 W, ±5%, 0805, , CR0805-10W-222JT, Venkel |
| 1 | R24 | 150, 1/10 W, ±5%, 0603, , CR0603-10W-150JT, Venkel |
| 2 | R25,R26 | 10 M, 1/10 W, ±5%, 0805, , CR0805-10W-106JT, Venkel |
| 2 | R28,R27 | 10, 1/10 W, ±5%, RC05, , CR0805-10W-100JT, Venkel |
| 1 | R29 | NI, , , 0603, , , |
| 1 | R30 | 0, 1/10 W, ±5%, 0603, , CR0603-10W-000JT, Venkel |
| 1 | U1 | Si3021, , , 16SOIC, , Si3021-KS Rev. C, Silicon Labs |
| 1 | U2 | Si301x, , , 16SOIC, , Si3015-KS Rev. D, Silicon Labs |
| 1 | Z1 | Zener Diode, 43 V, , SOD-80, , ZMM43, General Semi |
| 2 | Z4,Z5 | Zener Diode, 5.6 V, 500 mW, SOD123, , MMSZ5232B, Diodes Inc. |

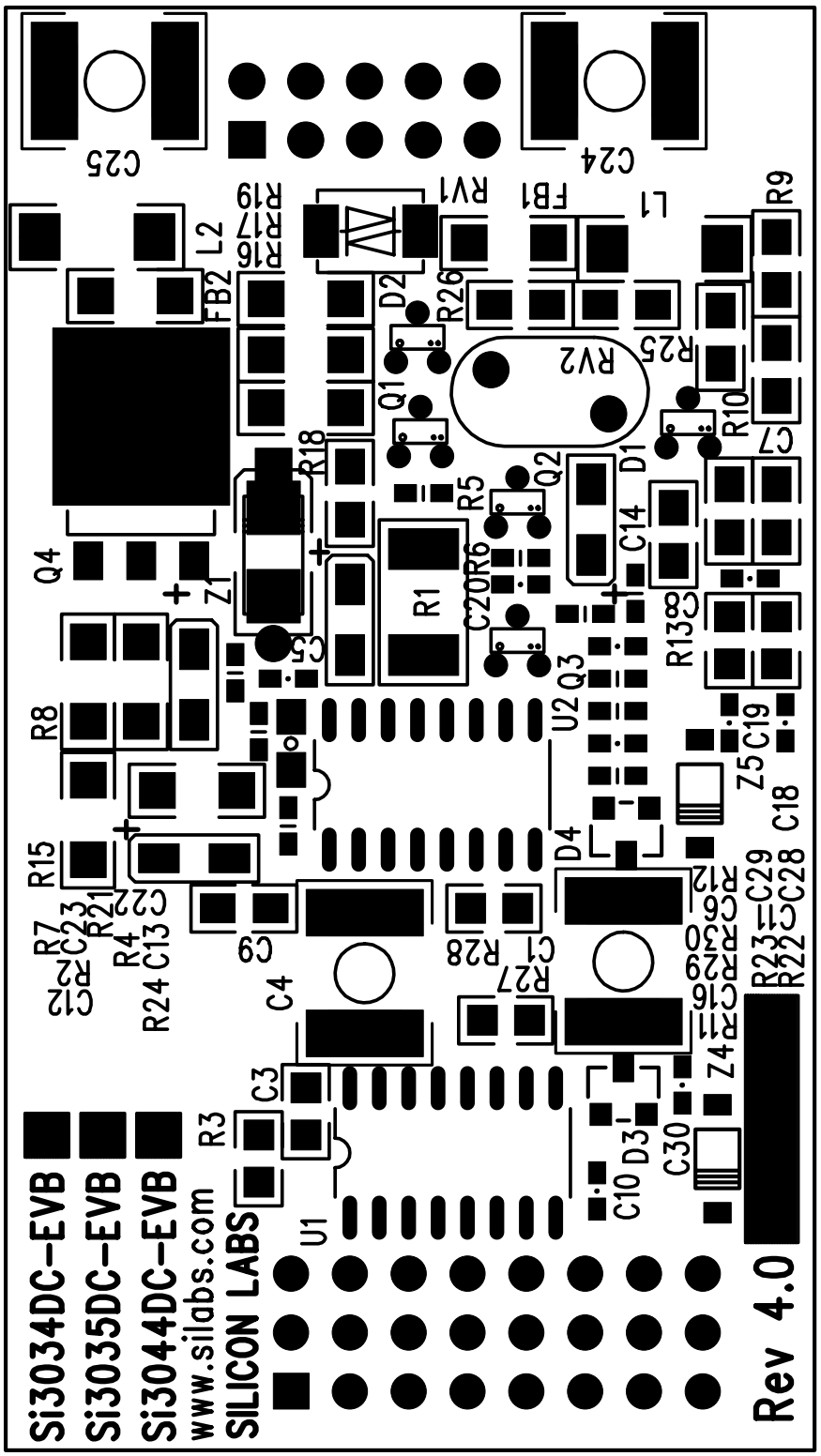



**Figure 1. Si3034/35/44 Daughter Card Silkscreen**

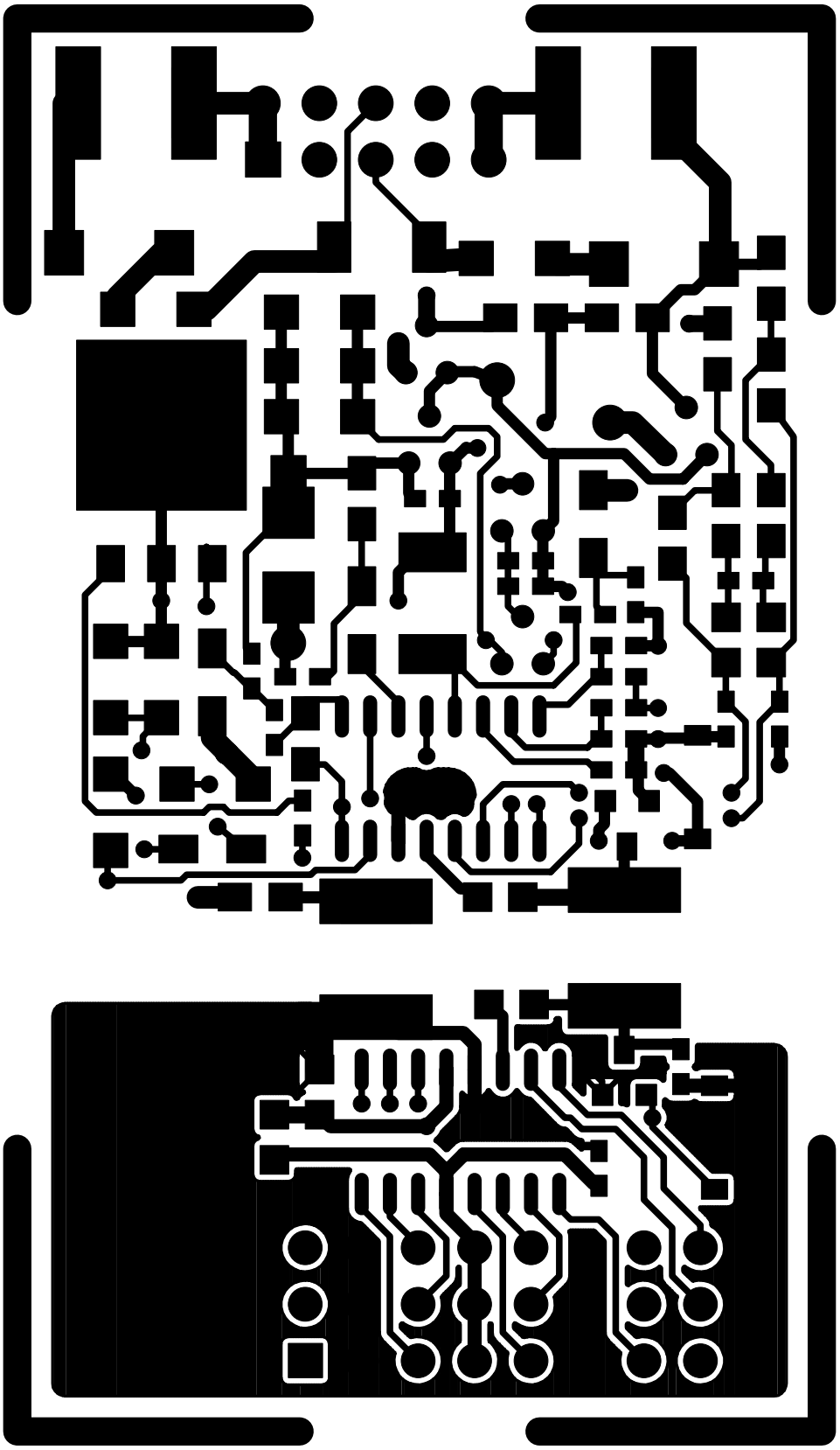


Figure 2. Si3034/35/44 Daughter Card Component Layer

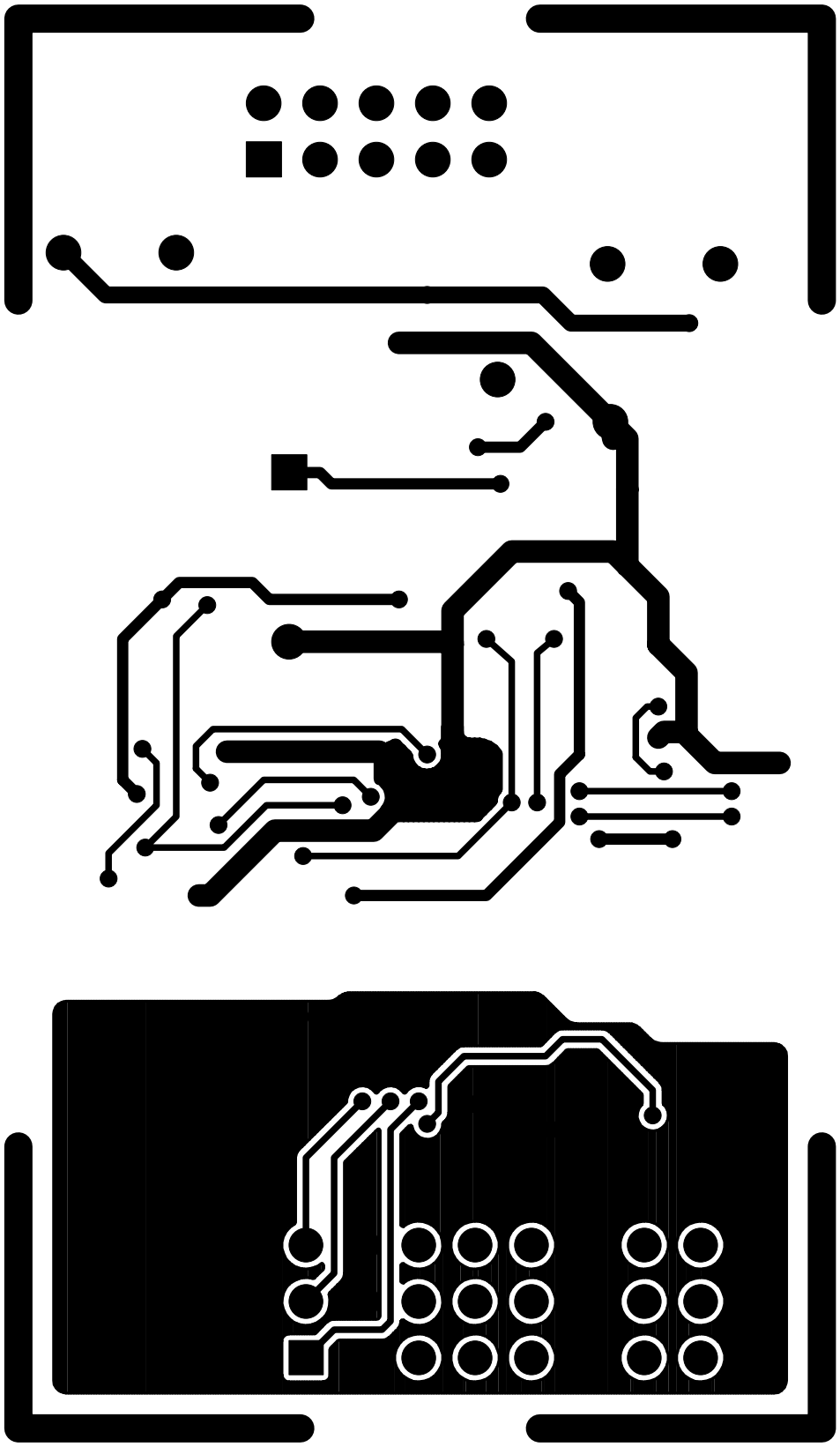


Figure 3. Si3034/35/44 Daughter Card Solder Layer

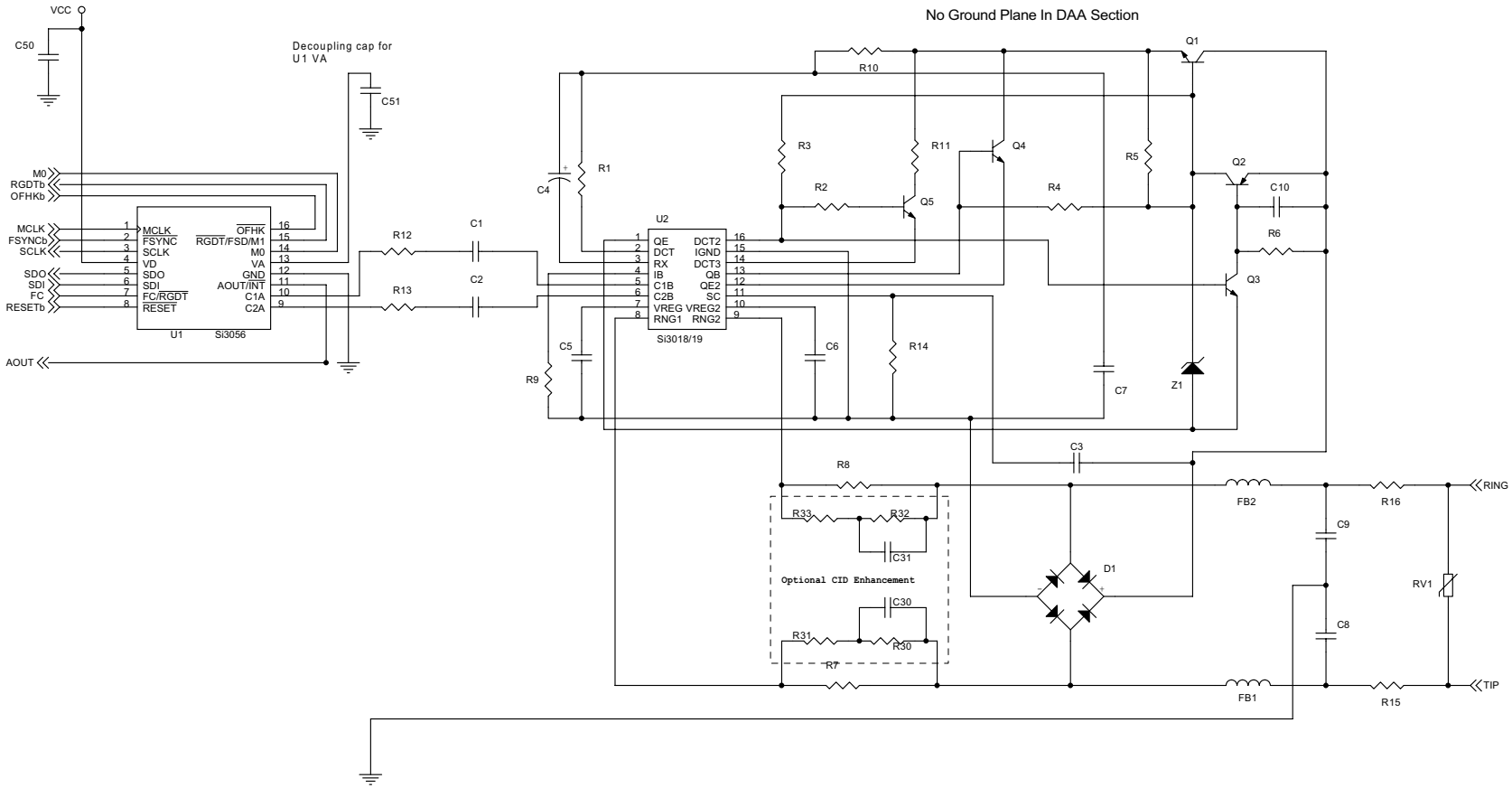



**Figure 13. Si3056 Daughter Card Schematic (1 of 2)**

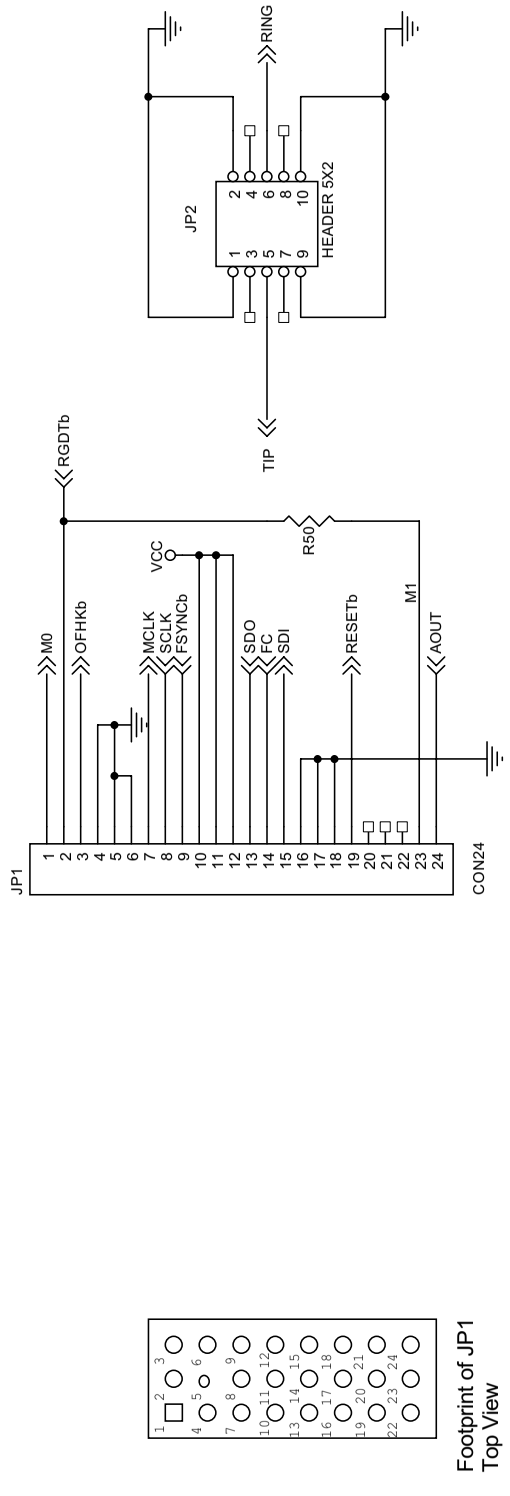



**Figure 14. Si3056 Daughter Card Schematic (2 of 2)**

## Bill of Materials: Si3056-EVB Daughter Card

| Reference | Value | Tolerance | Rating | Part Number | Manufacturer | PCB Footprint |
|---|---|---|---|---|---|---|
| C2,C1 | 33 pF | ±20% | Y2 | ECCAVS330KGS | Panasonic | Thru-hole |
| C3 | 10 nF | ±20% | 250 V | C0805X7R251-103MNE | Venkel | 805 |
| C4 | 1.0 uF | ±20% | 50 V | ECE-V1HS010SR | Panasonic | Size A |
| C6,C5 | 0.1 uF | ±20% | 16 V | C0603X7R160-104MNE | Venkel | 603 |
| C7 | 2.7 nF | ±20% | 50 V | C0603X7R500-272MNE | Venkel | 603 |
| C9,C8 | 680 pF | ±10% | Y2 | ECKATS681KBS | Panasonic | Thru-hole |
| C10 | 0.01 uF | ±20% | 16 V | C0603X7R160-103MNE | Venkel | 603 |
| C30,C31 | DNP 120pF | ±20% | 250 V | C0805X7R251-121MNE | Venkel | 805 |
| C51,C50 | 0.1 uF | ±20% | 16 V | C0805X7R160-104MNE | Venkel | 805 |
| D1 | HD04 | | 400 V | HD04-T | Diodes, Inc. | Mini-DIP |
| FB1,FB2 | Ferrite Bead | | | BLM21A601S | MuRata | 805 |
| JP1 | CON24 | | | SSW-108-02-G-T | Samtec | 3x8 100 mil |
| JP2 | HEADER 5X2 | | | SSW-105-01-T-D | Samtec | 5x2 100 mil |
| Q3,Q1 | NPN | | 300 V | MMBTA42LT1 | Motorola | SOT-23 |
| Q2 | PNP | | 300 V | MMBTA92LT1 | Motorola | SOT-23 |
| Q4,Q5 | NPN | | 80 V | MMBTA06LT1 | Motorola | SOT-23 |
| RV1 | SiDactor | 100 A | 275 V | P3100SB | Teccor | SOD 6 |
| R1 | 1.07 K | ±1% | 1/2 W | CR1210-2W-1071FT | Venkel | 1210 |
| R2 | 150 | ±5% | 1/16 W | CR0402-16W-150JT | Venkel | 402 |
| R3 | 3.65 K | ±1% | 1/2 W | CR1210-2W-3651FT | Venkel | 1210 |
| R4 | 2.49 K | ±1% | 1/2 W | CR1210-2W-2491FT | Venkel | 1210 |
| R6,R5 | 100 K | ±5% | 1/16 W | CR0402-16W-104JT | Venkel | 402 |
| R8,R7 | 20 M | ±1% | 1/8 W | CR0805-8W-2005FT | Venkel | 805 |
| R9 | 1 M | ±1% | 1/16 W | CR0402-16W-1004FT | Venkel | 402 |
| R10 | 536 | ±1% | 1/4 W | CR1206-4W-5360FT | Venkel | 1206 |
| R11 | 73.2 | ±1% | 1/2 W | CR1210-2W-73R2FT | Venkel | 1210 |
| R12,R13,R14 | 0 | ±1% | 1/16 W | CR0603-16W-000F | Venkel | 603 |
| R16,R15 | 0 | ±1% | 1/16 W | CR0805-16W-000F | Venkel | 805 |
| R32,R30 | DNP 15M | ±5% | 1/8 W | CR0805-8W-156JT | Venkel | 805 |
| R31,R33 | DNP 5.1M | ±5% | 1/8 W | CR0805-8W-515JT | Venkel | 805 |
| R50 | 47 K | ±5% | 1/16 W | CR0603-16W-473JT | Venkel | 603 |
| U1 | Si3056 | | | Si3056-KS Rev C | Silicon Labs | 16SOIC |
| U2 | Si3018/19 | | | Si3018-KS Rev C | Silicon Labs | 16SOIC |
| Z1 | 43 V | | 1/2 W | ZMM43 | General Semi | SOD-80 |

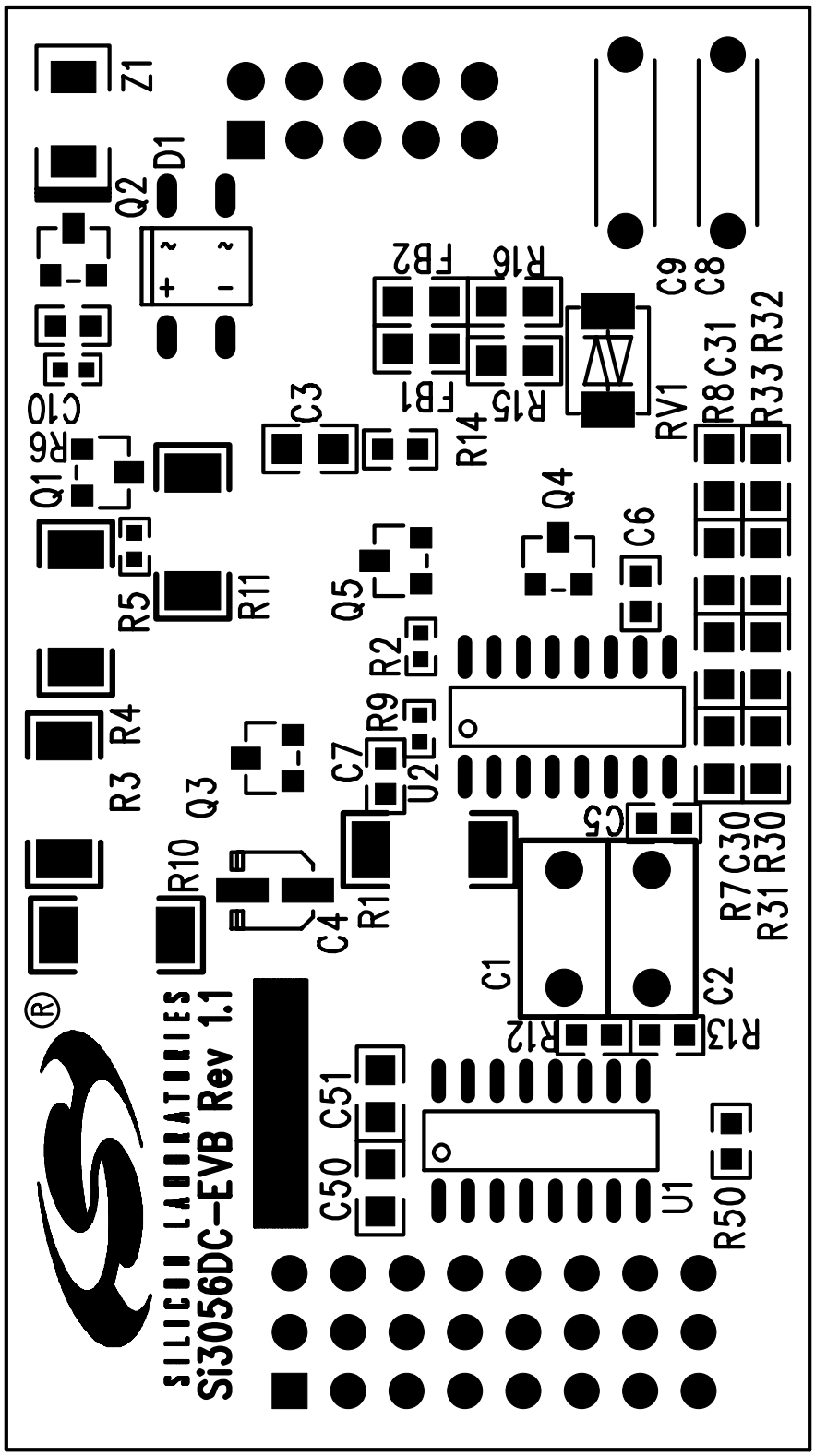



**Figure 15. Si3056 Daughter Card Silkscreen**

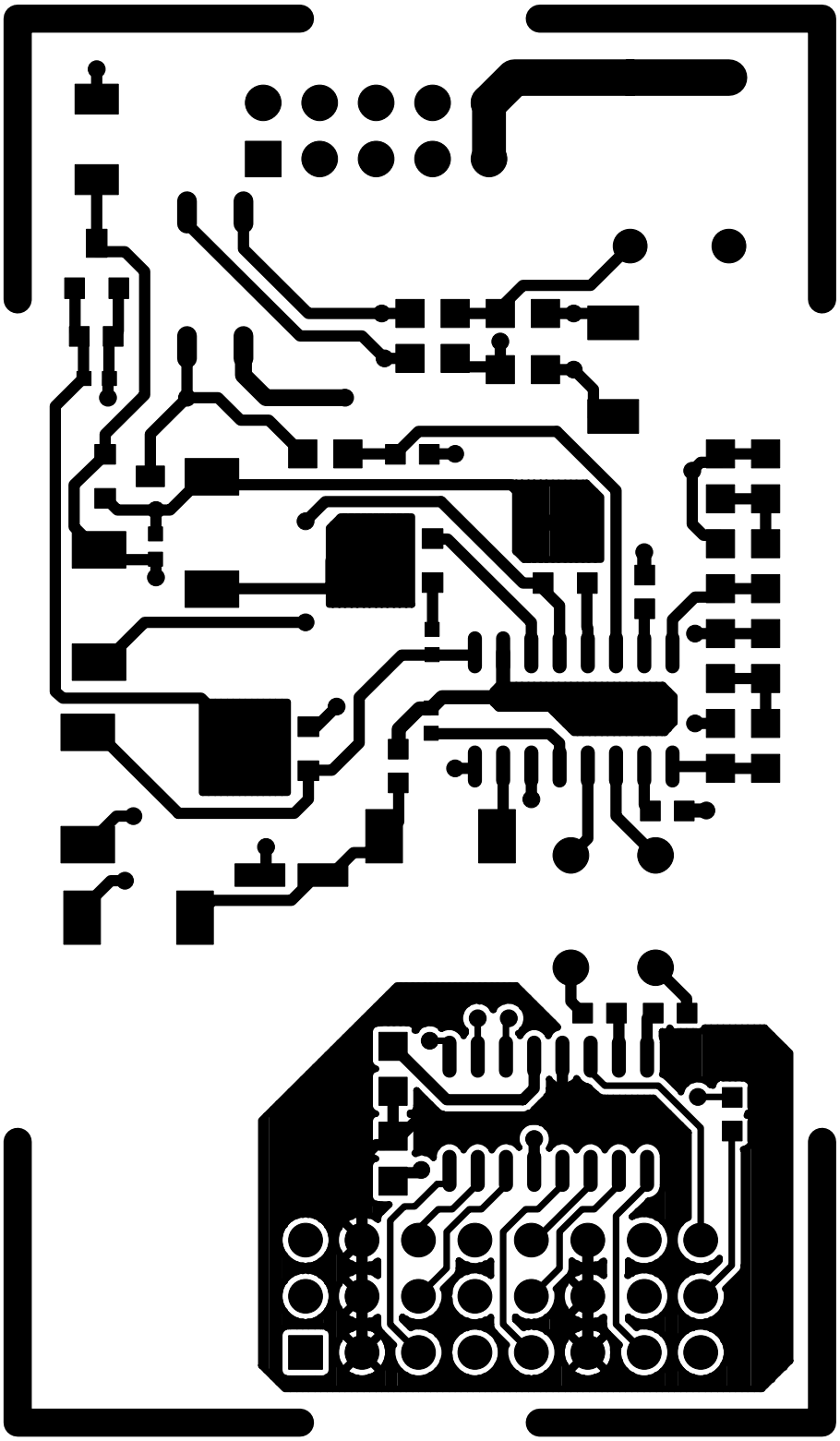


Figure 16. Si3056 Daughter Card Component Layer

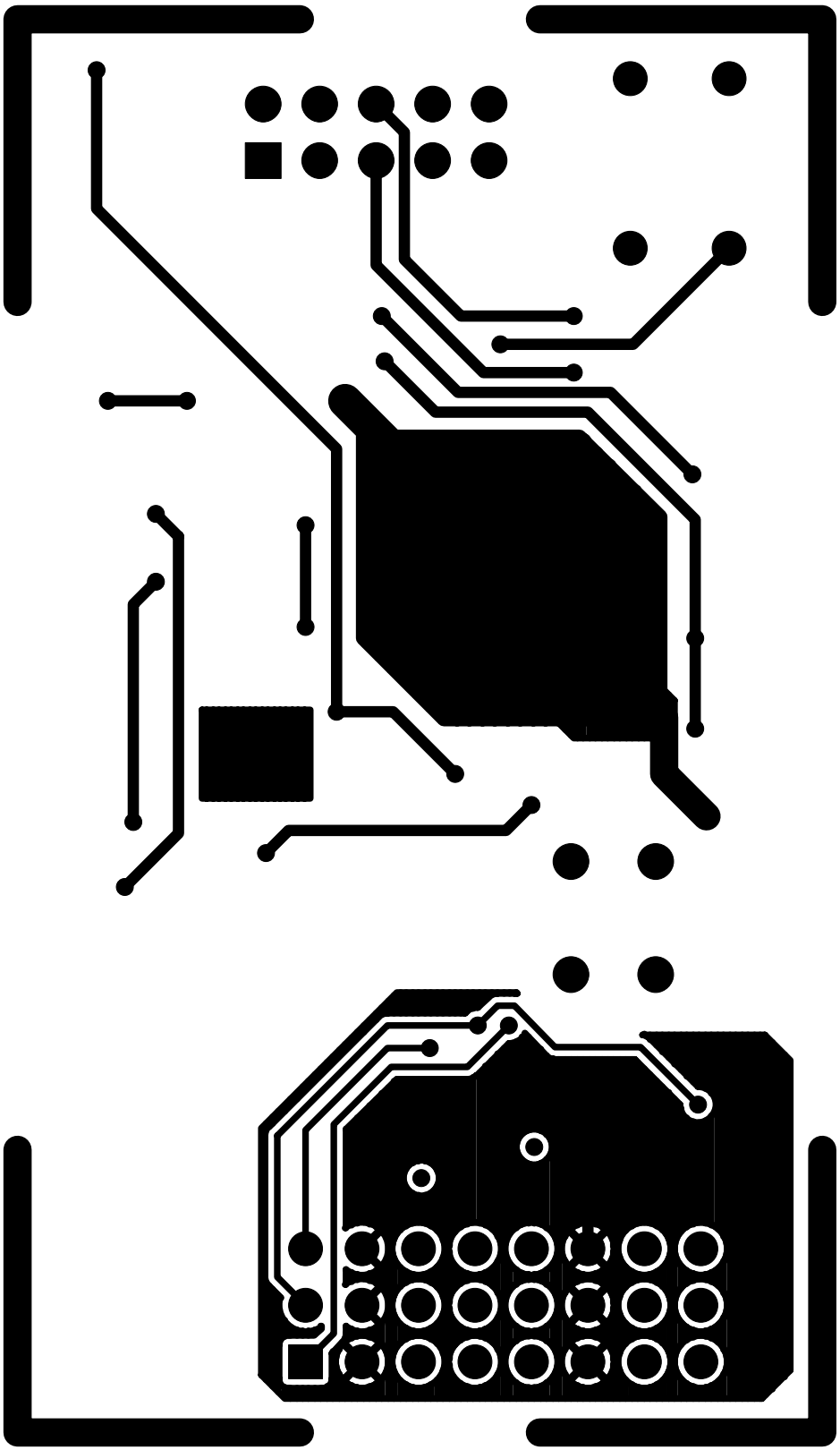


Figure 17. Si3056 Daughter Card Solder Layer

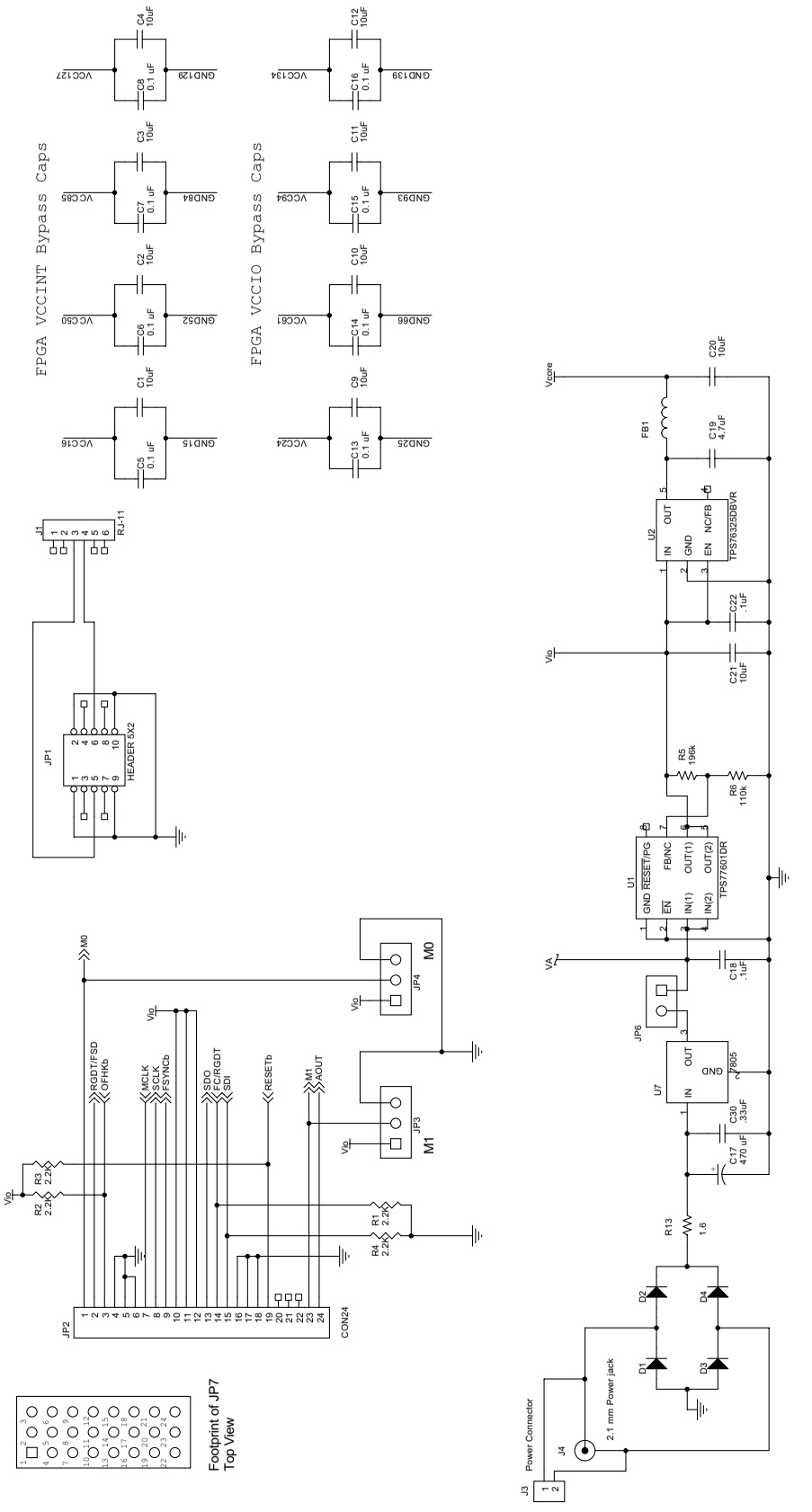



**Figure 18. Si30xx Motherboard Schematic (1 of 3)**

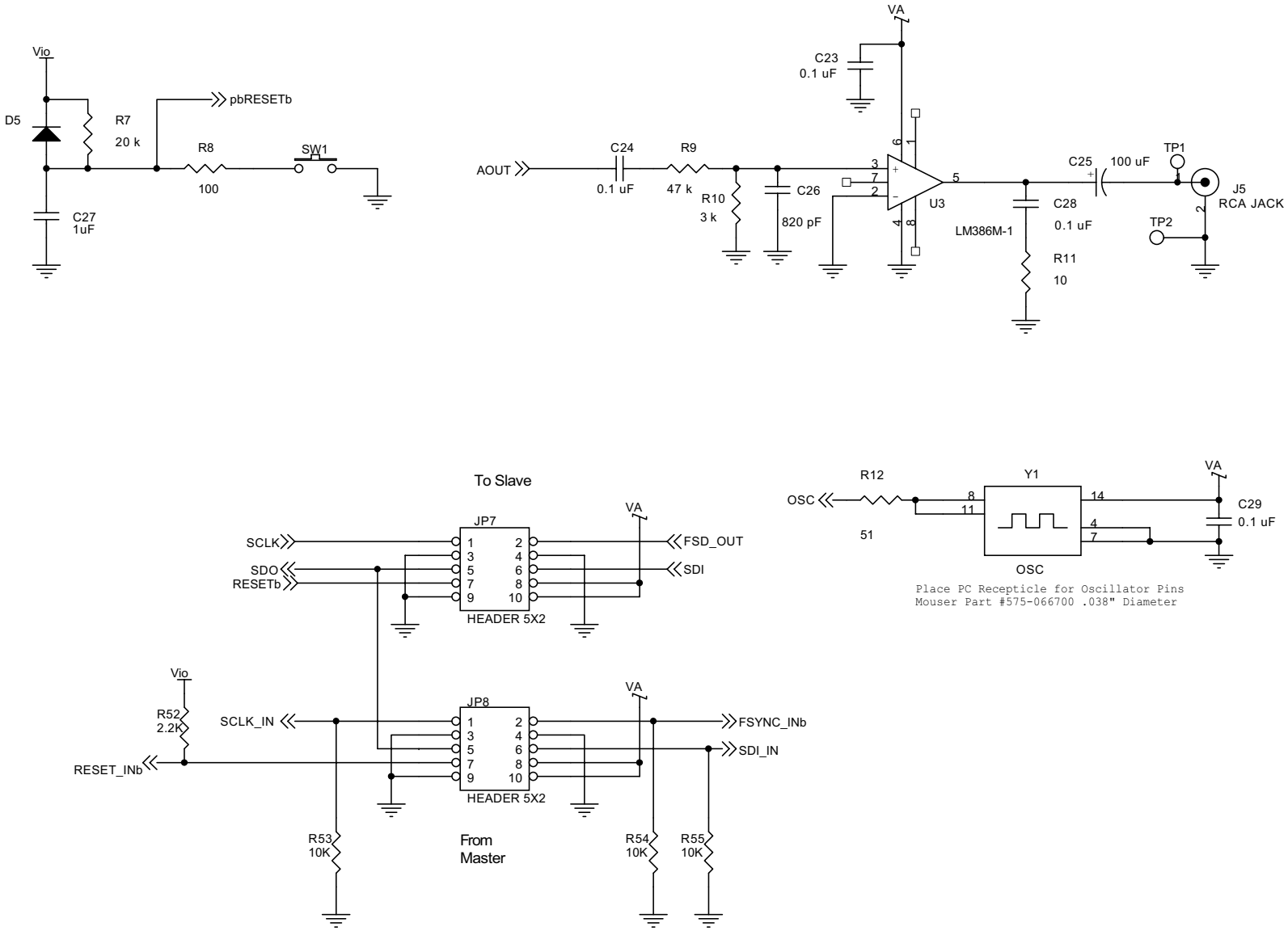



**Figure 19. Si30xx Motherboard Schematic (2 of 3)**

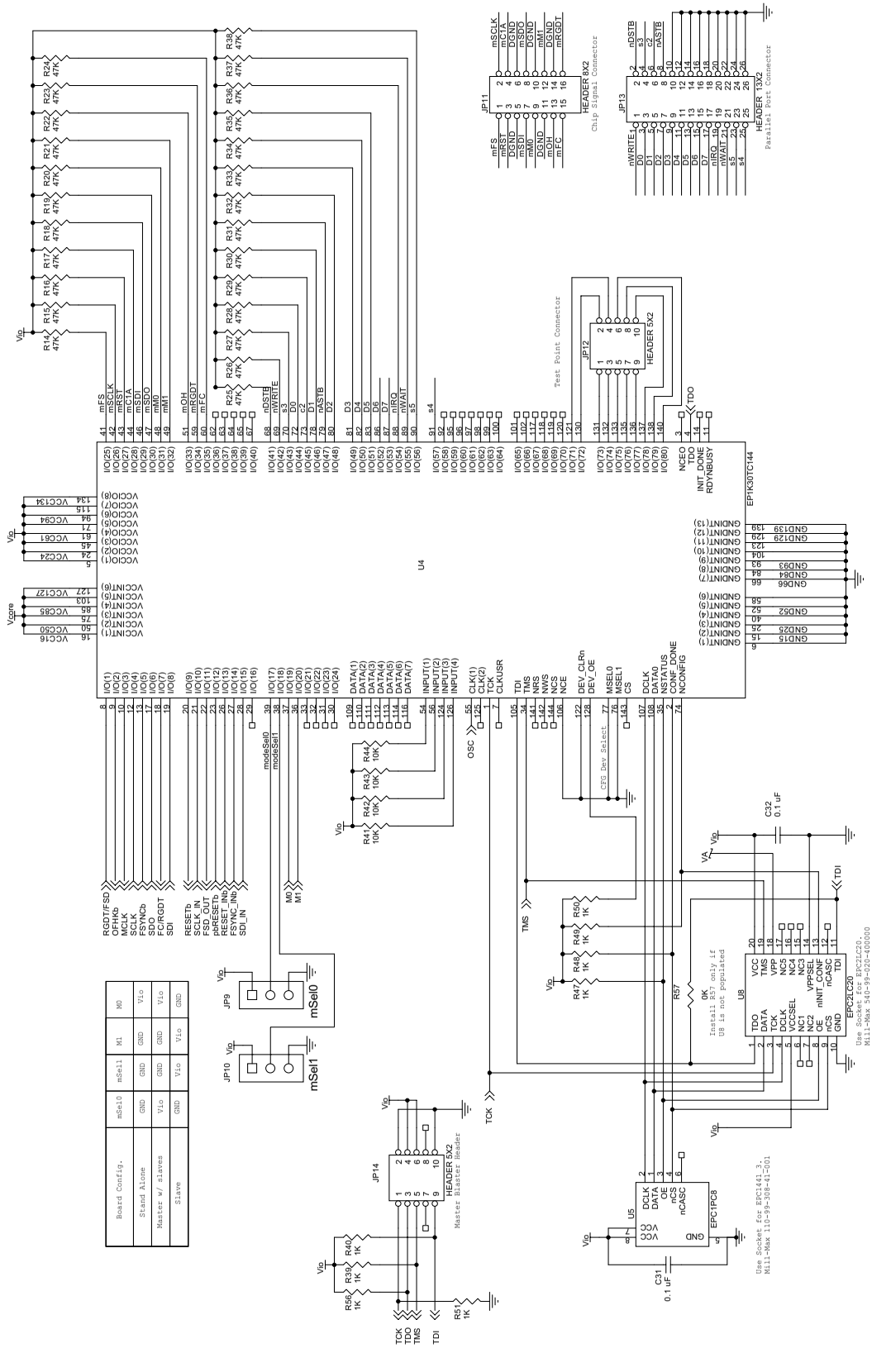


Figure 20. Si30xx Motherboard Schematic (3 of 3)

## Bill of Materials: Si30XX Motherboard

| Item | Qty | Reference | Part |
|---|---|---|---|
| 1 | 10 | C1,C2,C3,C4,C9,C10,C11, | 10uF, 10 V, ±10%, 1206, , C1206X7R100-106KNE, Venkel |
| | | C12,C20,C21 | |
| 2 | 14 | C5,C6,C7,C8,C13,C14,C15, C16,C23,C24,C28,C29,C31, C32 | 0.1 uF, 16 V, ±10%, 0603, , C0603X7R160-104KNE, Venkel |
| 3 | 1 | C17 | 470 uF, 25 V, ±20%, radial 10x16, , UVX1E471MPA, NIC Components |
| 4 | 2 | C18,C22 | .1uF, 25V, , 0805, , C0805X7R250-104KNE, Venkel |
| 5 | 1 | C19 | 4.7uF, 10V, +/-10%, 1206, , TDKC3216X5RA475KT, CLASSIC COMP |
| 6 | 1 | C25 | 100 uF, 16 V, ±10%, radial 6.3x11, , , TTI |
| 7 | 1 | C26 | 820 pF, 50 V, ±5%, 0805, , C0805COG500-821JNE, Venkel |
| 8 | 1 | C27 | 1uF, 10 V, ±10%, 1206, , C1206X7R100-105KNE, Venkel |
| 9 | 1 | C30 | .33uF, 25V, , 0805, , C0805G334Z3NT, CLASSIC COMP |
| 10 | 4 | D1,D2,D3,D4 | DIODE, 30 V, 0.5 A, SOD-123, , MBR0530T1, Motorola |
| 11 | 1 | D5 | DIODE, 400 mA, 75 V, DO-35, , 1N4148, Diodes, Inc. |
| 12 | 1 | FB1 | Ferrite Bead on wire, 3x1x4 (mm), , thru-hole 2, , 2743015112, Fair-Rite |
| 13 | 1 | JP1 | HEADER 5X2, , , 5x2 100 mil, , TMM-105-01-G-D, Samtec |
| 14 | 1 | JP2 | CON24, , , 3x8 100 mil, , TSW-108-07-G-T, Samtec |
| 15 | 4 | JP3,JP4,JP9,JP10 | 3X1 Header, , , 3x1 100 mil, , 68000-403, Berg Electronics |
| 16 | 1 | JP6 | 2X1 Header, , , 2x1 100 mil, , 517-6111TN, Mouser |
| 17 | 1 | JP7 | HEADER 5X2, , , 10 pin thru-hole, , TSW-105-08-T-D-RA, Samtec |
| 18 | 1 | JP8 | HEADER 5X2, , , 10 pin thru-hole, , SSW-105-02-T-D-RA, Samtec |
| 19 | 1 | JP11 | HEADER 8X2, , , 8x2 100 mil, , , |
| 20 | 2 | JP14,JP12 | HEADER 5X2, , , 5x2 100 mil, , , |
| 21 | 1 | JP13 | HEADER 13X2, , , 13X2 100 mil, , 13x2 pin Header with Shroud, Mouser |
| 22 | 1 | J1 | RJ-11, , , thru-hole 6, , 154-0L6641, Mouser |
| 23 | 1 | J3 | Power Connector, , , thru-hole 2, , TSA-2, Adam Tech |
| 24 | 1 | J4 | 2.1 mm Power jack, , , thru-hole 3, , ADC-002-1, Adam Tech |
| 25 | 1 | J5 | RCA JACK, , , thru-hole, , 16J097, Mouser |
| 26 | 5 | R1,R2,R3,R4,R52 | 2.2K, , , 0805, , CR0805-10W-222JT, Venkel |
| 27 | 1 | R5 | 196k, , , 0805, , MCHRIDEZHFX1963E, Classic Comp |
| 28 | 1 | R6 | 110k, , , 0805, , CR21-114J-T, Classic Comp |
| 29 | 1 | R7 | 20 k, 1/10 W, ±1%, 0805, , NRC10F2002TR, NIC Components |
| 30 | 1 | R8 | 100, 1/4 W, ±1%, 1206, , MCR18EZHMFX1000, Rohm |
| 31 | 1 | R9 | 47 k, 1/10 W, ±5%, 0805, , NRC10J473TR, NIC Components |
| 32 | 1 | R10 | 3 k, 1/10 W, ±5%, 0805, , NRC10J302TR, NIC Components |
| 33 | 1 | R11 | 10, 1/10 W, ±1%, 0805, , NRC10F10R0TR, NIC Components |
| 34 | 1 | R12 | 51, 1/10 W, ±5%, 0805, , CR21-510J-T, AVX |
| 35 | 1 | R13 | 1.6, , +-5%, 1206, , CR1206-8W-1R6JT, Venkel |
| 36 | 25 | R14,R15,R16,R17,R18,R19, R20,R21,R22,R23,R24,R25, R26,R27,R28,R29,R30,R31, R32,R33,R34,R35,R36,R37, R38 | 47K, , , 0603, , CR0603-16W-473JT, Venkel |
| 37 | 2 | R40,R39 | 1K, , , 0603, , CR0603-16W-1002FT, Venkel |
| 38 | 7 | R41,R42,R43,R44,R53,R54, R55 | 10K, , , 0603, , CR0603-16W-1002FT, Venkel |
| 39 | 6 | R47,R48,R49,R50,R51,R56 | 1K, , , 0603, , MCR03FZHJ102, TTI |
| 40 | 1 | SW1 | SW PUSHBUTTON, , , thru-hole 4, , 101-0161, Mouser |
| 41 | 1 | TP1 | Test Point, , , thru-hole, , 151-207, Mouser |
| 42 | 1 | TP2 | Test Point, , , thru-hole, , 151-203, Mouser |
| 43 | 1 | U1 | TPS77601DR, , , 8-Pin SOIC, , , Texas Instruments |
| 44 | 1 | U2 | TPS76325DBVR, , , 5-Pin SOT-23, , , Texas Instruments |
| 45 | 1 | U3 | OP-AMP, , , M, , LM386M-1, National Semi |
| 46 | 1 | U4 | EP1K30TC144, , , TQFP-144, , EP1K30TC144-3, Altera |
| 47 | 1 | U7 | 7805, , , TO-220AB, , uA7805CKC, Texas Instruments |
| 48 | 1 | U5 | Socket, , , DIP-8, ,110-99-308-41-001, Mill-Max |
| 49 | 6 | Y1 | PC Recepticle, .038" Diameter, 575-06670, Mouser |
| 50 | 1 | R57 | 0K, , , 0603, , CR0603-16W-000T, Venkel |
| 51 | 4 | N/A | 1/2" Plastic Standoff |
| 52 | 4 | N/A | Plastic Screw |

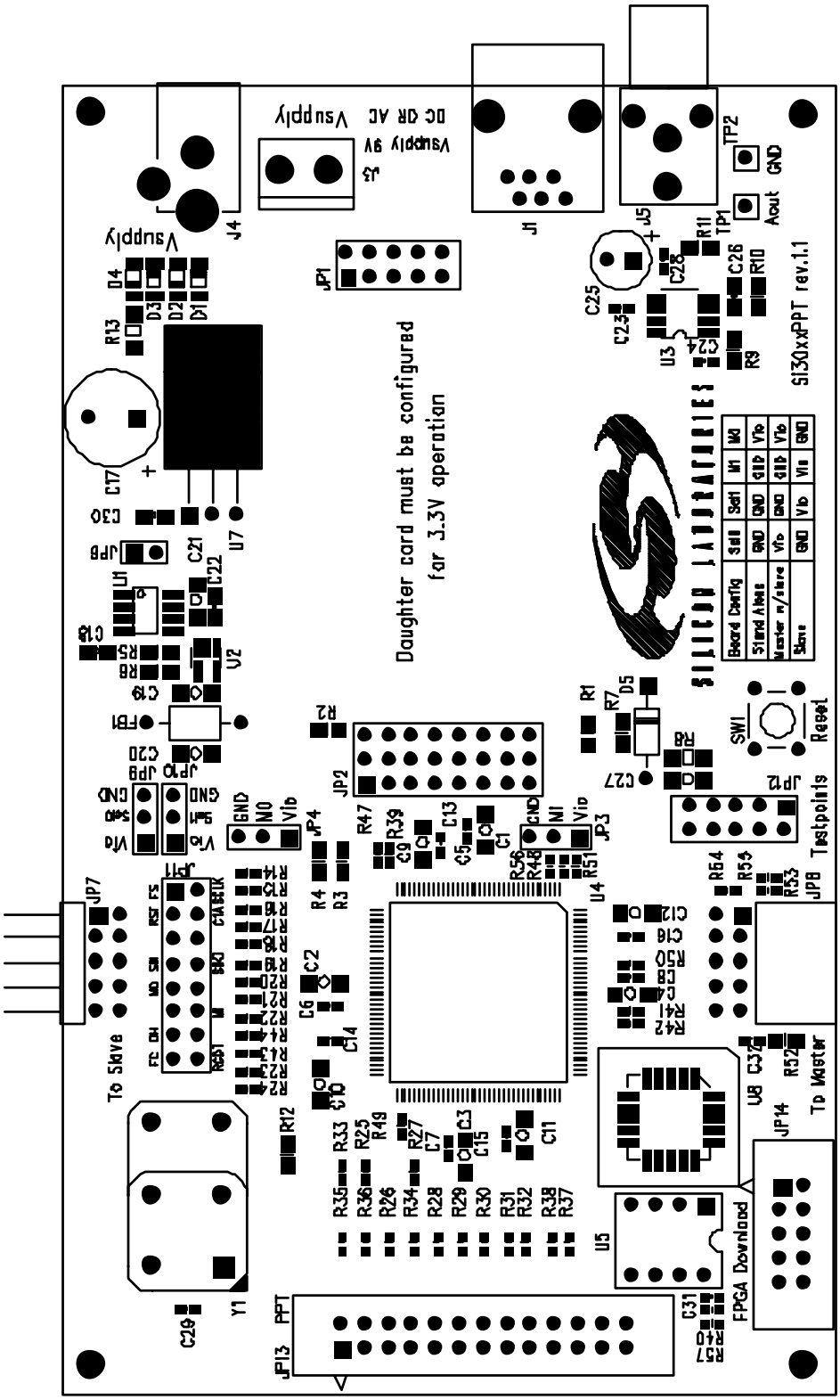



Figure 21. Si30xx Motherboard Silkscreen

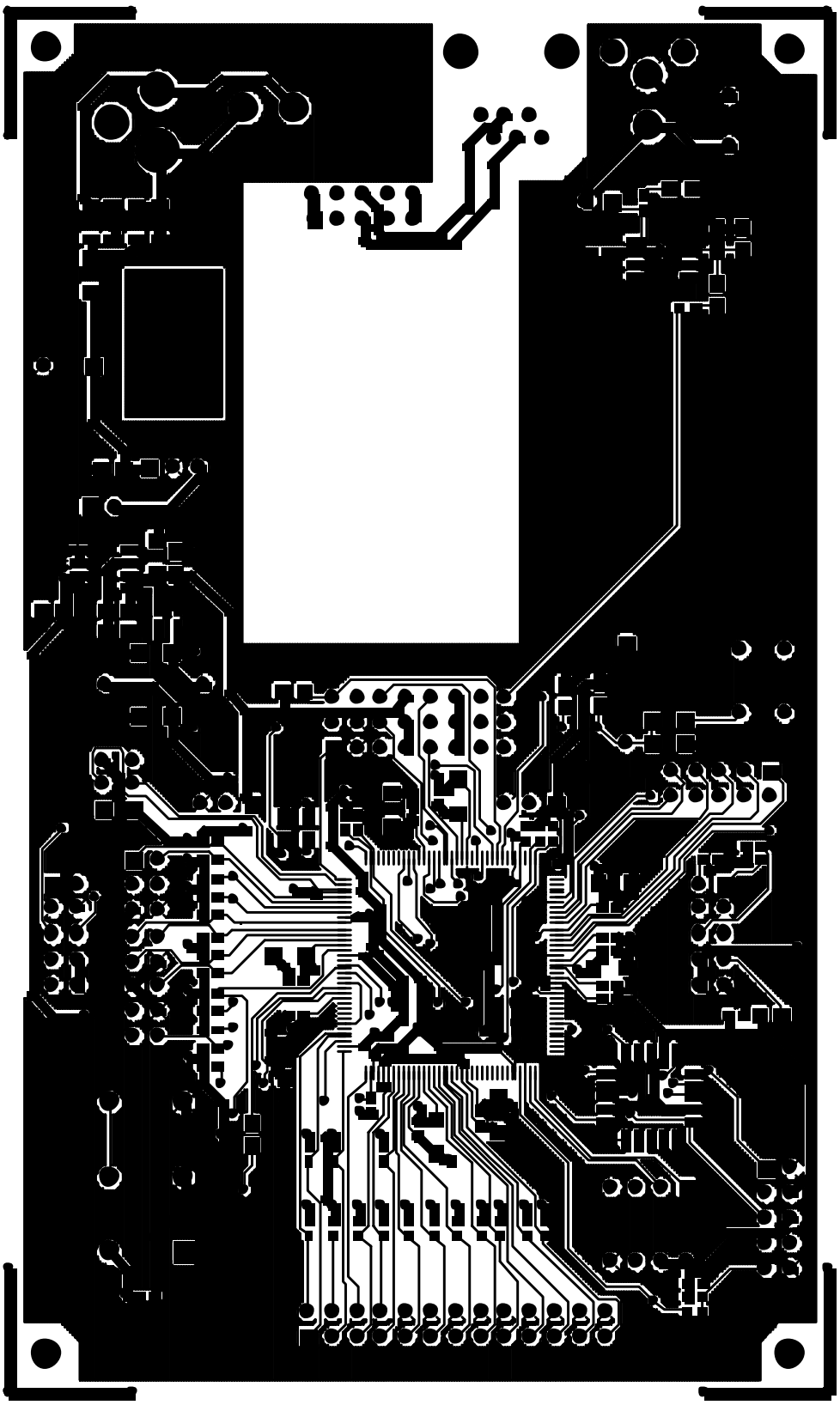


Figure 22. Si30xx Motherboard Component Layer

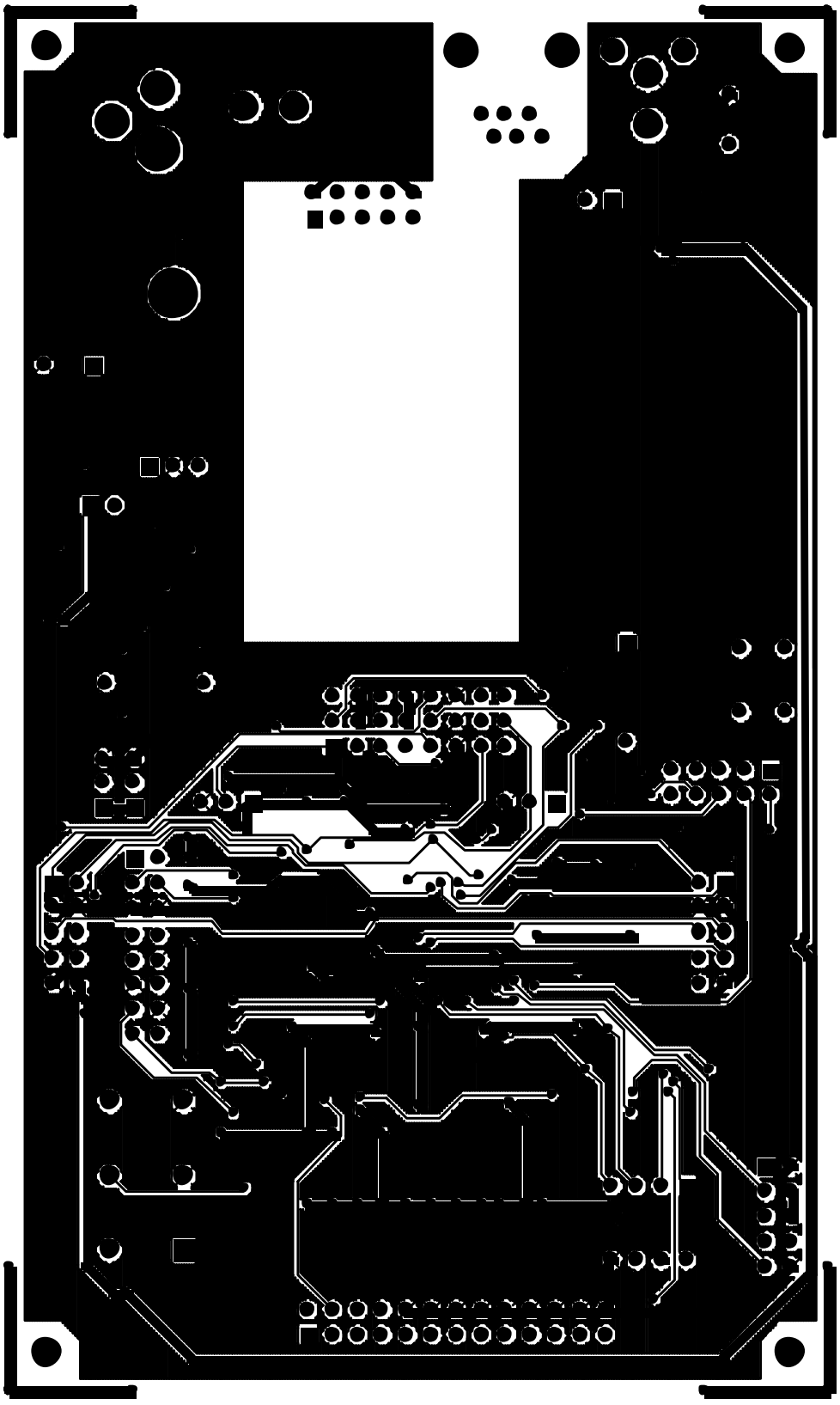


Figure 23. Si30xx Motherboard Solder Layer

**Notes:**

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