TPS560430-Q1 Evaluation Module

The Texas Instruments TPS560430QEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS560430-Q1 wide-input synchronous buck regulator. This document describes the setup and the input / output connections of the EVM. Included are the board layout, schematic and bill of materials.

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1 Introduction

The Texas Instruments TPS560430QEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS560430-Q1 wide-input buck regulator.
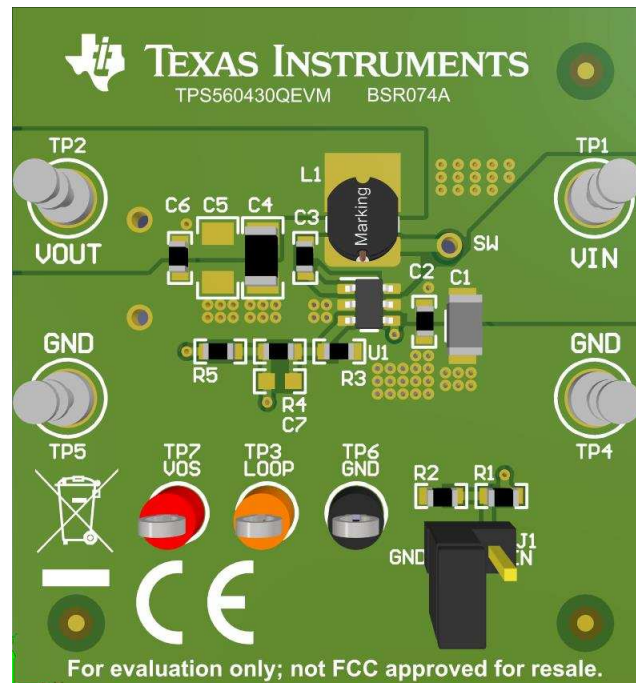

Figure 1. TPS560430QEVM Board

EVM Features

- 7.5-V to 36-V input voltage range
- Accurate 5-V output
- Up to 600-mA output current
- Switching frequency 2.1 MHz
- Hiccup mode short current protection
- Internal compensation

The EVM contains one DC/DC converter (See Table 1)

Table 1. Device and Package Configurations

CONVERTER	EVM	DEVICE	PACKAGE
U1	TPS560430QEVM	TPS560430-Q1	SOT23-6

2 Setup

This section describes the jumpers and connectors on the EVM and how to properly connect, set up and use the TPS560430XFEVM.

2.1 Input/Output Connector Description

VIN — Terminal TP1 – is the power input terminal for the converter. Adjacent to it is the GND reference ground. Use this terminal to attach the EVM to a cable harness.

VOUT — Terminal TP2 – is the regulated output voltage for the converter. Adjacent to it is the GND reference ground.

GND — Terminal TP4, TP5 – are the ground reference for the converter. Use these terminals to attach the EVM to a cable harness.

EN — Jumper J1 – is used to enable the switch-mode converter. The device will be enabled when the EN pin is high, and disabled when low. EN turn off trip point also can be programmed by changing R1 or R2. Refer to TPS560430 datasheet for enable and adjustable under-voltage lockout.
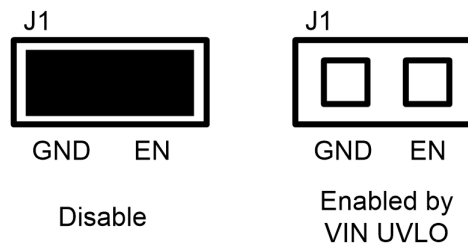

Figure 2. Enable Jumper Setting

Testpoint — TP3, TP6, TP7 – these are test points used for loop response measurements.

2.2 Adjusting the Output Voltage

If other outputs need to be configured, adjust the feedback resistors using the following equation.

$$V_{OUT} = V_{REF} \times (1 + (R4 / R3))$$

where

- V_{REF} is 1.0 V

(1)
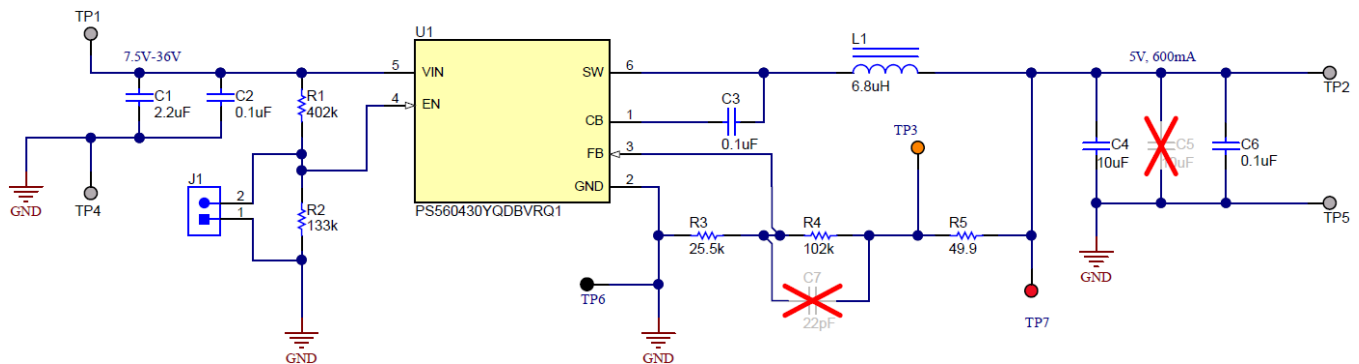
3 TPS560430QEVM Schematic

Figure 3. TPS560430QEVM Schematic

4   Board Layout

Figure 4 and Figure 5 show the board layout for the TPS560430QEVM. The PCB consists of a 2-layer design. The board size is 38 mm x 41 mm, 1-oz copper planes is applied on both layers.
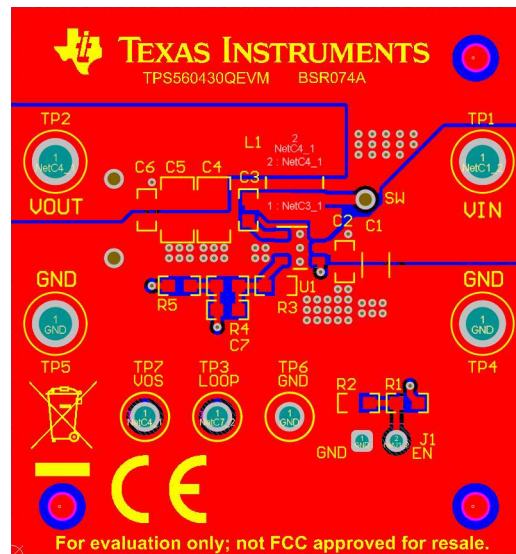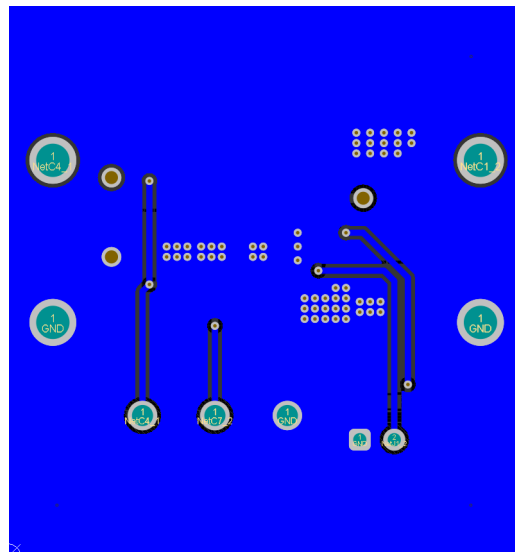

Figure 4. Top Layer

Figure 5. Bottom Layer

5 List of Materials

Table 2. TPS560430XFEVM List of Materials

DES	DESCRIPTION	PART NUMBER	MANUFACTURE	QUANTITY
C2, C3, C6	Capacitor, ceramic, 0.1 µF, 50 V, ±10%, X7R, 0603	GRM188R71H104KA93D		3
C1	Capacitor, ceramic, 2.2 µF, 50 V, ±10%, X7R, 1206	GRM31CR71H225KA88L		1
C4	Capacitor, ceramic, 10 µF, 10 V, ±10%, X7R, 1206	C3216X7R1A106M160AC		1
J1	Header, 100 mil, 2 x 1, gold, TH	TSW-102-07-G-S		1
L1	Inductor, Shielded Drum Core, Ferrite, 6.8 uH, 1.54 A, 0.131 ohm, SMD	744773068		1
R1	Resistor, 402 kΩ, 1%, 0.1 W, 0603	CRCW0603402KFKEA		1
R2	Resistor, 133 kΩ, 1%, 0.1 W, 0603	CRCW0603133KFKEA		1
R3	Resistor, 25.5 kΩ, 1%, 0.1 W, 0603	CRCW060325K5FKEA		1
R4	Resistor, 102 kΩ, 1%, 0.1 W, 0603	CRCW0603102KFKEA		1
R5	Resistor, 49.9 Ω, 1%, 0.1 W, 0603	CRCW060349R9FKEA		1
SH-J1	Shunt, 100 mil, flash gold, black	SPC02SYAN		1
TP1, TP2, TP4, TP5	Terminal, turret, TH, double	1502-2		4
TP3	Test point, compact, orange, TH	5008		1
TP6	Test point, compact, black, TH	5006		1
TP7	Test point, compact, red, TH	5005		1
U1	Device, 36-V, 600-mA, Synchronous Buck Regulator	PS560430YQDBVRQ1	Texas Instruments	1

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