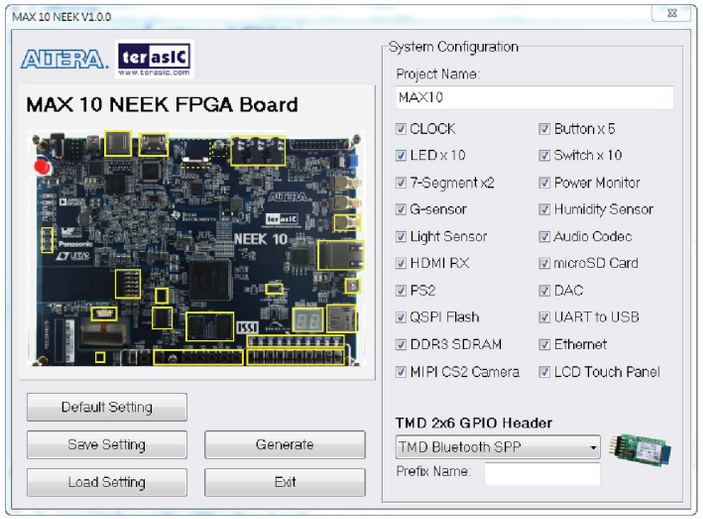
6 System Builder

This tool allows users to create customizable Quartus II projects depending on their requirements. The top-level design file, pin assignments, and I/O standard settings for the MAX 10 NEEK will be generated automatically from this tool. This tool can be found in the “Tools” folder of System CD.



7 Getting Help

For further discussion, support, and resources, please go to:

http://max10.terasic.com

If you encounter any problem, please contact us below

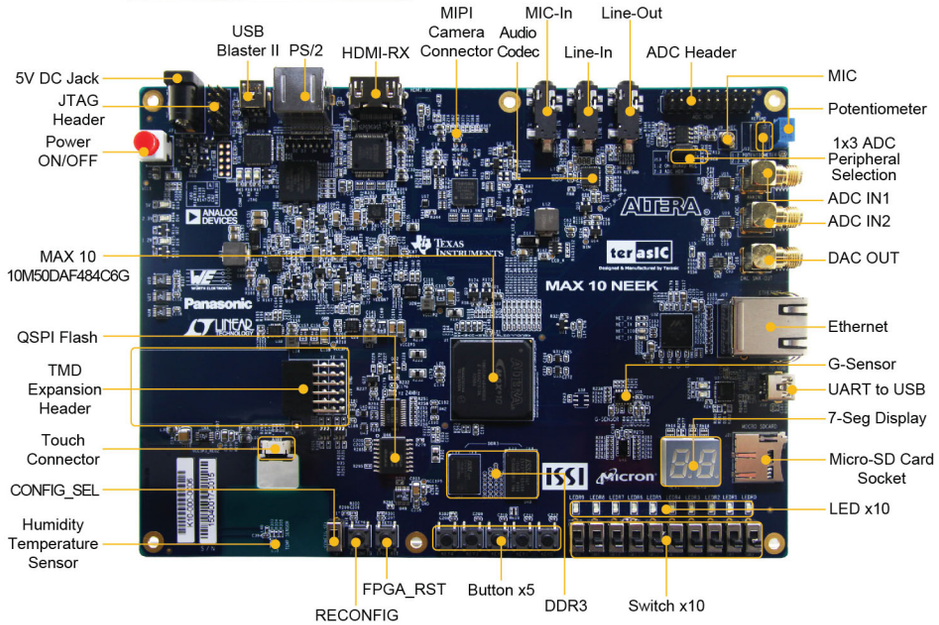
Email: support@terasic.com Tel: +886-3-575-0880

CPT-3251-00

terasIC
www.terasic.com
ALTERA

MAX 10 NEEK

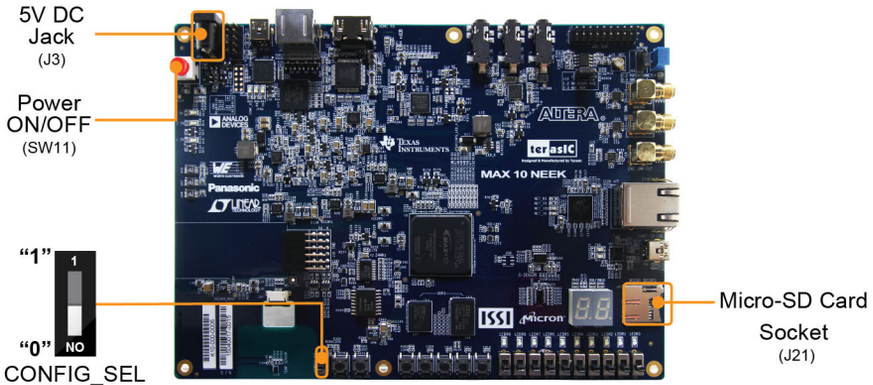
Quick Start Guide



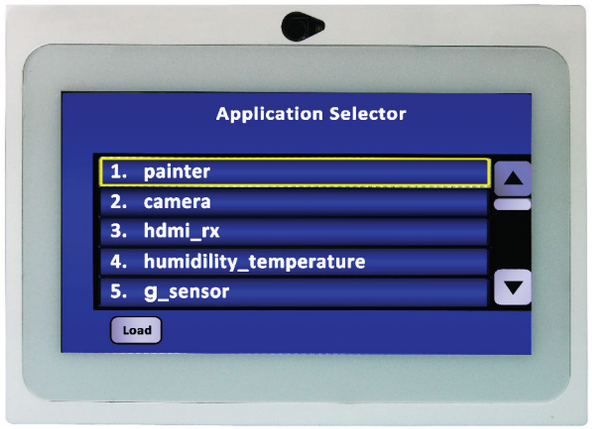
1 What’s in the Box?

1. MAX 10 NEEK Board
2. MAX 10 NEEK Quick Start Guide
3. Type A to Mini-B USB Cable
4. Power Adapter(5V/3A)
5. Micro-SD Card

2 Perform Power-on Test



1. Insert the provided Micro-SD card to the Micro-SD card socket.
2. The CONFIG_SEL switch is set to "0".
3. Connect the power adapter to the power jack (J3) on the MAX 10 NEEK.
4. Turn on the development board by pressing the red power button (SW11).
5. The GUI of Applicaiton Selector utility will appear on the LCD.
6. Scroll to select a demonstration using the side-bar.
7. Tap on the Load button to run a demonstration



3 Contents of the MAX 10 NEEK System CD

Users can download the MAX 10 NEEK System CD from this link:

http://cd-max10.terasic.com

MAX 10 NEEK System CD Contents	
Directory Name	***Contents***
Datasheet	Contains the datasheets of the components on the MAX 10 NEEK
Demonstrations	Contains design examples for MAX 10 NEEK application
Factory_Recovery	Contains the default code of Application Selector and recovery procedure
Schematic	Contains the schematics of MAX 10 NEEK
Tool	Contains the design tools for MAX 10 NEEK
UserManual	Contains the manuals of MAX 10 NEEK

4 Start Your First FPGA Design

Users can refer to the document My_First_FPGA.pdf found in the MAX 10 NEEK System CD manual folder.

This document describes the complete FPGA design flow, including:

1. Create a new Quartus II project.
2. Add user logic and utilize MegaCore IPs.
3. Download .sof file to the FPGA to view the result.

5 Start Your First Nios II Design

Users can refer to the documnet My_First_Nios II.pdf found in the MAX 10 NEEK system CD manual folder.

This document describes the complete Nios II design flow, including:

1. Creating a new Quartus II project.
2. Creating a new Qsys system including Nios II processor and other peripherals onboard.
3. Creating a new Nios II project for hello program.
4. Download .sof and .elf files to the FPGA to view the result.