

MAX16033–MAX16040

Low-Power Battery-Backup Circuits in Small μ DFN Packages

General Description

The MAX16033–MAX16040 supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (μ P) systems. The devices significantly improve system reliability and accuracy compared to other ICs or discrete components. The MAX16033–MAX16040 provide μ P reset, backup-battery switchover, power-fail warning, watchdog, and chip-enable gating features.

The MAX16033–MAX16040 operate from supply voltages up to 5.5V. The factory-set reset threshold voltage ranges from 2.32V to 4.63V. The devices feature a manual-reset input (MAX16033/MAX16037), a watchdog timer input (MAX16034/MAX16038), a battery-on output (MAX16035/MAX16039), an auxiliary adjustable-reset input (MAX16036/MAX16040), and chip-enable gating (MAX16033–MAX16036). Each device includes a power-fail comparator and offers an active-low push-pull reset or an active-low open-drain reset.

The MAX16033–MAX16040 are available in 2mm x 2mm, 8-pin or 10-pin μ DFN packages and are fully specified from -40°C to $+85^{\circ}\text{C}$.

Applications

- Portable/Battery-Powered Equipment
- POS Equipment
- Critical μ P/ μ C Power Monitoring
- Set-Top Boxes
- Controllers
- Computers
- Fax Machines
- Industrial Control
- Real-Time Clocks
- Intelligent Instrument

Pin Configurations and Typical Operating Circuit appear at end of data sheet

Selector Guide

PART	$\overline{\text{MR}}$	WATCHDOG	BATTON	RESETIN	$\overline{\text{CEIN}}/\overline{\text{CEOUT}}$	PFI, $\overline{\text{PFO}}$	PIN-PACKAGE
MAX16033_	✓				✓	✓	10 μ DFN-10
MAX16034_		✓			✓	✓	10 μ DFN-10
MAX16035_			✓		✓	✓	10 μ DFN-10
MAX16036_				✓	✓	✓	10 μ DFN-10
MAX16037_	✓					✓	8 μ DFN-8
MAX16038_		✓				✓	8 μ DFN-8
MAX16039_			✓			✓	8 μ DFN-8
MAX16040_				✓		✓	8 μ DFN-8

Note: Replace “_” with L for push-pull or P for open-drain $\overline{\text{RESET}}$ and $\overline{\text{PFO}}$ outputs.

Features

- Low 1.2V Operating Supply Voltage
- Precision Monitoring of 5.0V, 3.3V, 3.0V, and 2.5V Power-Supply Voltages
- Independent Power-Fail Comparator
- Debounced Manual-Reset Input
- Watchdog Timer, 1.6s Timeout
- Battery-On Output Indicator
- Auxiliary User-Adjustable RESETIN
- Low 13 μ A Quiescent Supply Current
- Two Available Output Structures:
 - Active-Low Push-Pull Reset
 - Active-Low Open-Drain Reset
- Active-Low Reset Valid Down to 1.2V
- Power-Supply Transient Immunity
- 140ms (min) Reset Timeout Period
- Small 2mm x 2mm, 8-Pin and 10-Pin μ DFN Packages

Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE
MAX16033LLB_+_T	-40°C to $+85^{\circ}\text{C}$	10 μ DFN
MAX16033PLB_+_T	-40°C to $+85^{\circ}\text{C}$	10 μ DFN
MAX16034LLB_+_T	-40°C to $+85^{\circ}\text{C}$	10 μ DFN
MAX16034PLB_+_T	-40°C to $+85^{\circ}\text{C}$	10 μ DFN

*These parts offer a choice of reset threshold voltages. From the Reset Threshold Ranges table, insert the desired threshold voltage code in the blank to complete the part number. See the Selector Guide for a listing of device features.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Ordering Information continued on last page.



Absolute Maximum Ratings

Terminal Voltages (with respect to GND)

V_{CC} , BATT, OUT.....	-0.3V to +6V
\overline{RESET} (open drain), \overline{PFO} (open drain)	-0.3V to +6V
\overline{RESET} (push-pull), \overline{PFO} (push-pull), BATTON, RESETIN, WDI MR, \overline{CEIN} , \overline{CEOUT} , PFI.....	-0.3V to ($V_{OUT} + 0.3V$)

Input Current

V_{CC} Peak.....	1A
V_{CC} Continuous.....	250mA
BATT Peak.....	250mA
BATT Continuous.....	40mA
GND.....	75mA

Output Current

OUT.....	Short-Circuit Protected for up to 5s
\overline{RESET} , BATTON.....	20mA
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
8-Pin μ DFN (derate 4.8mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$).....	380.6mW
10-Pin μ DFN (derate 5mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$).....	402.8mW
Operating Temperature Range	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{CC} = 2.25V$ to $5.5V$, $V_{BATT} = 3V$, \overline{RESET} not asserted, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, for MAX16039PLA31+T, $T_A = -55^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC} , V_{BATT}	No load (Note 2)	0		5.5	V
Supply Current	I_{CC}	No load, $V_{CC} > V_{TH}$	$V_{CC} = 2.8V$	13	30	μA
			$V_{CC} = 3.6V$	16	35	
			$V_{CC} = 5.5V$	22	50	
Supply Current in Battery Backup Mode		$V_{BATT} = 2.8V$, $V_{CC} = 0V$, excluding I_{OUT}	$T_A = +25^\circ\text{C}$		1	μA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		2	
			$T_A = -55^\circ\text{C}$ (MAX16039PLA31+T only)		10	
BATT Standby Current (Note 3)	I_{BATT}	$(V_{BATT} + 0.2V) < V_{CC} < 5.5V$	$T_A = +25^\circ\text{C}$	-0.1	+0.02	μA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.3	+0.02	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		+0.06	
V_{CC} to OUT On-Resistance	R_{ON}	$V_{CC} = 4.75V$, $V_{CC} > V_{TH}$, $I_{OUT} = 150\text{mA}$			3.1	Ω
		$V_{CC} = 3.15V$, $V_{CC} > V_{TH}$, $I_{OUT} = 65\text{mA}$			3.7	
		$V_{CC} = 2.5V$, $V_{CC} > V_{TH}$, $I_{OUT} = 25\text{mA}$			4.6	
Output Voltage in Battery Backup Mode	V_{OUT}	$V_{BATT} = 4.50V$, $V_{CC} = 0V$, $I_{OUT} = 20\text{mA}$			$V_{BATT} - 0.2$	V
		$V_{BATT} = 3.15V$, $V_{CC} = 0V$, $I_{OUT} = 10\text{mA}$			$V_{BATT} - 0.15$	
		$V_{BATT} = 2.5V$, $V_{CC} = 0V$, $I_{OUT} = 5\text{mA}$			$V_{BATT} - 0.15$	
Battery-Switchover Threshold	V_{SW}	$V_{CC} - V_{BATT}$, $V_{CC} < V_{TH}$	V_{CC} rising		0	mV
			V_{CC} falling		-40	

Electrical Characteristics (continued)

(V_{CC} = 2.25V to 5.5V, V_{BATT} = 3V, \overline{RESET} not asserted, T_A = -40°C to +85°C, for MAX16039PLA31+T, T_A = -55°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET OUTPUT						
Reset Threshold	V_{TH}	MAX160__L_46	4.50	4.63	4.75	V
		MAX160__L_44	4.25	4.38	4.50	
		MAX160__L_31	3.00	3.08	3.15	
		MAX160__L_29	2.85	2.93	3.00	
		MAX160__L_26	2.55	2.63	2.70	
		MAX160__L_23	2.25	2.32	2.38	
V_{CC} Falling Reset Delay		V_{CC} falling at 10V/ms		25		μ s
Reset Active Timeout Period	t_{RP}		140		280	ms
\overline{RESET} Output Low Voltage	V_{OL}	\overline{RESET} asserted	$I_{SINK} = 1.6mA, V_{CC} \geq 2.1V$		0.3	V
			$I_{SINK} = 100\mu A, V_{CC} \geq 1.2V$		0.4	
\overline{RESET} Output High Voltage	V_{OH}	MAX160__L only (push-pull), \overline{RESET} not asserted, $I_{SOURCE} = 500\mu A, V_{CC} \geq V_{TH(MAX)}$	0.8 x V_{CC}			V
\overline{RESET} Output Leakage Current	I_{LKG}	MAX160__P only (open drain), not asserted			1	μ A
POWER-FAIL COMPARATOR						
PFI Input Threshold	V_{PFI}	V_{PFI} falling	1.185	1.235	1.285	V
PFI Hysteresis				1		%
PFI Input Current		$V_{PFI} = 0V$ or V_{CC}	-100		+100	nA
\overline{PFO} Output Low Voltage	V_{OL}	Output asserted	$V_{CC} \geq 2.1V, I_{SINK} = 1.6mA$		0.3	V
			$V_{CC} \geq 1.2V, I_{SINK} = 100\mu A$		0.4	
\overline{PFO} Output High Voltage	V_{OH}	MAX160__L only (push-pull), $V_{CC} \geq V_{TH(MAX)}, I_{SOURCE} = 500\mu A$, output not asserted	0.8 x V_{CC}			V
\overline{PFO} Leakage Current		MAX160__P only (open drain), $V_{PFO} = 5.5V$, not asserted			1	μ A
\overline{PFO} Delay Time		$V_{PFI} + 100mV$ to $V_{PFI} - 100mV$		4		μ s
MANUAL RESET (MAX16033/MAX16037)						
\overline{MR} Input Voltage	V_{IL}		0.3 x V_{CC}			V
	V_{IH}		0.7 x V_{CC}			
Pullup Resistance to V_{CC}			20		165	k Ω
Minimum Pulse Width			1			μ s
Glitch Immunity		$V_{CC} = 3.3V$		100		ns
\overline{MR} to Reset Delay				120		ns

Electrical Characteristics (continued)

($V_{CC} = 2.25V$ to $5.5V$, $V_{BATT} = 3V$, \overline{RESET} not asserted, $T_A = -40^\circ C$ to $+85^\circ C$, for MAX16039PLA31+T, $T_A = -55^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG (MAX16034/MAX16038)						
Watchdog Timeout Period	t_{WD}		1.00	1.65	2.25	s
Minimum WDI Input Pulse Width	t_{WDI}	(Note 4)	100			ns
WDI Input Voltage	V_{IL}			$0.3 \times V_{CC}$		V
	V_{IH}		$0.7 \times V_{CC}$			
WDI Input Current			-1.0		+1.0	μA
BATTON (MAX16035/MAX16039)						
Output Voltage	V_{OL}	$I_{SINK} = 3.2mA$, $V_{BATT} = 2.1V$			0.4	V
Output Short-Circuit Current		Sink current, $V_{CC} = 5V$		60		mA
		Source current, $V_{BATT} \geq 2V$	10	30	120	μA
RESETIN (MAX16036/MAX16040)						
RESETIN Threshold	V_{RTH}		1.185	1.235	1.285	V
RESETIN Input Current				0.01	25	nA
RESETIN to Reset Delay		($V_{RTH} + 100mV$) to ($V_{RTH} - 100mV$)		1.5		μs
CHIP-ENABLE GATING (MAX16033–MAX16036)						
\overline{CEIN} Leakage Current		\overline{RESET} asserted			± 1	μA
\overline{CEIN} to \overline{CEOUT} Resistance		\overline{RESET} not asserted, $V_{CC} = V_{TH(MAX)}$, $V_{\overline{CEIN}} = V_{CC}/2$, $I_{SINK} = 10mA$			100	Ω
\overline{CEOUT} Short-Circuit Current		\overline{RESET} asserted, $V_{\overline{CEOUT}} = 0V$		1	2.0	mA
\overline{CEIN} to \overline{CEOUT} Propagation Delay (Note 4)		50 Ω source impedance driver, $C_{LOAD} = 50pF$	$V_{CC} = 4.75V$	1.5	7	ns
			$V_{CC} = 3.15V$	2	9	
\overline{CEOUT} Output-Voltage High		$V_{CC} = 5V$, $V_{CC} \geq V_{BATT}$, $I_{SOURCE} = 100\mu A$	$0.7 \times V_{CC}$		V	
		$V_{CC} = 0V$, $V_{BATT} \geq 2.2V$, $I_{SOURCE} = 1\mu A$	$V_{BATT} - 0.1$			
\overline{RESET} to \overline{CEOUT} Delay				1		μs

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$. All overtemperature limits are guaranteed by design.

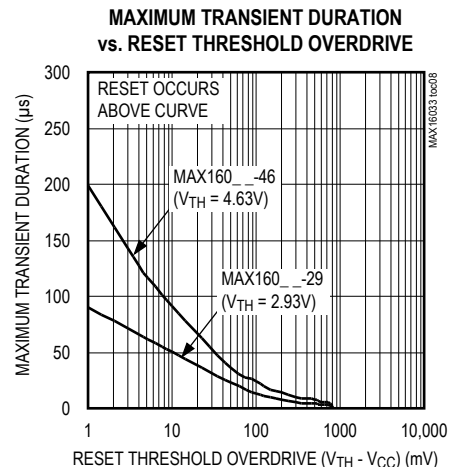
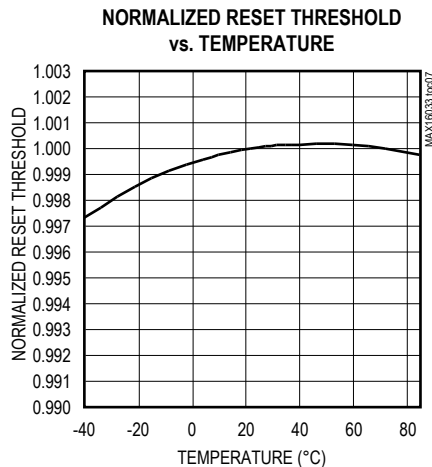
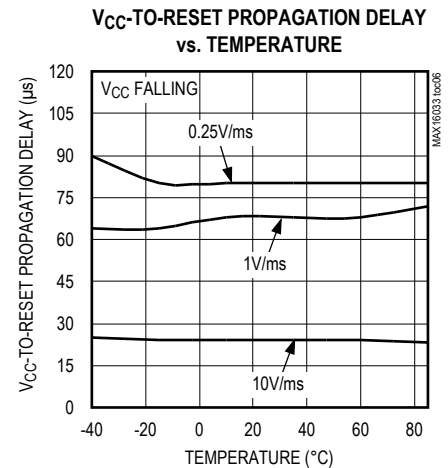
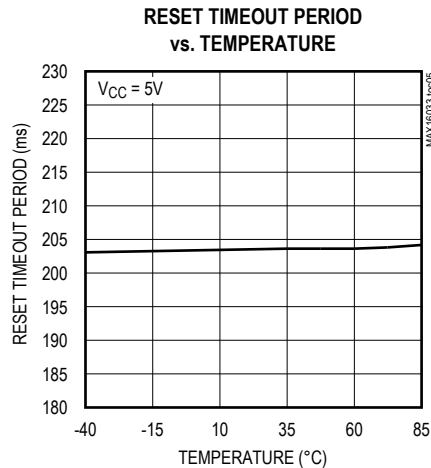
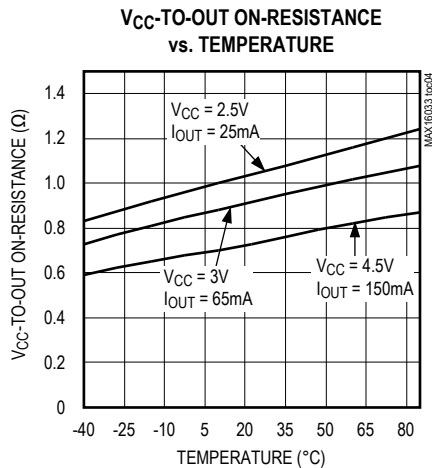
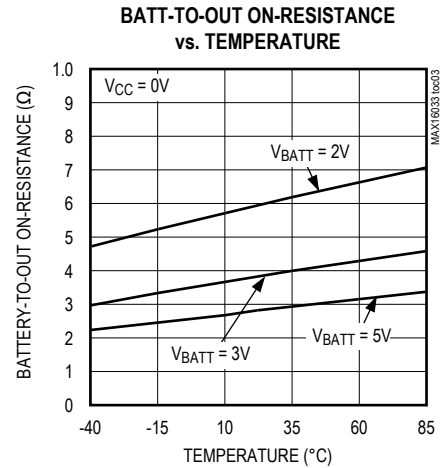
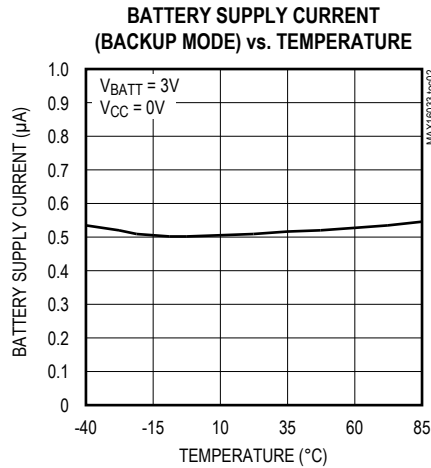
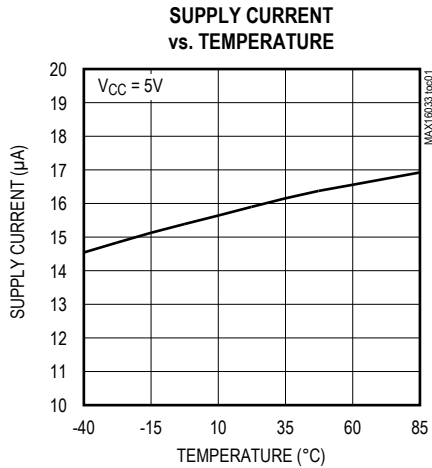
Note 2: V_{BATT} can be 0V any time, or V_{CC} can go down to 0V if V_{BATT} is active (except at startup).

Note 3: Positive current flows into BATT.

Note 4: Guaranteed by design.

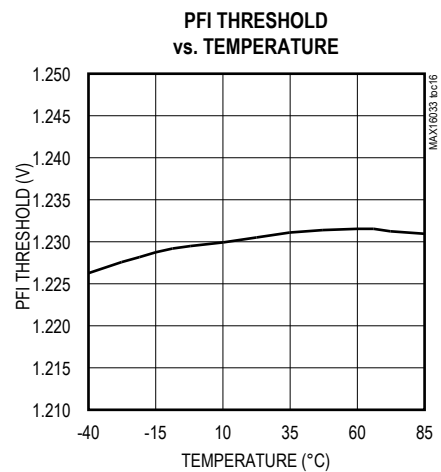
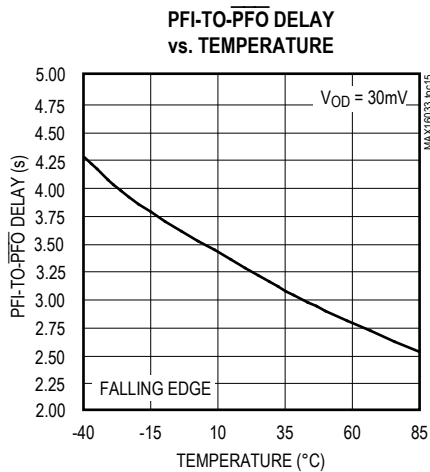
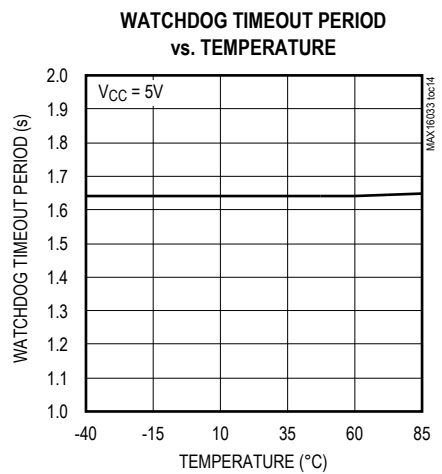
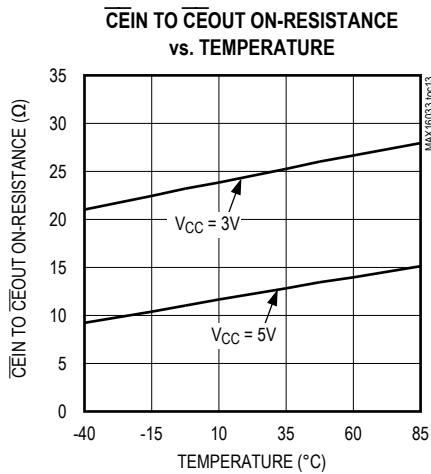
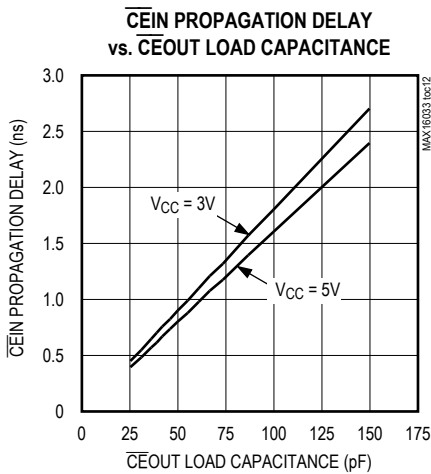
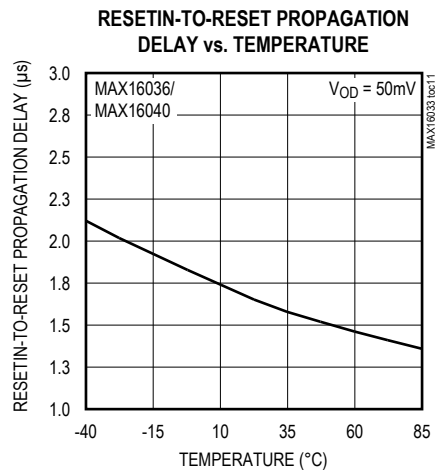
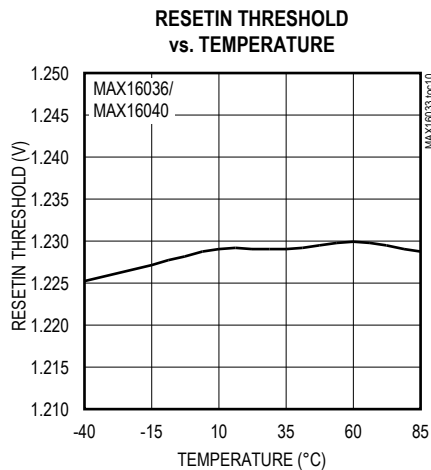
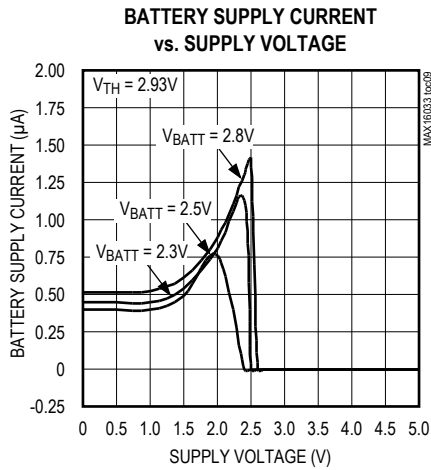
Typical Operating Characteristics

(TA = +25°C, unless otherwise noted.)



Typical Operating Characteristics (continued)

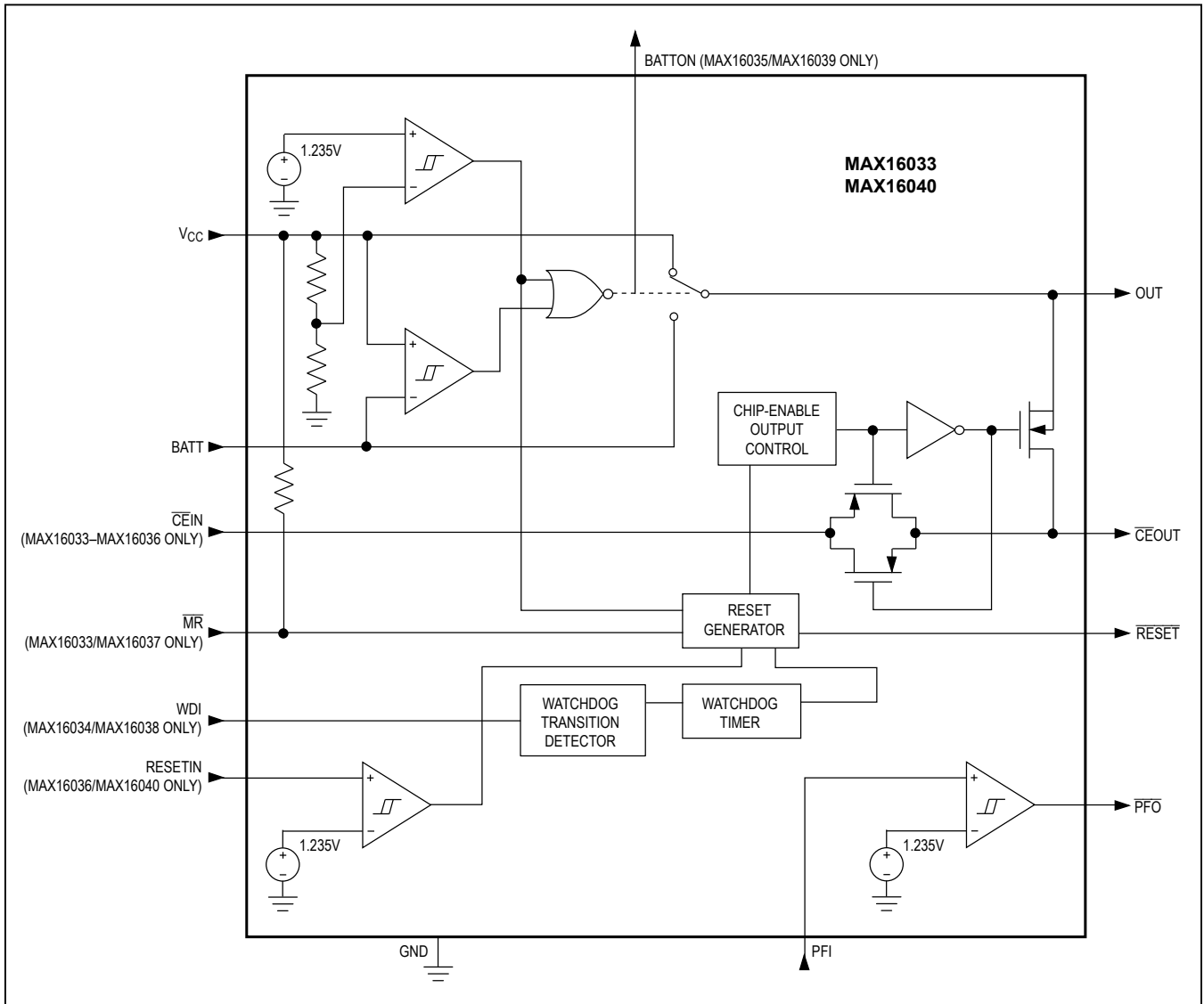
(TA = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
MAX16033– MAX16036 (10-pin μ DFN)	MAX16037– MAX16040 (8-pin μ DFN)		
1	1	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ remains low when V_{CC} is below the reset threshold (V_{TH}), the manual-reset input is low, or RESE TIN is low. It asserts low in pulses when the internal watchdog times out. $\overline{\text{RESET}}$ remains low for the reset timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after the manual-reset input goes from low to high, after RESE TIN goes high, or after the watchdog triggers a reset event. The MAX160__L is an active-low push-pull output, while the MAX160__P is an active-low open-drain output.
2	—	$\overline{\text{CEIN}}$	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to GND or OUT if not used.
3	2	PFI	Power-Fail Input. $\overline{\text{PFO}}$ goes low when V_{PFI} falls below 1.235V.
4	3	GND	Ground
5	4	$\overline{\text{MR}}$	Manual-Reset Input (MAX16033/MAX16037). Driving $\overline{\text{MR}}$ low asserts $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ remains asserted as long as MR is low and for the reset timeout period (t_{RP}) after $\overline{\text{MR}}$ transitions from low to high. Leave unconnected, or connect to V_{CC} if not used. $\overline{\text{MR}}$ has an internal 20k Ω pullup to V_{CC} .
		WDI	Watchdog Input (MAX16034/MAX16038). If WDI remains high or low for longer than the watchdog timeout period (t_{WD}), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period (t_{RP}). The internal watchdog clears whenever $\overline{\text{RESET}}$ asserts or whenever WDI sees a rising or falling edge (Figure 2).
		BATTON	Battery-On Output (MAX16035/MAX16039). BATTON goes high during battery backup mode.
		RESE TIN	Reset Input (MAX16036/MAX16040). When RESE TIN falls below 1.235V, $\overline{\text{RESET}}$ asserts. $\overline{\text{RESET}}$ remains asserted as long as RESE TIN is low and for at least t_{RP} after RESE TIN goes high.
6	5	$\overline{\text{PFO}}$	Active-Low Power-Fail Output. $\overline{\text{PFO}}$ goes low when V_{PFI} falls below 1.235V. $\overline{\text{PFO}}$ stays low until V_{PFI} goes above 1.235V. $\overline{\text{PFO}}$ also goes low when V_{CC} falls below the reset threshold voltage.
7	6	V_{CC}	Supply Voltage, 1.2V to 5.5V
8	7	OUT	Output. OUT sources from V_{CC} when $\overline{\text{RESET}}$ is not asserted and from the greater of V_{CC} or BATT when V_{CC} is below the reset threshold voltage.
9	8	BATT	Backup-Battery Input. When V_{CC} falls below the reset threshold, OUT switches to BATT if V_{BATT} is 40mV greater than V_{CC} . When V_{CC} rises above V_{BATT} , OUT switches to V_{CC} . The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.
10	—	$\overline{\text{CEOUT}}$	Chip-Enable Output. $\overline{\text{CEOUT}}$ goes low only when $\overline{\text{CEIN}}$ is low and reset is not asserted. When $\overline{\text{CEOUT}}$ is disconnected from $\overline{\text{CEIN}}$, $\overline{\text{CEOUT}}$ is actively pulled up to OUT.

Pin Description (continued)



Detailed Description

The *Typical Operating Circuit* shows a typical connection for the MAX16033–MAX16040. OUT powers the static random-access memory (SRAM). If V_{CC} is greater than the reset threshold (V_{TH}), or if V_{CC} is lower than V_{TH} but higher than V_{BATT} , V_{CC} is connected to OUT. If V_{CC} is lower than V_{TH} and V_{CC} is less than V_{BATT} , BATT is connected to OUT. OUT supplies up to 200mA from V_{CC} . In battery-backup mode, an internal MOSFET connects the backup battery to OUT. The on-resistance of the MOSFET is a function of the backup-battery voltage and temperature and is shown in the BATT-to-OUT On-Resistance vs. Temperature graph in the *Typical Operating Characteristics*.

Chip-Enable Signal Gating (MAX16033–MAX16036 Only)

The MAX16033–MAX16036 provide internal gating of chip-enable (\overline{CE}) signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure or brownout condition. During normal operation, the \overline{CE} gate is enabled and passes all \overline{CE} transitions. When reset asserts, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX16033–MAX16036 provide a series transmission gate from \overline{CEIN} to \overline{CEOUT} . A 2ns (typ) propagation delay

from \overline{CEIN} to \overline{CEOUT} allows these devices to be used with most μ Ps and high-speed DSPs.

When \overline{RESET} is deasserted, \overline{CEIN} is connected to \overline{CEOUT} through a low on-resistance transmission gate. If \overline{CEIN} is high when \overline{RESET} is asserted, \overline{CEOUT} remains high regardless of any subsequent transitions on \overline{CEIN} during the reset event.

If \overline{CEIN} is low when \overline{RESET} is asserted, \overline{CEOUT} is held low for 1 μ s to allow completion of the read/write operation (Figure 1). After the 1 μ s delay expires, \overline{CEOUT} goes high and stays high regardless of any subsequent transitions on \overline{CEIN} during the reset event. When \overline{CEOUT} is disconnected from \overline{CEIN} , \overline{CEOUT} is actively pulled up to OUT.

The propagation delay through the chip-enable circuitry depends on both the source impedance of the drive to \overline{CEIN} and the capacitive loading at \overline{CEOUT} . The chip-enable propagation delay is specified from the 50% point of \overline{CEIN} to the 50% point of \overline{CEOUT} , using a 50 Ω driver and 50pF load capacitance. Minimize the capacitive load at \overline{CEOUT} and use a low output-impedance driver to minimize propagation delay.

In high-impedance mode, the leakage current at \overline{CEIN} is $\pm 1\mu A$ (max) over temperature. In low-impedance mode, the impedance of \overline{CEIN} appears as a 75 Ω resistor in series with the load at \overline{CEOUT} .

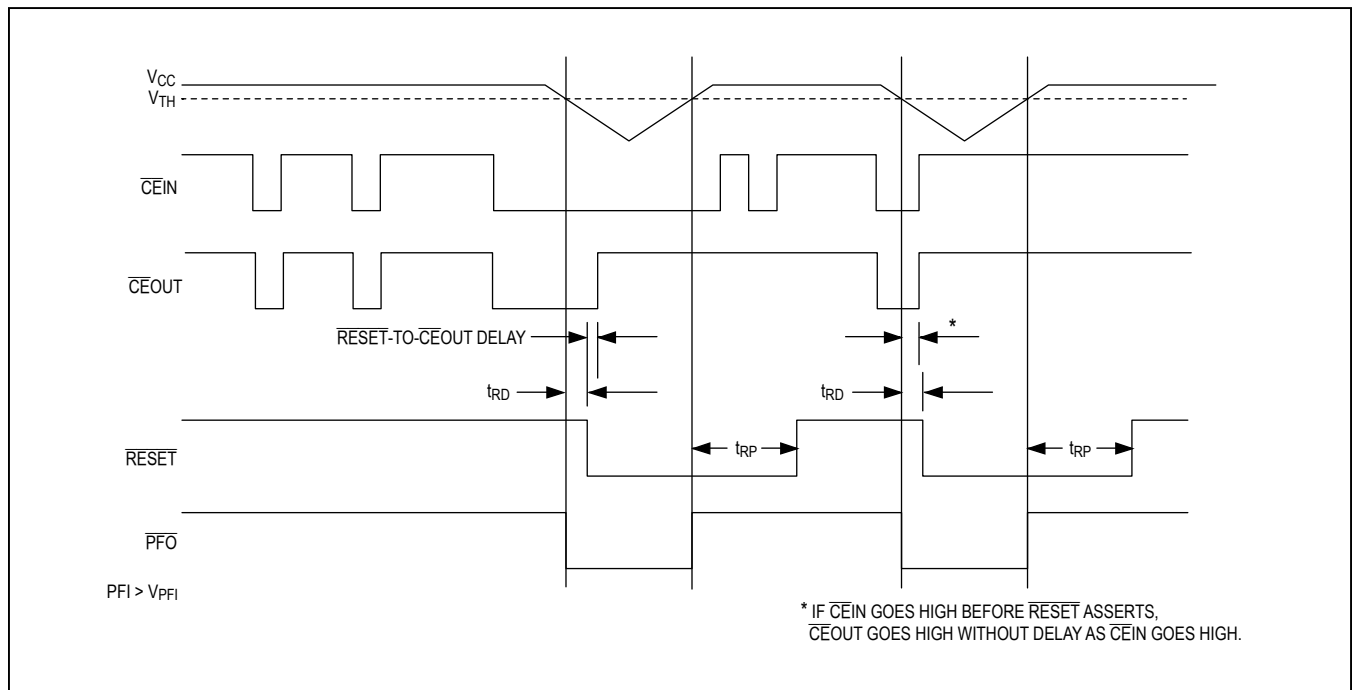


Figure 1. \overline{RESET} and Chip-Enable Timing

Backup-Battery Switchover

To preserve the contents of the RAM in a brownout or power failure, the MAX16033–MAX16040 automatically switch to back up the battery installed at BATT when the following two conditions are met:

- 1) V_{CC} falls below the reset threshold voltage.
- 2) V_{CC} is below V_{BATT} .

Table 1 lists the status of the inputs and outputs in battery-backup mode. The devices do not power up if the only voltage source is V_{BATT} . OUT only powers up from V_{CC} at startup.

Table 1. Input and Output Status in Battery-Backup Mode

PIN	STATUS
V_{CC}	Disconnected from OUT
OUT	Connected to BATT
BATT	Connected to OUT. Current drawn from the battery is less than $1\mu A$ (at $V_{BATT} = 2.8V$, excluding I_{OUT}) when $V_{CC} = 0V$.
RESET	Asserted
BATTON	High state
\overline{MR} , RESETIN, \overline{CEIN} , and WDI	Inputs ignored
\overline{CEOUT}	Connected to OUT
\overline{PFO}	Asserted

Manual-Reset Input (MAX16033/MAX16037 Only)

Many μP -based products require manual-reset capability, allowing the user or external logic circuitry to initiate a reset. For the MAX16033/MAX16037, a logic-low on \overline{MR} asserts RESET. RESET remains asserted while \overline{MR} is low and for a minimum of 140ms (t_{RP}) after it returns

high. \overline{MR} has an internal $20k\Omega$ (min) pullup resistor to V_{CC} . This input can be driven from TTL/CMOS logic outputs or with open-drain/collector outputs. Connect a normally open momentary switch from \overline{MR} to GND to create a manual-reset function; external debounce circuitry is not required. When driving \overline{MR} from long cables, or when using the device in a noisy environment, connect a $0.1\mu F$ capacitor from \overline{MR} to GND to provide additional noise immunity.

Watchdog Input (MAX16034/MAX16038 Only)

The watchdog monitors μP activity through the watchdog input (WDI). RESET asserts when the μP fails to toggle WDI. Connect WDI to a bus line or μP I/O line. A change of state (high to low, low to high, or a minimum 100ns pulse) resets the watchdog timer. If WDI remains high or low for longer than the watchdog timeout period (t_{WD}), the internal watchdog timer runs out and triggers a reset pulse for the reset timeout period (t_{RP}). The internal watchdog timer clears whenever RESET is asserted or whenever WDI sees a rising or falling edge. If WDI remains in either a high or low state, a reset pulse periodically asserts after every watchdog timeout period (t_{WD}); see Figure 2.

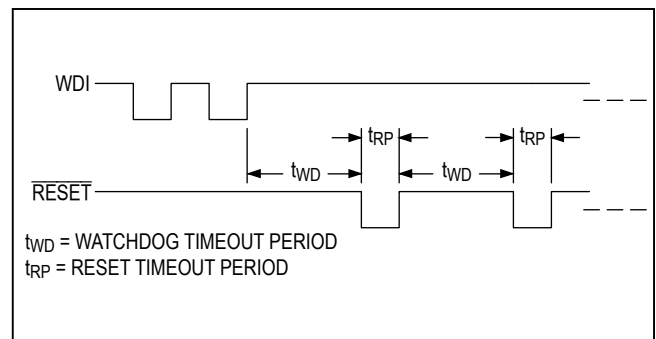


Figure 2. MAX16034/MAX16038 Watchdog Timeout Period and Reset Active Time

**BATTON Indicator
(MAX16035/MAX16039 Only)**

BATTON is a push-pull output that asserts high when in battery-backup mode. BATTON typically sinks 3.2mA at a 0.4V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from OUT. Use BATTON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher current applications (Figure 3).

**RESETIN Comparator
(MAX16036/MAX16040 Only)**

An internal 1.235V reference sets the RESETIN threshold voltage. RESET asserts when the voltage at RESETIN is below 1.235V. Use the RESETIN function to monitor a secondary power supply.

Use the following equations to set the reset threshold voltage (V_{RTH}) of the secondary power supply (see Figure 4):

$$V_{RTH} = V_{REF} (R1/R2 + 1)$$

where V_{REF} = 1.235V. To simplify the resistor selection, choose a value for R2 and calculate R1:

$$R1 = R2 [(V_{RTH}/V_{REF}) - 1]$$

Since the input current at RESETIN is 25nA (max), large values (up to 1MΩ) can be used for R2 with no significant loss in accuracy.

Power-Fail Comparator

The MAX16033–MAX16040 issue an interrupt (nonmaskable or regular) to the µP when a power failure occurs. The power line is monitored by two external resistors connected to the power-fail input (PFI). When the voltage at PFI falls below 1.235V, the power-fail output (PFO) drives the processor’s NMI input low. An earlier power-fail warning can be generated if the unregulated DC input of the regulator is available for monitoring. The MAX16033–MAX16040 turn off the power-fail comparator and force PFO low when V_{CC} falls below the reset threshold voltage (Figure 1). The MAX160__L devices provide push-pull PFO outputs. The MAX160__P devices provide open-drain PFO outputs.

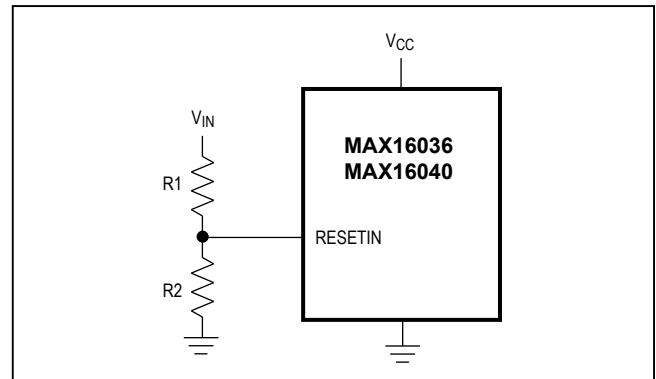


Figure 4. Setting RESETIN Voltage for the MAX16036/MAX16040

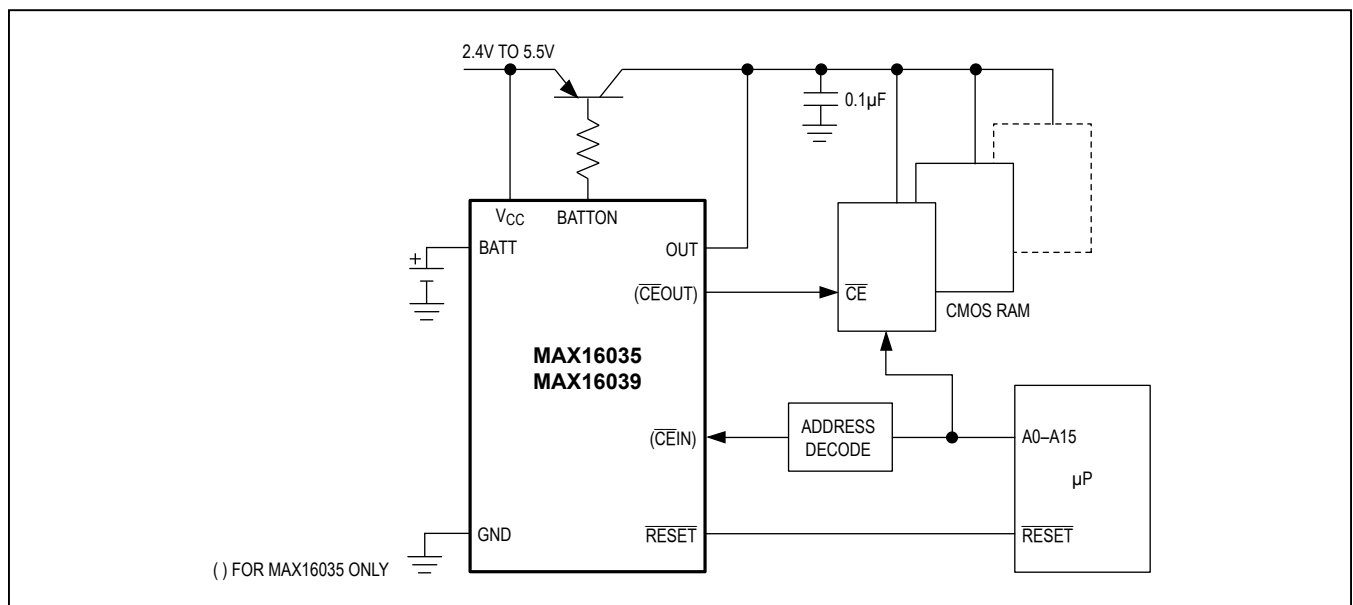


Figure 3. MAX16035/MAX16039 BATTON Driving an External Pass Transistor

RESET

A μ P’s reset input puts the μ P in a known state. The MAX16033–MAX16040 μ P supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ asserts when V_{CC} is below the reset threshold voltage and for at least 140ms (t_{RP}) after V_{CC} rises above the reset threshold. $\overline{\text{RESET}}$ also asserts when $\overline{\text{MR}}$ is low (MAX16033/MAX16037) or when RESETIN is below 1.235V (MAX16036/MAX16040). The MAX16034/MAX16038 watchdog function causes $\overline{\text{RESET}}$ to assert in pulses following a watchdog timeout (Figure 2). The MAX160__L devices provide push-pull $\overline{\text{RESET}}$ outputs. The MAX160__P devices provide open-drain $\overline{\text{RESET}}$ outputs.

Applications Information

Operation Without a Backup Power Source

The MAX16033–MAX16040 provide a battery-backup function. If a backup power source is not used, connect BATT to GND and OUT to V_{CC} .

Using a Super Cap as a Backup Power Source

Super caps are capacitors with extremely high capacitance, such as 0.47F. Figure 5 shows two methods to use a super cap as a backup power source. Connect the super cap through a diode to the 3V input (Figure 5a) or connect the super cap through a diode to 5V (Figure 5b), if a 5V supply is available. The 5V supply charges the super cap to a voltage close to 5V, allowing a longer backup period. Since V_{BATT} can be higher than V_{CC} while V_{CC} is above the reset threshold voltage, there are no special precautions required when using these μ P supervisors with a super cap.

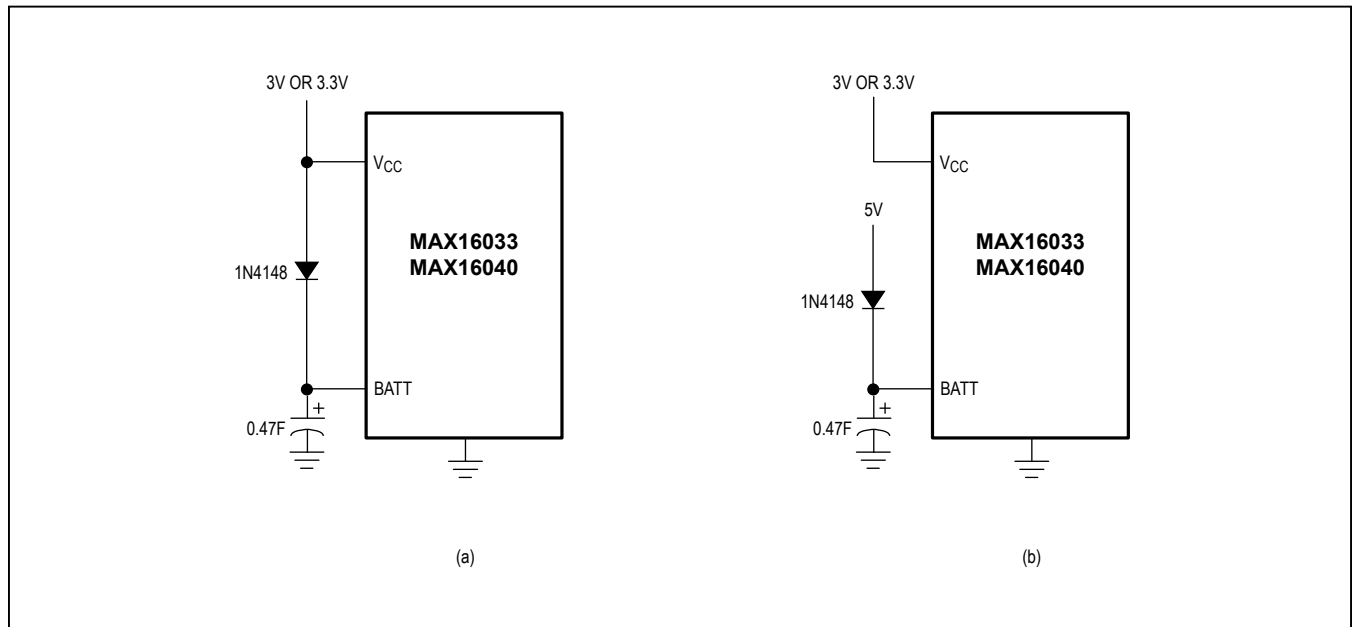


Figure 5. Using a Super Cap as a Backup Source

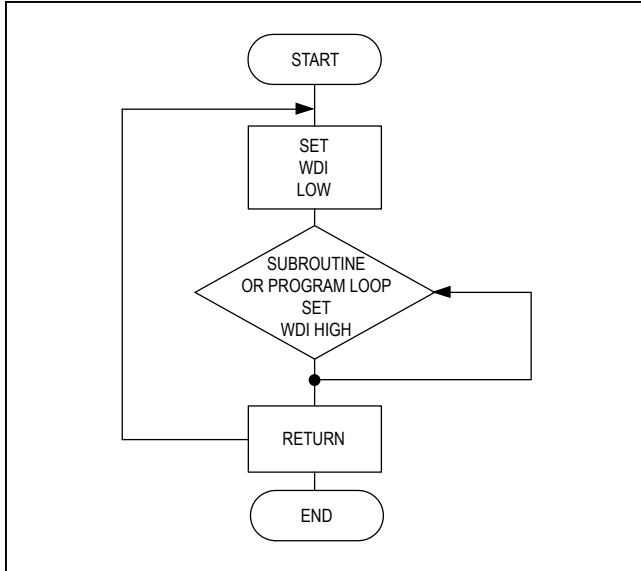


Figure 6. Watchdog Flow Diagram

Watchdog Software Considerations

One way to help the watchdog timer to monitor software execution more closely is to set and reset the watchdog at different points in the program, rather than pulsing the watchdog input periodically. Figure 6 shows a flow diagram where the I/O driving the watchdog is set low in the beginning of the program, set high at the beginning of every subroutine or loop, and set low again when the program returns to the beginning. If the program should hang in any subroutine, the watchdog would timeout and reset the μ P.

Replacing the Backup Battery

Decouple BATT to GND with a 0.1 μ F capacitor. The backup power source can be removed while V_{CC} remains valid without the danger of triggering a reset pulse. The device does not enter battery-backup mode when V_{CC} stays above the reset threshold voltage.

Power-Fail Comparator

Monitoring an Additional Power Supply

Monitor another voltage by connecting a resistive divider to PFI, as shown in Figure 7. The threshold voltage is:

$$V_{TH(PFI)} = 1.235 (R1/R2 + 1)$$

where $V_{TH(PFI)}$ is the threshold at which the monitored voltage will trip \overline{PFO} .

To simplify the resistor selection, choose a value for R2 and calculate R1:

$$R1 = R2 [(V_{TH(PFI)}/1.235) - 1]$$

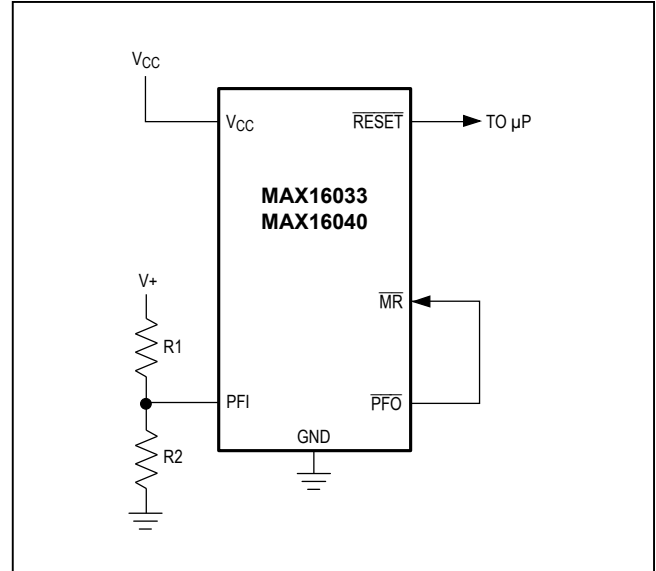


Figure 7. Monitoring an Additional Power Supply

Connect \overline{PFO} to \overline{MR} in applications that require \overline{RESET} to assert when the second voltage falls below its threshold. \overline{RESET} remains asserted as long as \overline{PFO} holds \overline{MR} low, and for 140ms (min) after \overline{PFO} goes high.

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator provides a typical hysteresis of 12mV, which is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider. Connect a voltage-divider between PFI and \overline{PFO} , as shown in Figure 8a, to provide additional noise immunity. Select the ratio of R1 and R2 such that V_{PFI} falls to 1.235V when V_{IN} drops to its trip point (V_{TRIP}). R3 adds hysteresis and is typically more than 10 times the value of R1 or R2. The hysteresis window extends above (V_H) and below (V_L) the original trip point, V_{TRIP} . Connecting an ordinary signal diode in series with R3, as shown in Figure 8b, causes the lower trip point (V_L) to coincide with the trip point without hysteresis (V_{TRIP}). This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. Set the current through R1 and R2 to be at least 10 μ A to ensure that the 100nA (max) PFI input current does not shift the trip point. Set R3 to be higher than 10k Ω to reduce the load at \overline{PFO} . Capacitor C1 adds additional noise rejection.

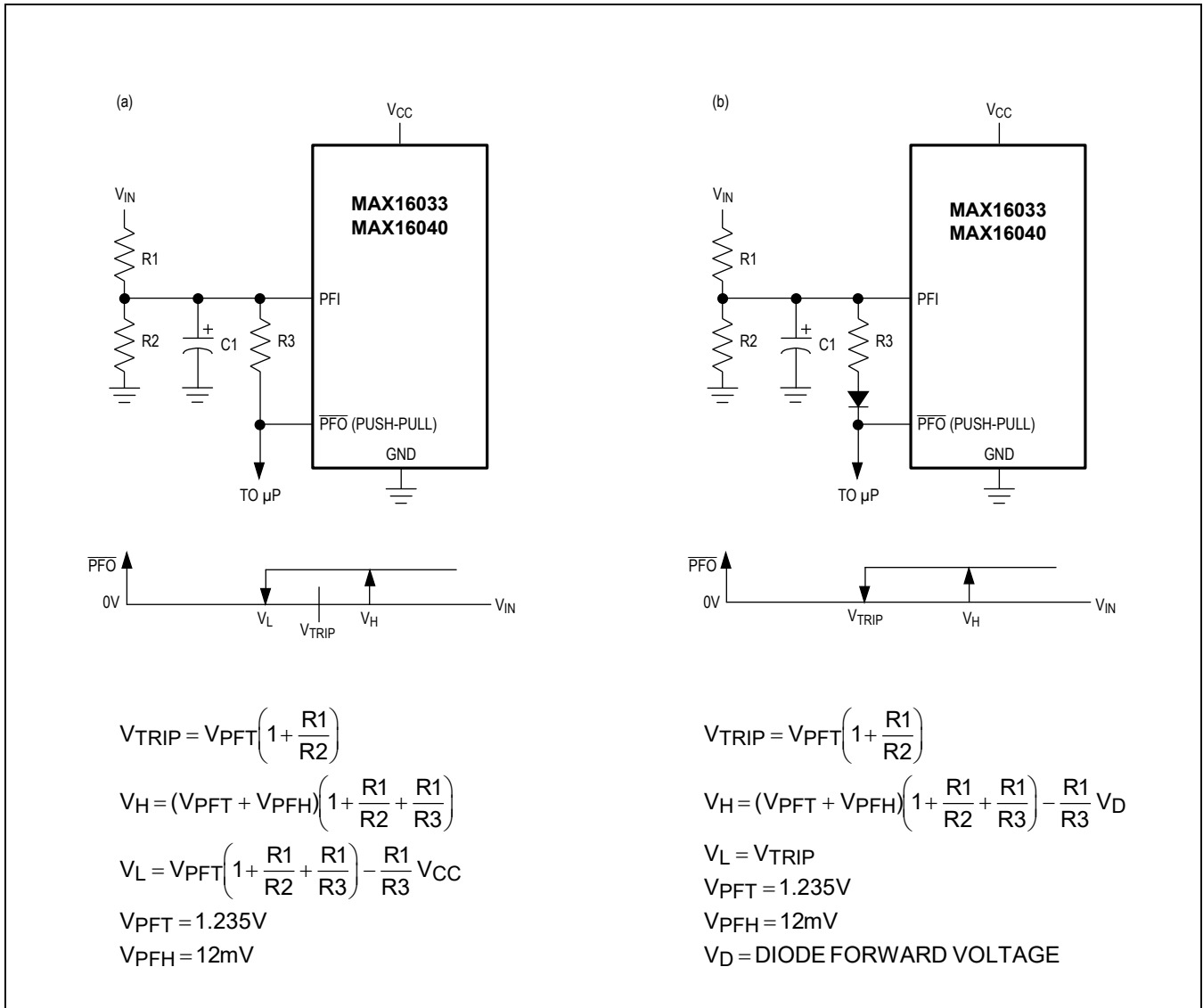


Figure 8. (a) Adding Additional Hysteresis to the Power-Fail Comparator. (b) Shifting the Additional Hysteresis above V_{TRIP}

Monitoring a Negative Voltage

Connect the circuit, as shown in Figure 9, to use the power-fail comparator to monitor a negative supply rail. $\overline{\text{PFO}}$ stays low when V^- is good. When V^- rises to cause PFI to be above +1.235V, $\overline{\text{PFO}}$ goes high. Ensure V_{CC} comes up before the negative supply.

Negative-Going V_{CC} Transients

The MAX16033–MAX16040 are relatively immune to short-duration, negative-going V_{CC} transients. Resetting the μP when V_{CC} experiences only small glitches is not usually desired.

The *Typical Operating Characteristics* section contains a Maximum Transient Duration vs. Reset Threshold Overdrive graph. The graph shows the maximum pulse width of a negative-going V_{CC} transient that would not trigger a reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold voltage), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 25 μs does not trigger a reset pulse.

A 0.1 μF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

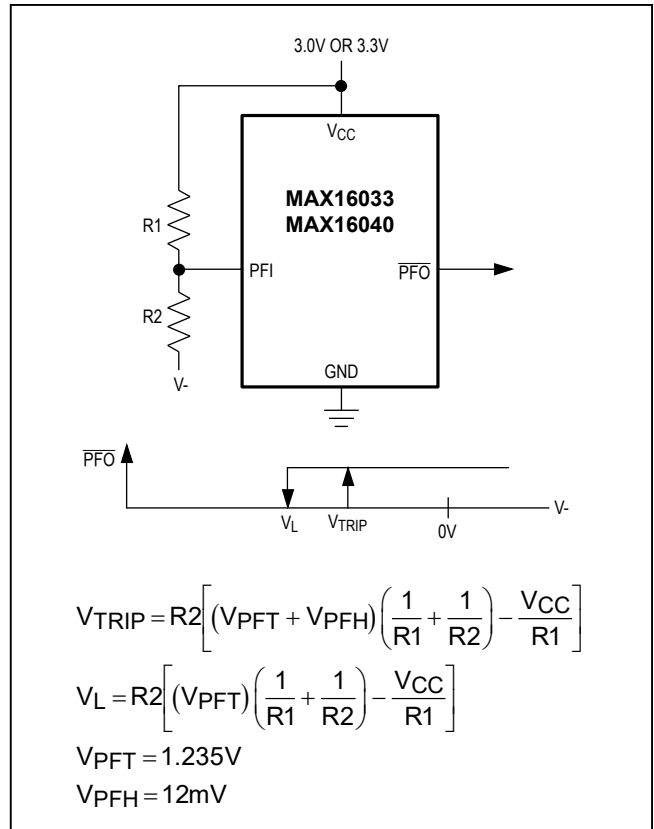


Figure 9. Monitoring a Negative Voltage

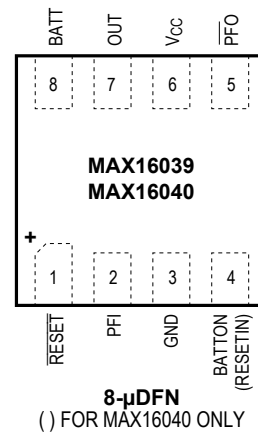
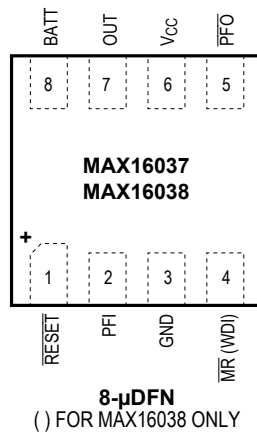
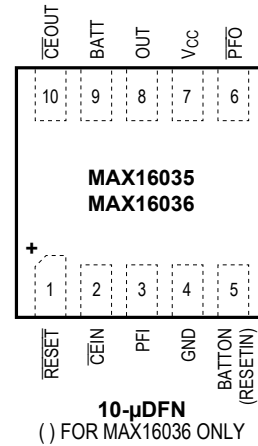
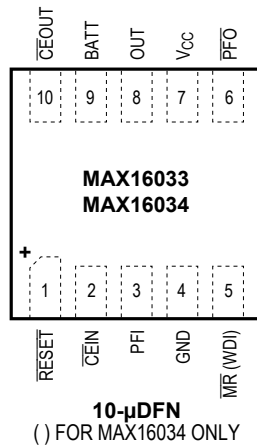
Device Marking Codes

PART	TOP MARK	PART	TOP MARK	PART	TOP MARK	PART	TOP MARK
MAX16033LLB23+T	+ABE	MAX16035LLB23+T	+ACC	MAX16037LLA23+T	+ABX	MAX16039LLA23+T	+ACV
MAX16033LLB26+T	+ABF	MAX16035LLB26+T	+ACD	MAX16037LLA26+T	+ABY	MAX16039LLA26+T	+ACW
MAX16033LLB29+T	+ABG	MAX16035LLB29+T	+ACE	MAX16037LLA29+T	+ABZ	MAX16039LLA29+T	+ACX
MAX16033LLB31+T	+ABH	MAX16035LLB31+T	+ACF	MAX16037LLA31+T	+ACA	MAX16039LLA31+T	+ACY
MAX16033LLB44+T	+ABI	MAX16035LLB44+T	+ACG	MAX16037LLA44+T	+ACB	MAX16039LLA44+T	+ACZ
MAX16033LLB46+T	+ABJ	MAX16035LLB46+T	+ACH	MAX16037LLA46+T	+ACC	MAX16039LLA46+T	+ADA
MAX16033PLB23+T	+ABK	MAX16035PLB23+T	+ACI	MAX16037PLA23+T	+ACD	MAX16039PLA23+T	+ADB
MAX16033PLB26+T	+ABL	MAX16035PLB26+T	+ACJ	MAX16037PLA26+T	+ACE	MAX16039PLA26+T	+ADC
MAX16033PLB29+T	+ABM	MAX16035PLB29+T	+ACK	MAX16037PLA29+T	+ACF	MAX16039PLA29+T	+ADD
MAX16033PLB31+T	+ABN	MAX16035PLB31+T	+ACL	MAX16037PLA31+T	+ACG	MAX16039PLA31+T	+ADE
MAX16033PLB44+T	+ABO	MAX16035PLB44+T	+ACM	MAX16037PLA44+T	+ACH	MAX16039PLA44+T	+ADF
MAX16033PLB46+T	+ABP	MAX16035PLB46+T	+ACN	MAX16037PLA46+T	+ACI	MAX16039PLA46+T	+ADG
MAX16034LLB23+T	+ABQ	MAX16036LLB23+T	+ACO	MAX16038LLA23+T	+ACJ	MAX16040LLA23+T	+ADH
MAX16034LLB26+T	+ABR	MAX16036LLB26+T	+ACP	MAX16038LLA26+T	+ACK	MAX16040LLA26+T	+ADI
MAX16034LLB29+T	+ABS	MAX16036LLB29+T	+ACQ	MAX16038LLA29+T	+ACL	MAX16040LLA29+T	+ADJ
MAX16034LLB31+T	+ABT	MAX16036LLB31+T	+ACR	MAX16038LLA31+T	+ACM	MAX16040LLA31+T	+ADK
MAX16034LLB44+T	+ABU	MAX16036LLB44+T	+ACS	MAX16038LLA44+T	+ACN	MAX16040LLA44+T	+ADL
MAX16034LLB46+T	+ABV	MAX16036LLB46+T	+ACT	MAX16038LLA46+T	+ACO	MAX16040LLA46+T	+ADM
MAX16034PLB23+T	+ABW	MAX16036PLB23+T	+ACU	MAX16038PLA23+T	+ACP	MAX16040PLA23+T	+ADN
MAX16034PLB26+T	+ABX	MAX16036PLB26+T	+ACV	MAX16038PLA26+T	+ACQ	MAX16040PLA26+T	+ADO
MAX16034PLB29+T	+ABY	MAX16036PLB29+T	+ACW	MAX16038PLA29+T	+ACR	MAX16040PLA29+T	+ADP
MAX16034PLB31+T	ABZ	MAX16036PLB31+T	+ACX	MAX16038PLA31+T	+ACS	MAX16040PAL31+T	+ADQ
MAX16034PLB44+T	+ACA	MAX16036PLB44+T	+ACY	MAX16038PLA44+T	+ACT	MAX16040PLA44+T	+ADR
MAX16034PLB46+T	+ACB	MAX16036PLB46+T	+ACZ	MAX16038PLA46+T	+ACU	MAX16040PLA46+T	+ADS

Note: 48 standard versions shown in **bold** are available. Sample stock is generally held on standard versions only. Contact factory for nonstandard versions availability.

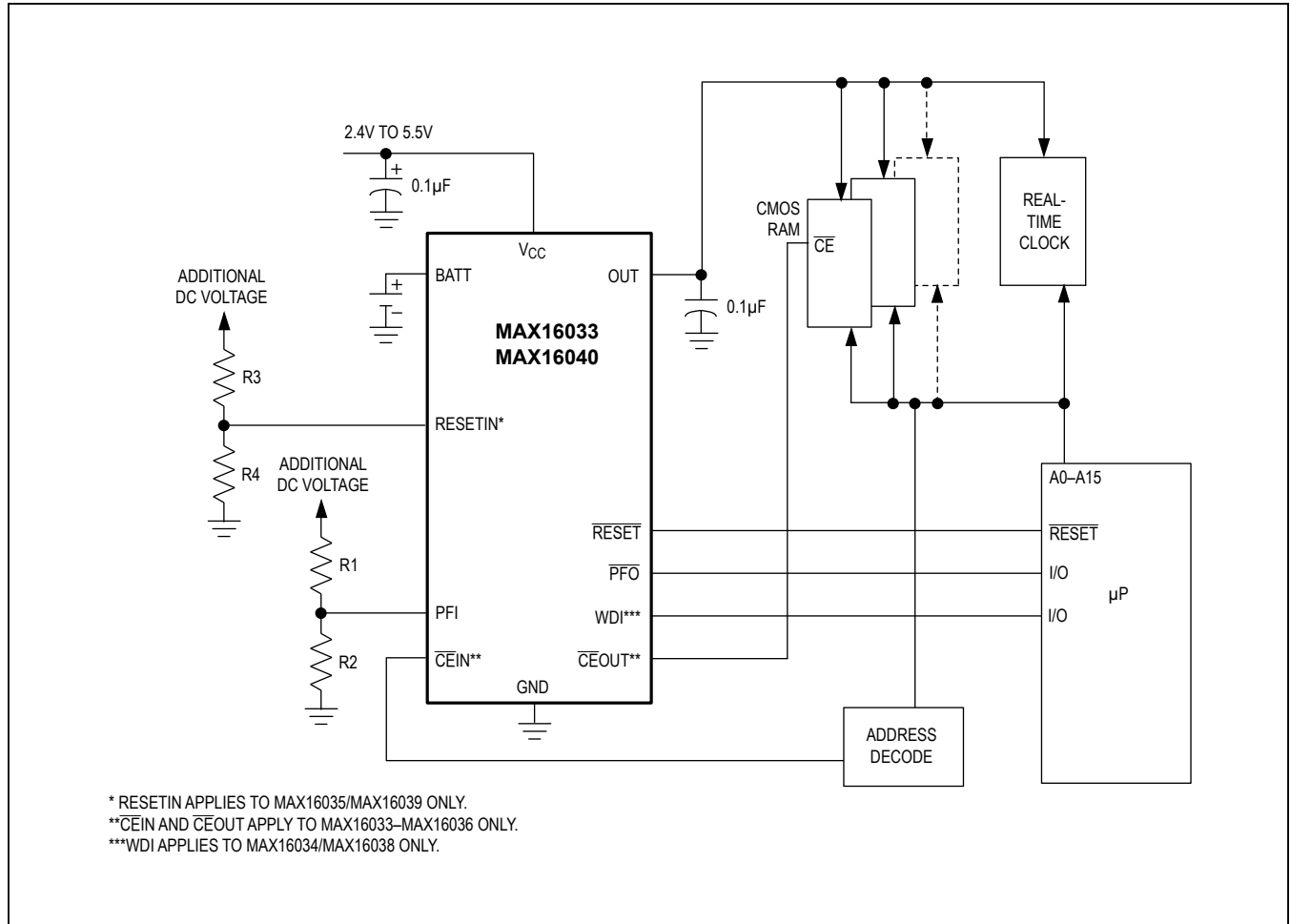
Pin Configurations

TOP VIEW



+ DENOTES A LEAD(Pb)-FREE PACKAGE.

Typical Operating Circuit



Ordering Information (continued)

PART*	TEMP RANGE	PIN-PACKAGE
MAX16035 LLB__+T	-40°C to +85°C	10 μ DFN
MAX16035PLB__+T	-40°C to +85°C	10 μ DFN
MAX16036 LLB__+T	-40°C to +85°C	10 μ DFN
MAX16036PLB__+T	-40°C to +85°C	10 μ DFN
MAX16037 LLA__+T	-40°C to +85°C	8 μ DFN
MAX16037PLA__+T	-40°C to +85°C	8 μ DFN
MAX16038 LLA__+T	-40°C to +85°C	8 μ DFN
MAX16038PLA__+T	-40°C to +85°C	8 μ DFN
MAX16039 LLA__+T	-40°C to +125°C	8 μ DFN
MAX16039PLA__+T	-40°C to +85°C	8 μ DFN
MAX16039PLA31+T	-55°C to +85°C	8 μ DFN
MAX16040 LLA__+T	-40°C to +85°C	8 μ DFN
MAX16040PLA__+T	-40°C to +85°C	8 μ DFN

*These parts offer a choice of reset threshold voltages. From the Reset Threshold Ranges table, insert the desired threshold voltage code in the blank to complete the part number. See the Selector Guide for a listing of device features.

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Reset Threshold Ranges

SUFFIX	RESET-THRESHOLD VOLTAGE (V)		
	MIN	TYP	MAX
46	4.50	4.63	4.75
44	4.25	4.38	4.50
31	3.00	3.08	3.15
29	2.85	2.93	3.00
26	2.55	2.63	2.70
23	2.25	2.32	2.38

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 μ DFN	L822+1	21-0164	90-0005
10 μ DFN	L1022+1	21-0164	90-0006

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	5/14	Data sheet rebranded; updated <i>Electrical Characteristics</i> and <i>Ordering Information</i> tables to support MAX16039PLA31+T option at -55°C	2, 19
2	5/19	Updated <i>Electrical Characteristics</i> and <i>Ordering Information</i>	2, 19

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the *Electrical Characteristics* table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.