


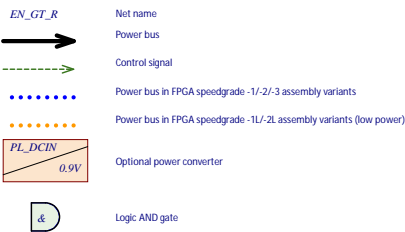
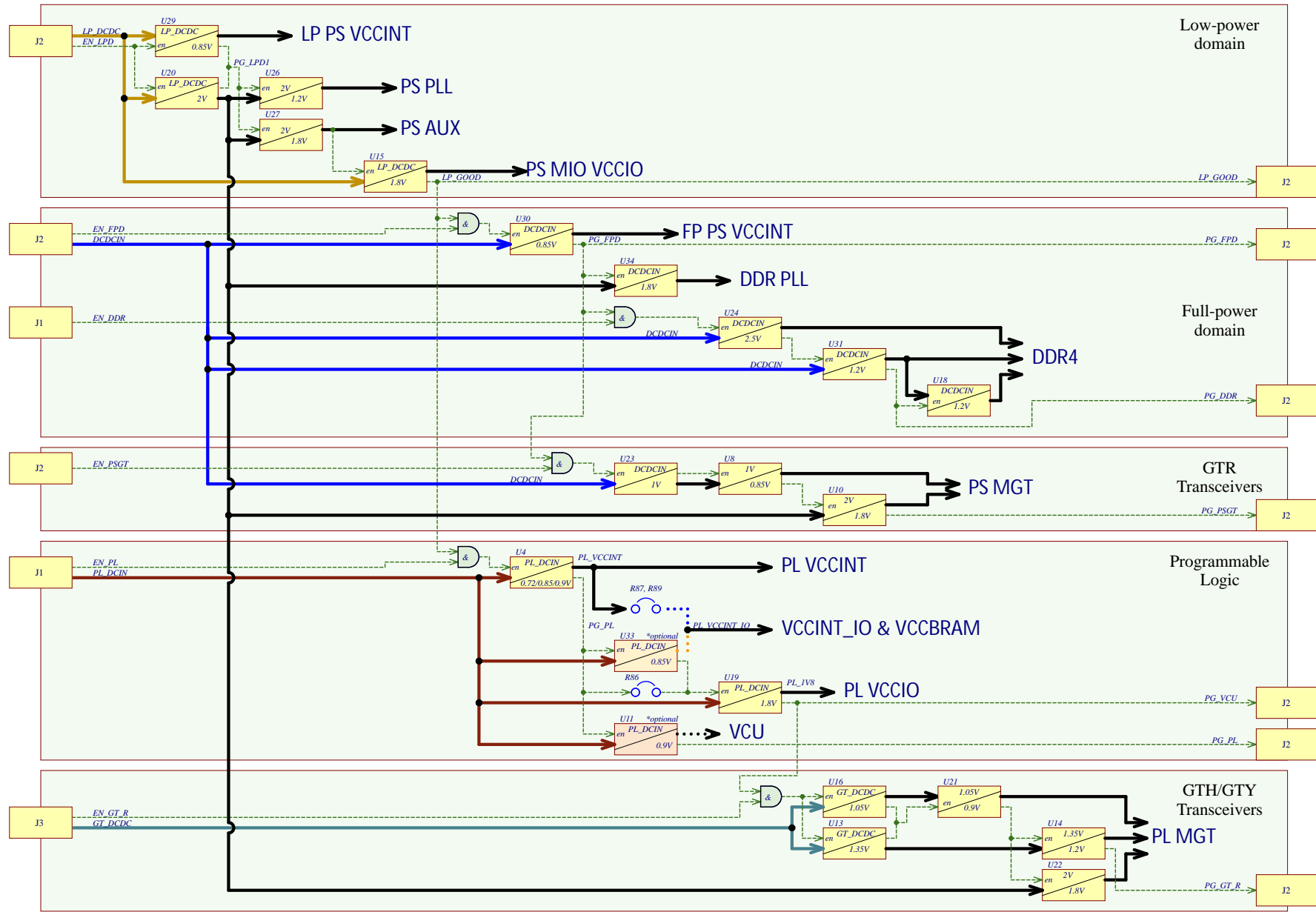
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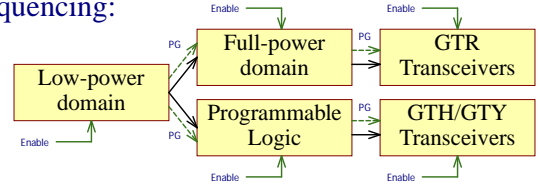
Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0803</b>		
	A4	Number: <b>TE0803 4DE21-L</b>	Rev. <b>04</b>
	Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>30</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		





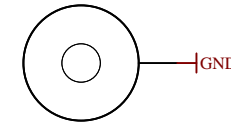
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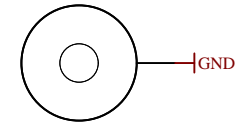
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A3	Number: TE0803 4DE21-L	Rev. 04
Datum: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 3 of 30
Filename: Power_Diagram.SchDoc		

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_LN Legal Notices Modules.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_1 POWER_1.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_OVERVIEW TE0803-Overview.SchDoc
U_PD Power_Diagram.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

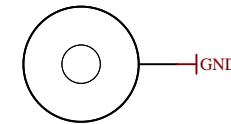
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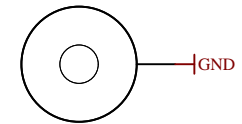
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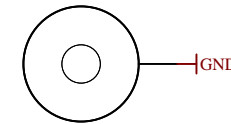
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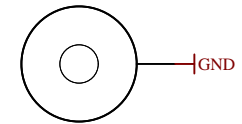
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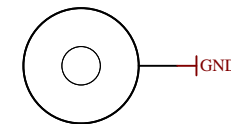
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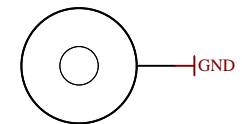
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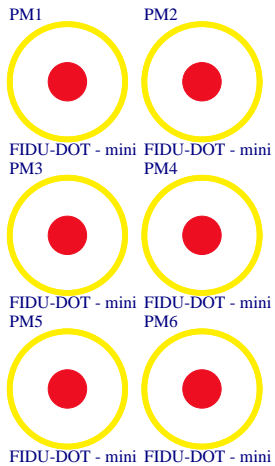
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial  
Serial  
Serialnumber 6,3 x 6.3mm

Assembly variant 4DE21-L

Created by

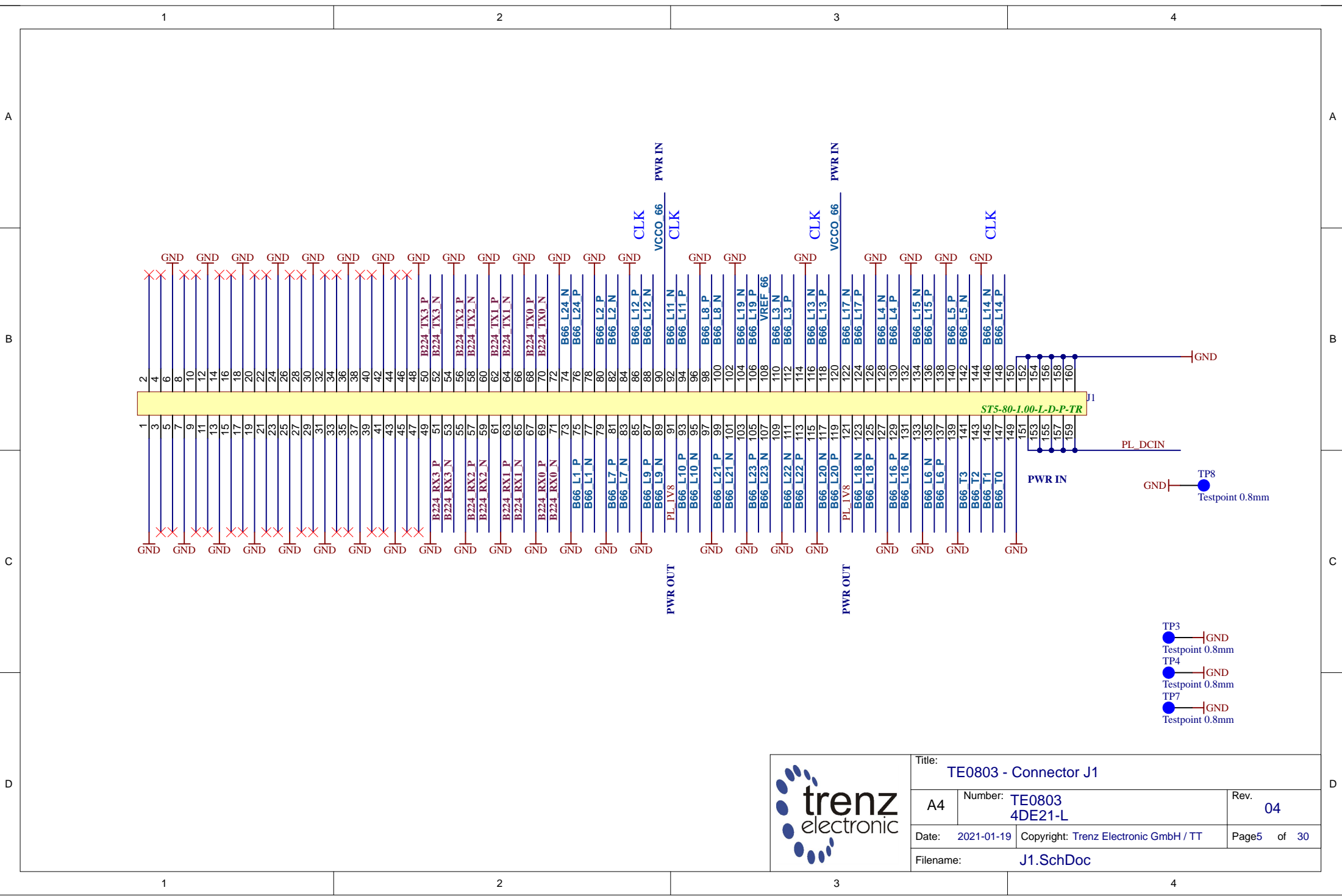
Modified by

Modified at

SVN Revision 11196



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A4	Number: TE0803 4DE21-L	Rev. 04
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Title: TE0803 - Connector J1		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page5 of 30
Filename: J1.SchDoc		

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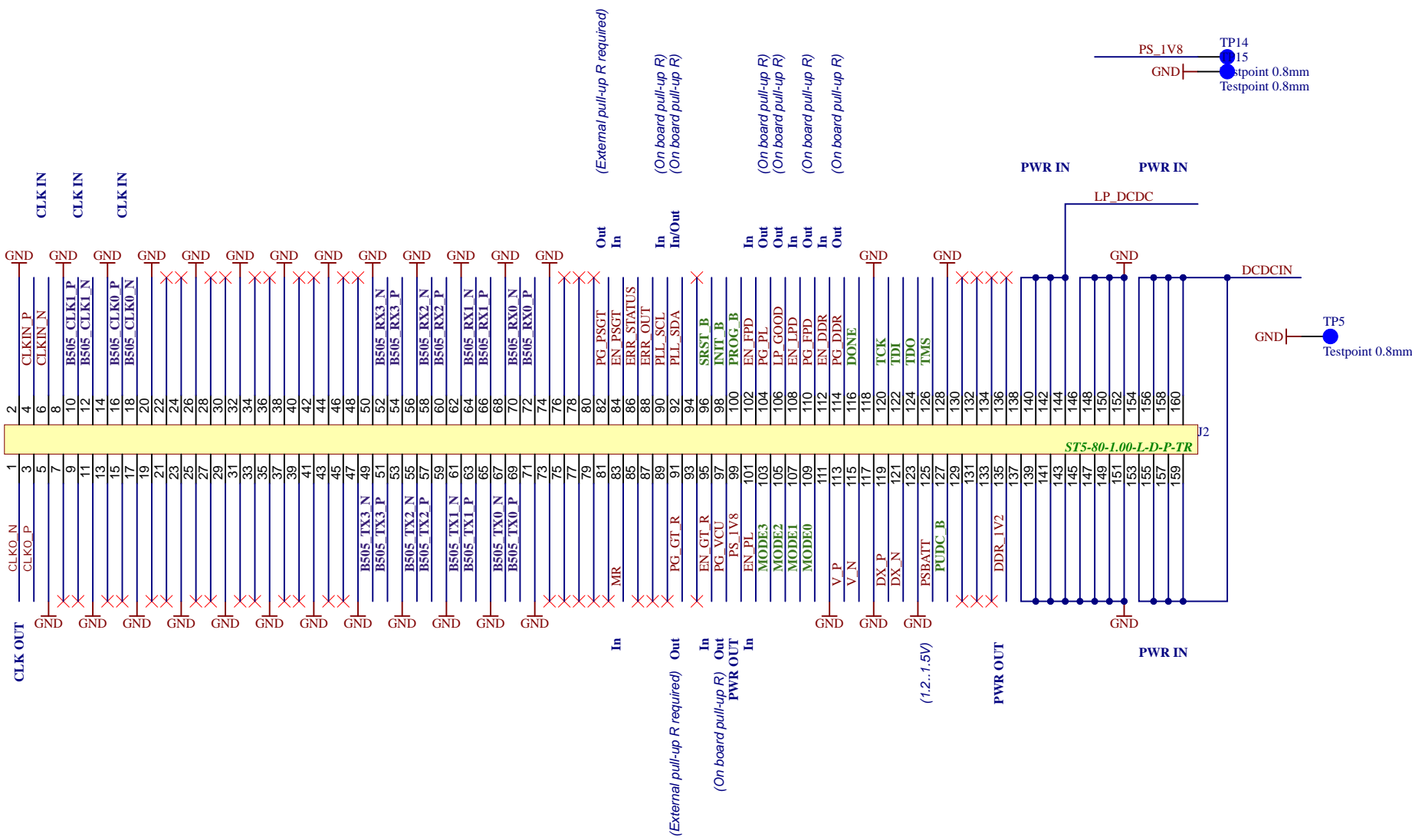
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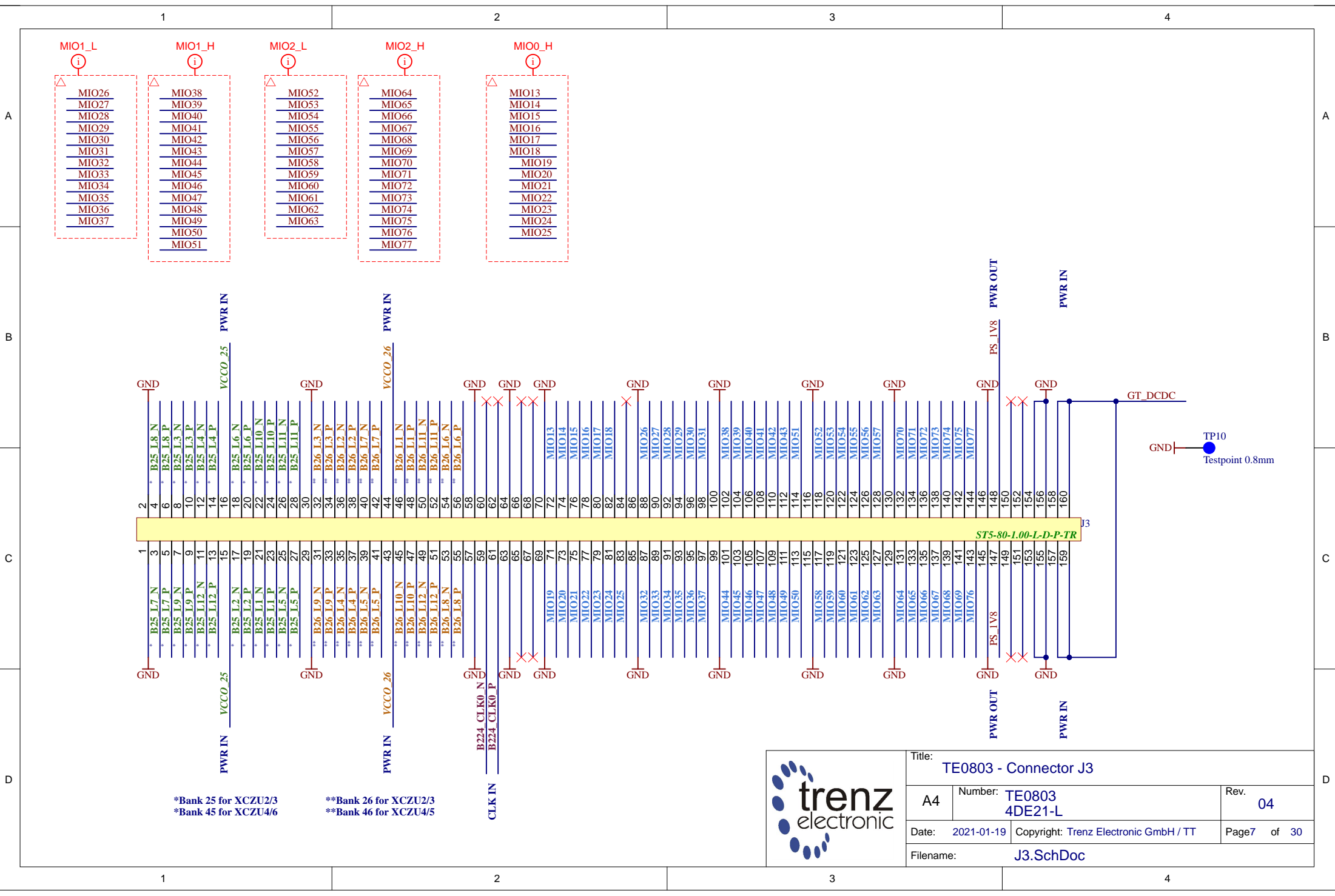
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A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 6 of 30
Filename: J2.SchDoc		

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\*Bank 25 for XCZU2/3  
 \*Bank 45 for XCZU4/6

\*\*Bank 26 for XCZU2/3  
 \*\*Bank 46 for XCZU4/5



Title: TE0803 - Connector J3		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 7 of 30
Filename: J3.SchDoc		

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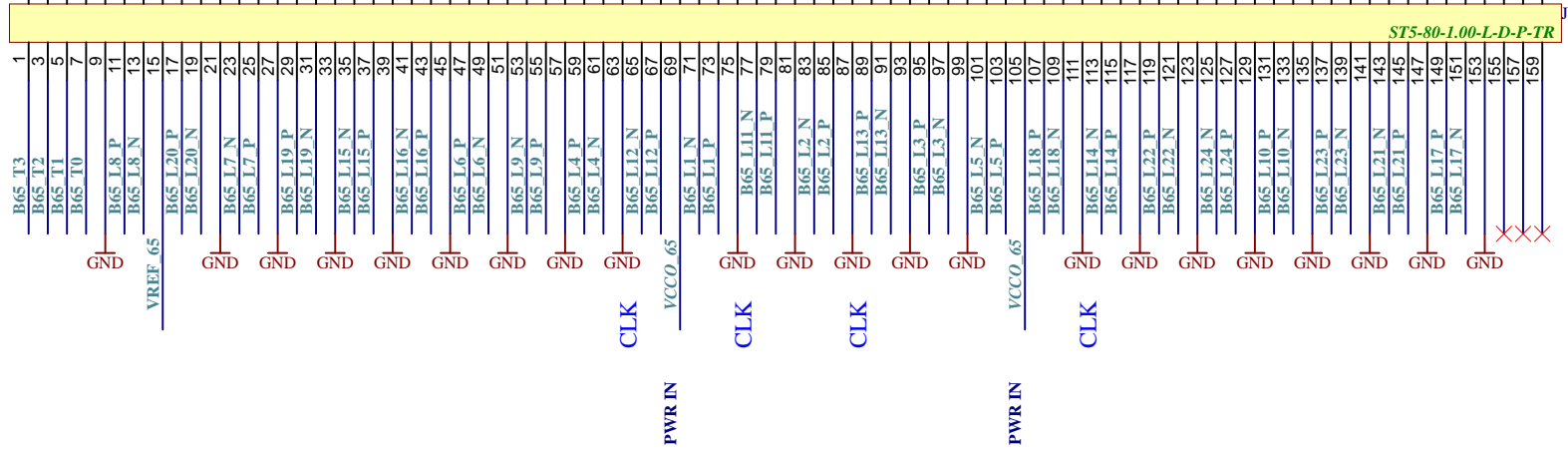
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J4 ST5-80-1.00-L-D-P-TR



Title: TE0803 - Connector J4		
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page8 of 30
Filename: J4.SchDoc		

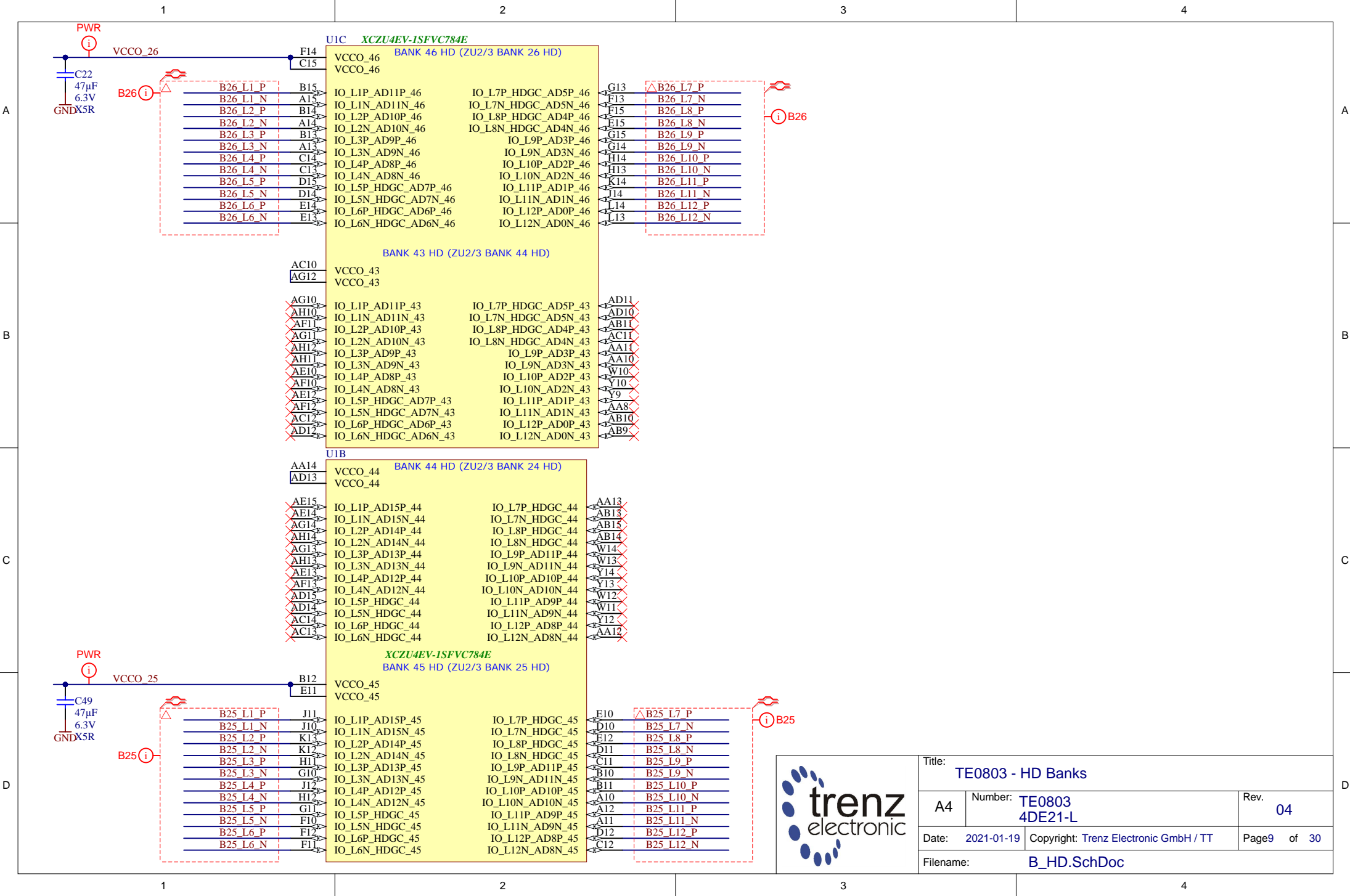
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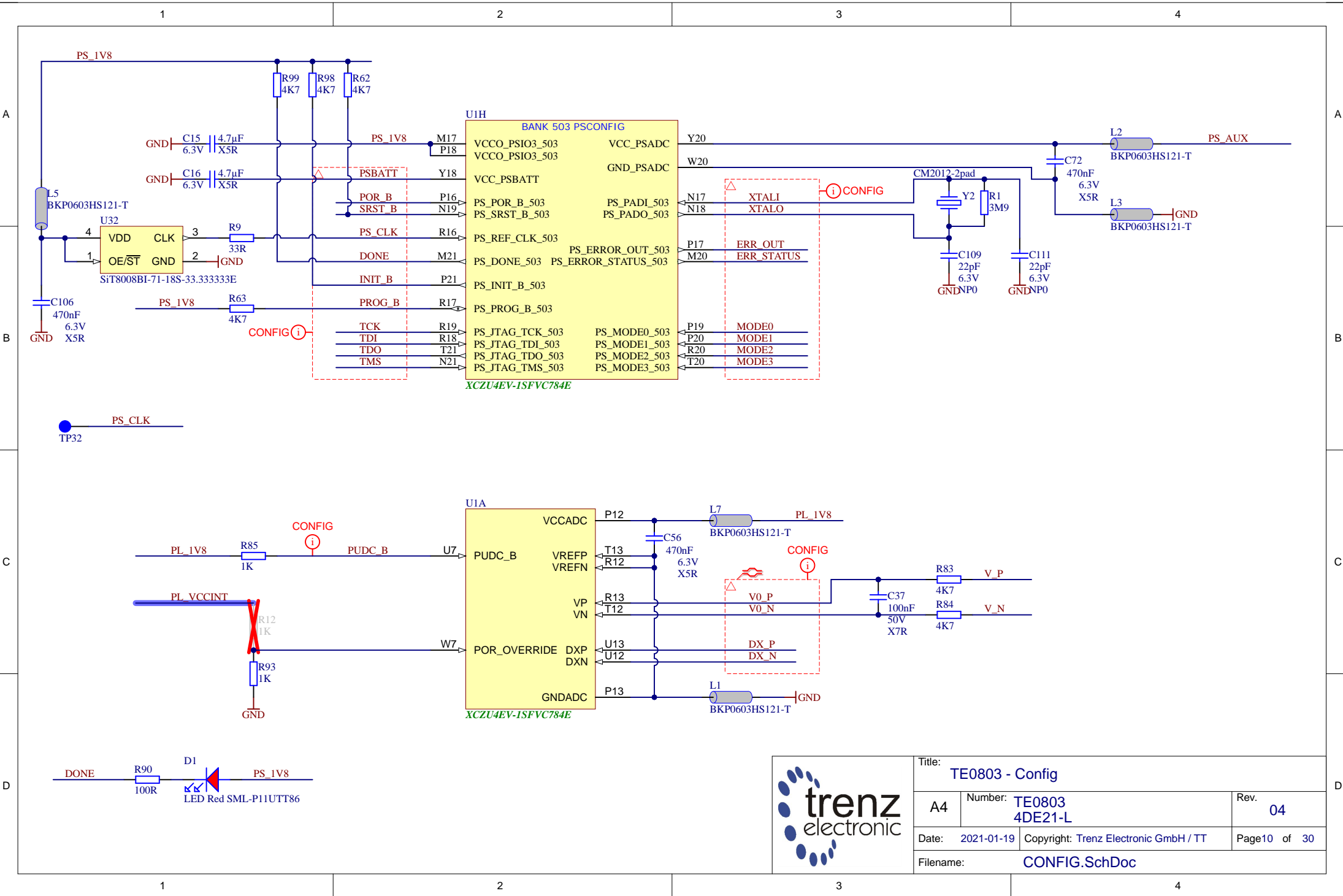
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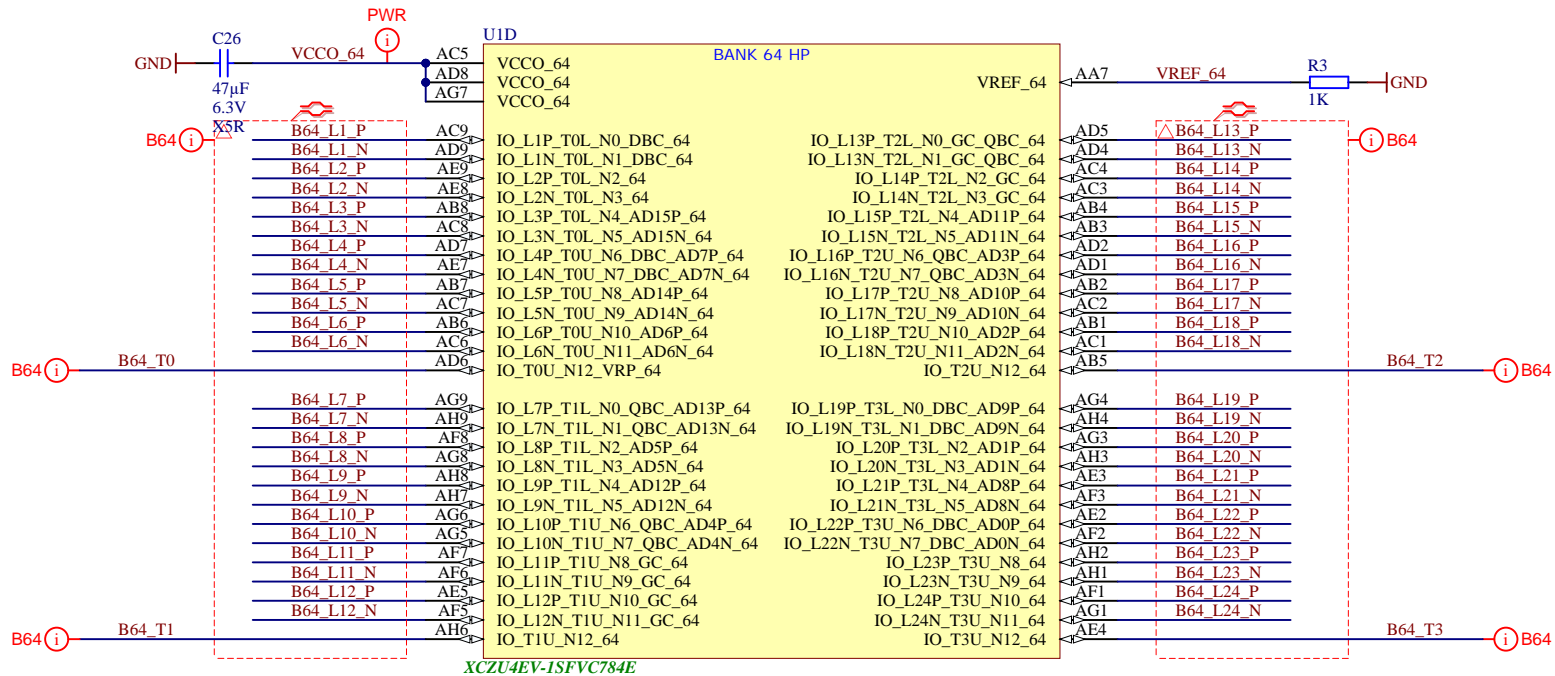




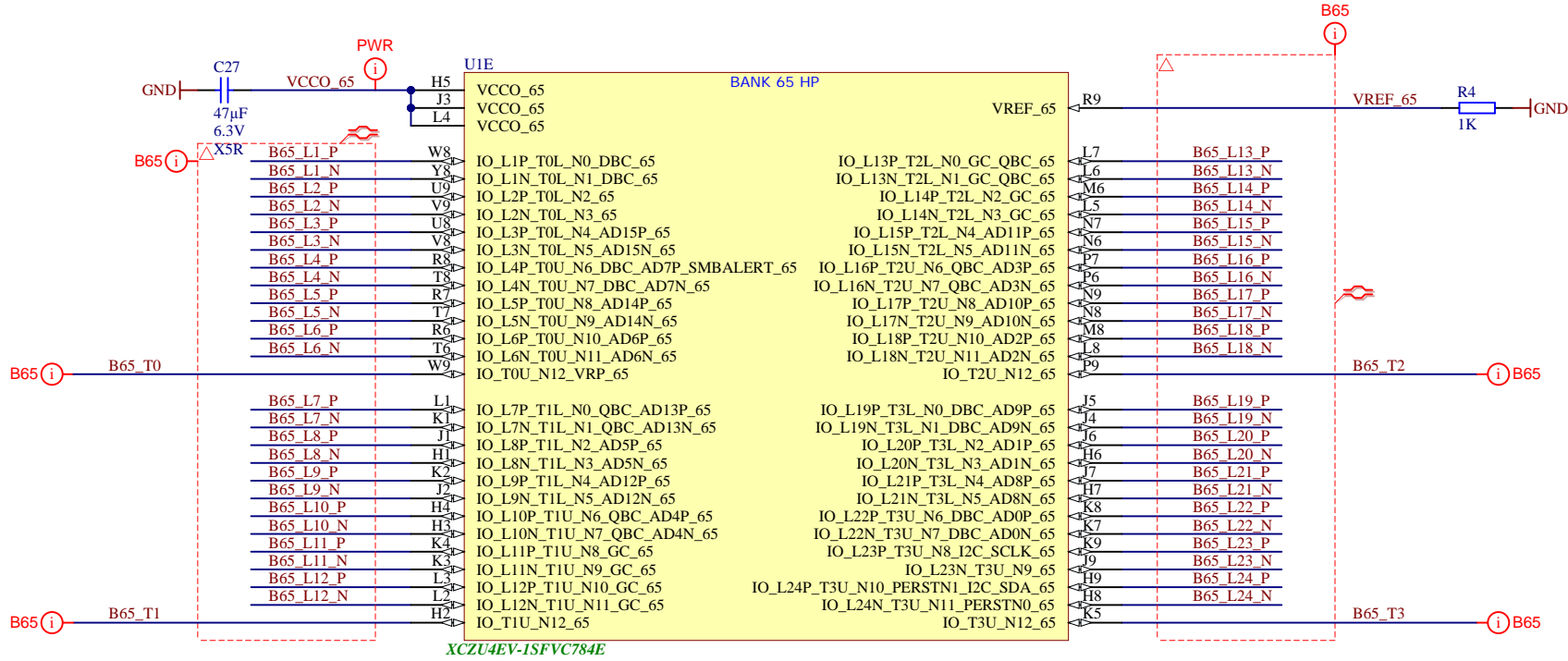
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page9 of 30
Filename: B_HD.SchDoc		



Title: TE0803 - Config		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 10 of 30
Filename: CONFIG.SchDoc		

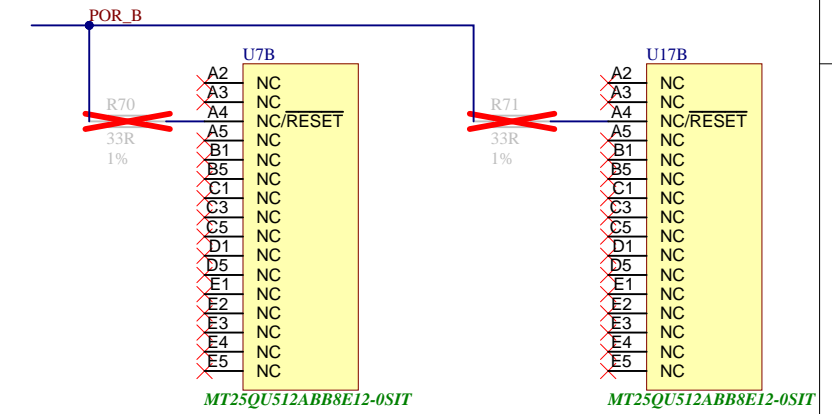
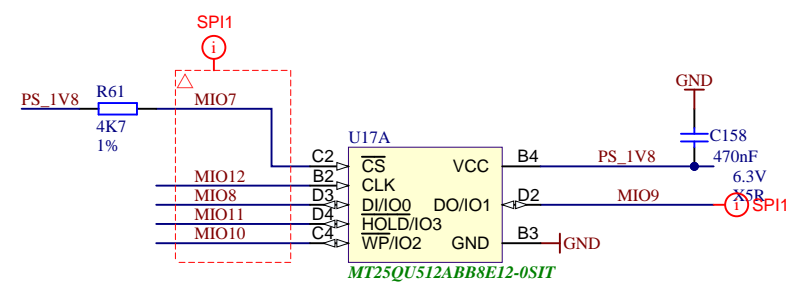
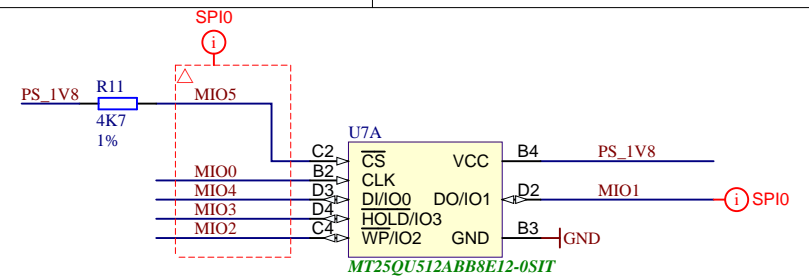
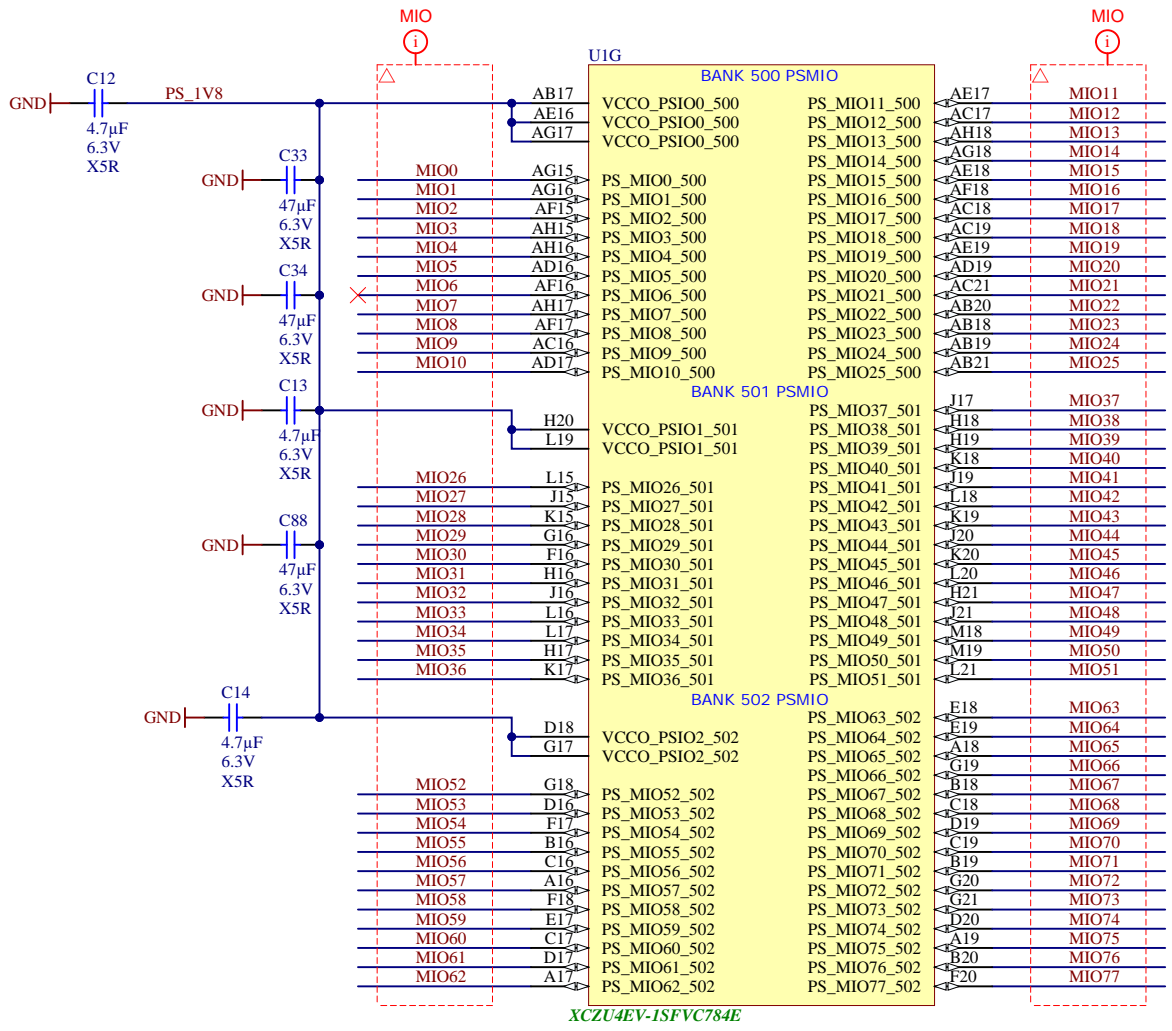


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Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>30</b>
Filename: <b>B64.SchDoc</b>		



Title: <b>TE0803 - B65</b>		
A4	Number: <b>TE0803 4DE21-L</b>	Rev. <b>04</b>
Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>12</b> of <b>30</b>
Filename: <b>B65.SchDoc</b>		





	Title: <b>TE0803 - MIO Banks</b>		
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	Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>14</b> of <b>30</b>
	Filename: <b>B_MIO.SchDoc</b>		

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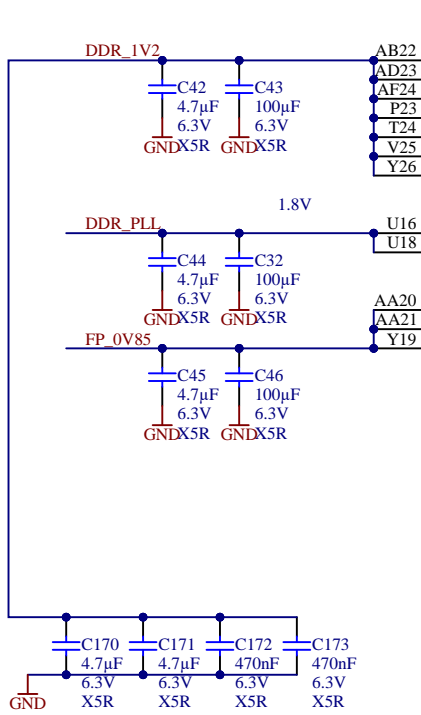
D

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U11		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504		W27	DDR4-CS
PS_DDR_CS_N1_504		V26	
PS_DDR_BA0_504		V23	DDR4-BA0
PS_DDR_BA1_504		W22	DDR4-BA1
PS_DDR_BG0_504		W24	DDR4-BG0
PS_DDR_BG1_504		V22	DDR4-BG1
PS_DDR_PARITY_504		V24	DDR4-PAR
PS_DDR_RAM_RST_N_504		U23	DDR4-RESET
PS_DDR_ACT_N_504		Y23	DDR4-ACT
PS_DDR_ALERT_N_504		U25	DDR4-ALERT
PS_DDR_ZQ_504		U24	
PS_DDR_ODT0_504		U28	DDR4-ODT0
PS_DDR_ODT1_504		U26	

*XCZU4EV-1SFVC784E*

U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
		PS_DDR_DQ64_504	PS_DDR_DQ64_504
		PS_DDR_DQ65_504	PS_DDR_DQ65_504
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ66_504
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ67_504
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ68_504
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ69_504
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ70_504
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ71_504
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	
DDR4-DQS3_N	AF27	PS_DDR_DQS_N3_504	
DDR4-DQS4_P	N23	PS_DDR_DQS_P4_504	
DDR4-DQS4_N	M23	PS_DDR_DQS_N4_504	
DDR4-DQS5_P	L23	PS_DDR_DQS_P5_504	
DDR4-DQS5_N	K23	PS_DDR_DQS_N5_504	
DDR4-DQS6_P	N26	PS_DDR_DQS_P6_504	
DDR4-DQS6_N	N27	PS_DDR_DQS_N6_504	
DDR4-DQS7_P	J26	PS_DDR_DQS_P7_504	
DDR4-DQS7_N	J27	PS_DDR_DQS_N7_504	
	R27	PS_DDR_DQS_P8_504	
	T27	PS_DDR_DQS_N8_504	
		PS_DDR_DM0_504	AG20
		PS_DDR_DM1_504	AE23
		PS_DDR_DM2_504	AE25
		PS_DDR_DM3_504	AE28
		PS_DDR_DM4_504	R23
		PS_DDR_DM5_504	H23
		PS_DDR_DM6_504	L27
		PS_DDR_DM7_504	H26
		PS_DDR_DM8_504	T26

*XCZU4EV-1SFVC784E*



Title: <b>TE0803 - PS_DDR</b>		
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Filename: <b>PS_DDR.SchDoc</b>		

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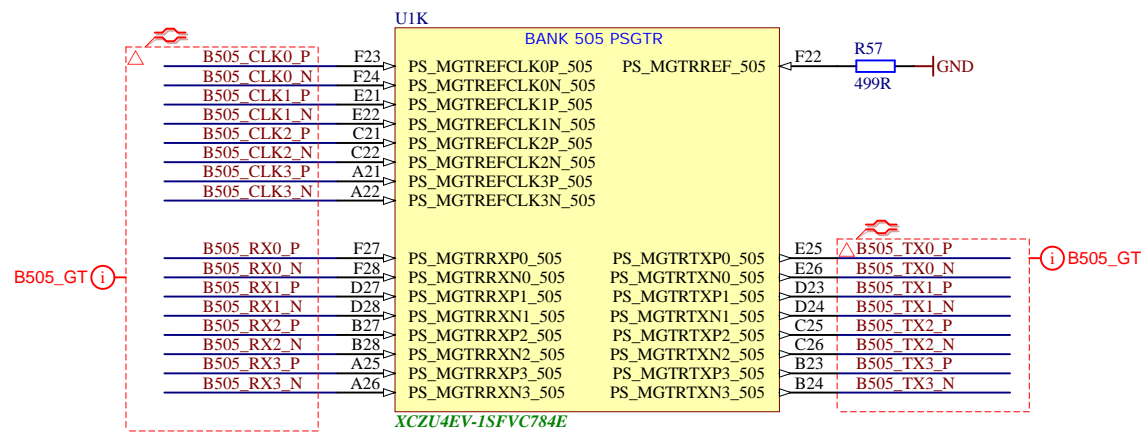
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			Title: TE0803 - PS_GT	
			A4	Number: TE0803 4DE21-L
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT		Page 16 of 30
Filename: B_PS_GT.SchDoc				

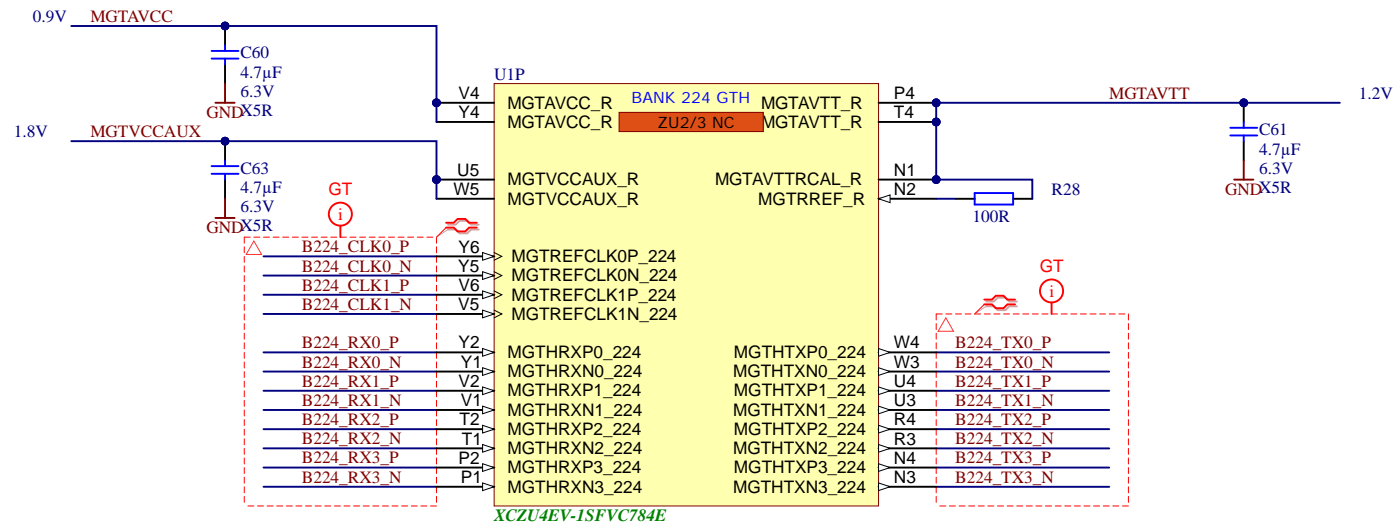
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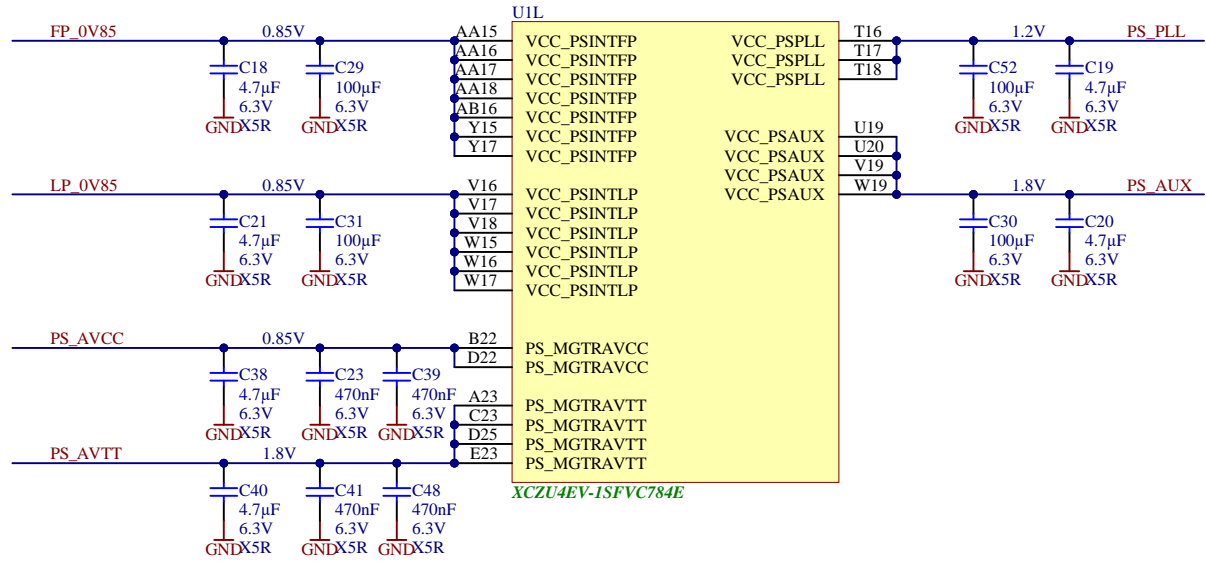
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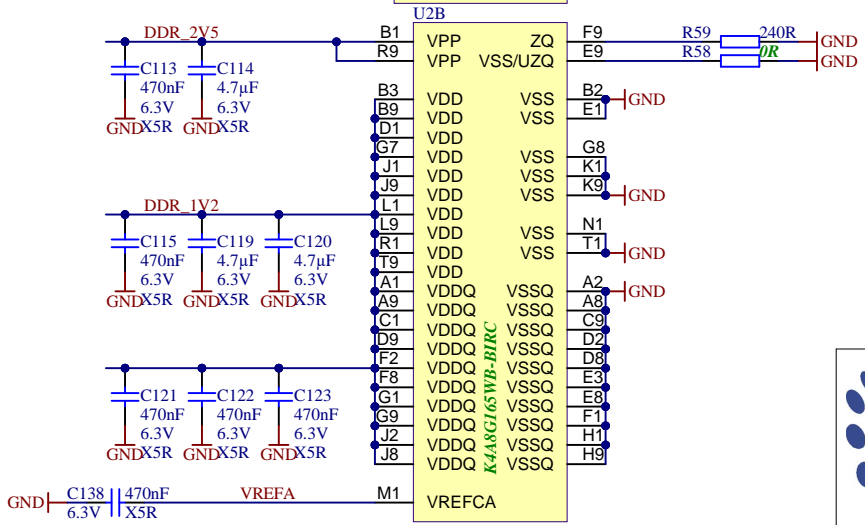
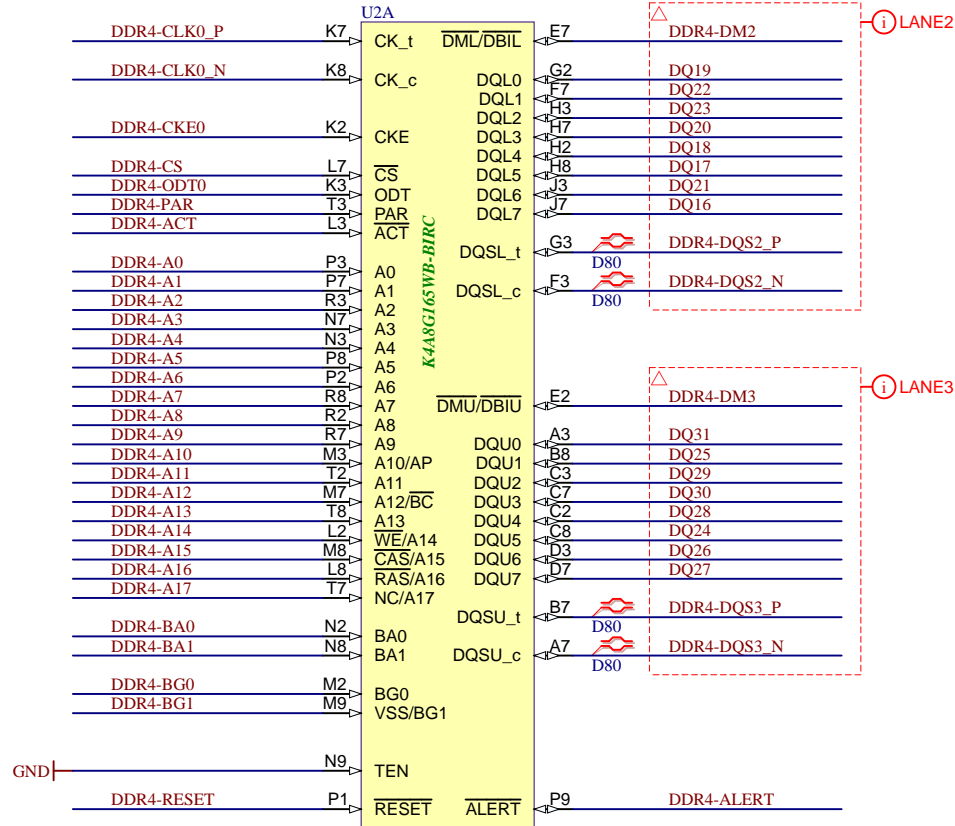


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	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 17 of 30
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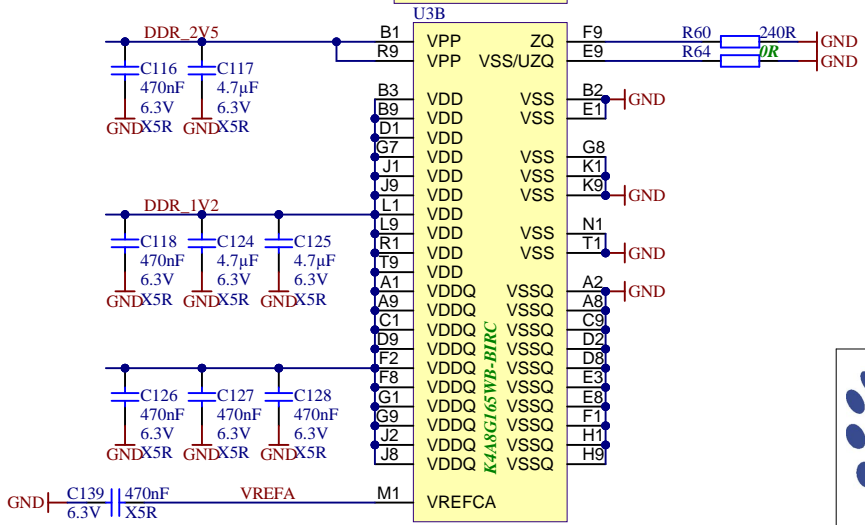
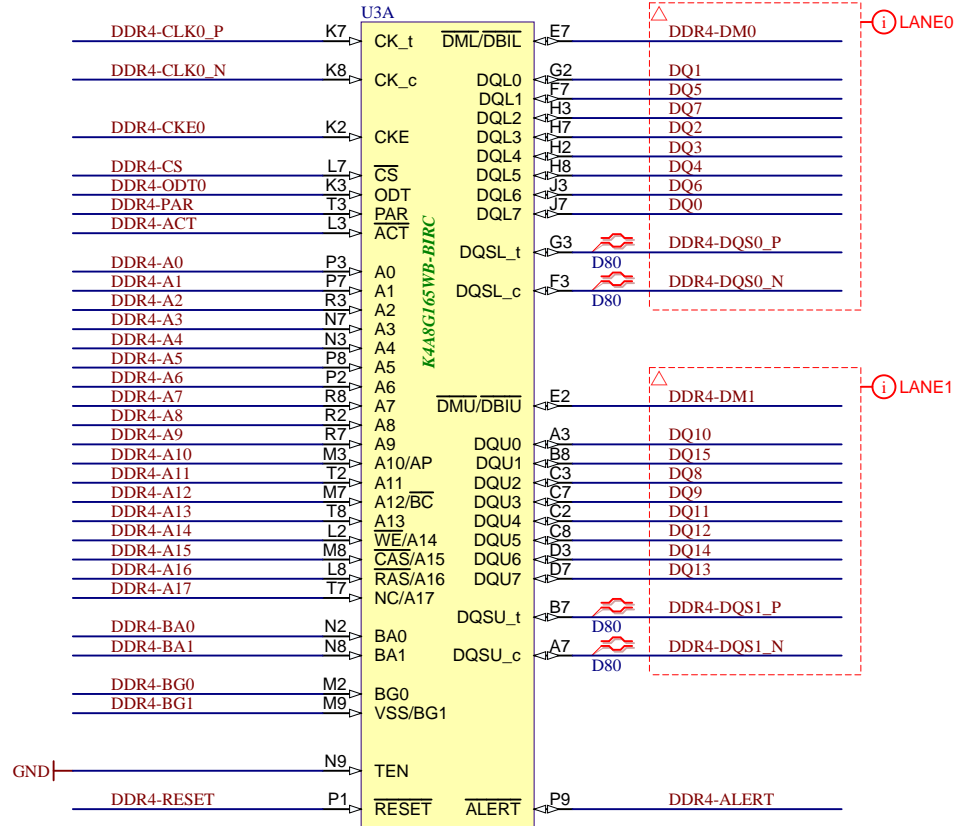


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	A4	Number: TE0803 4DE21-L	Rev. 04
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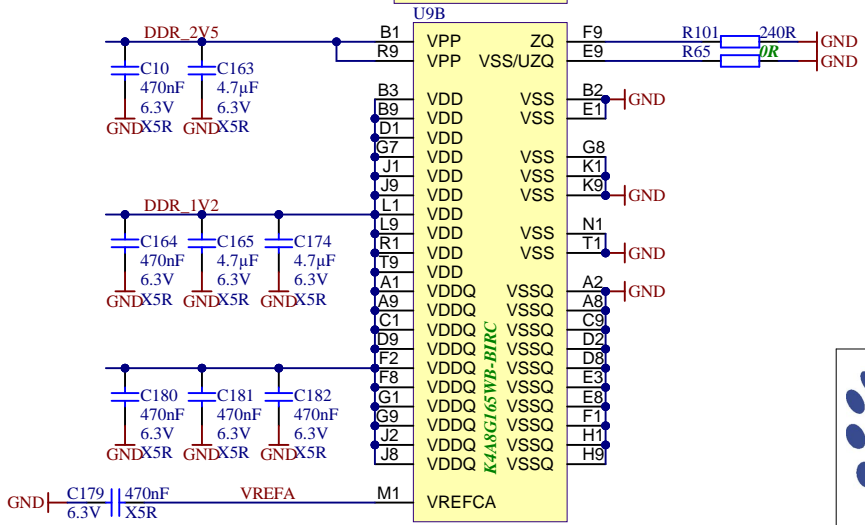
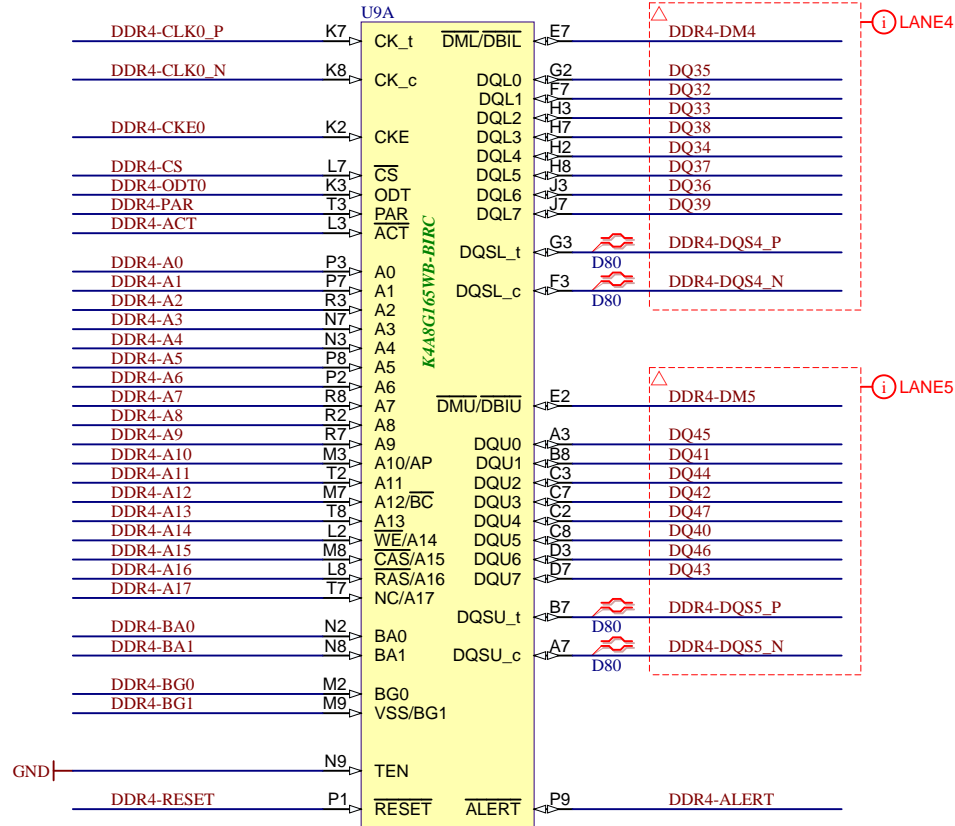




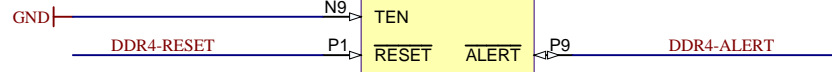
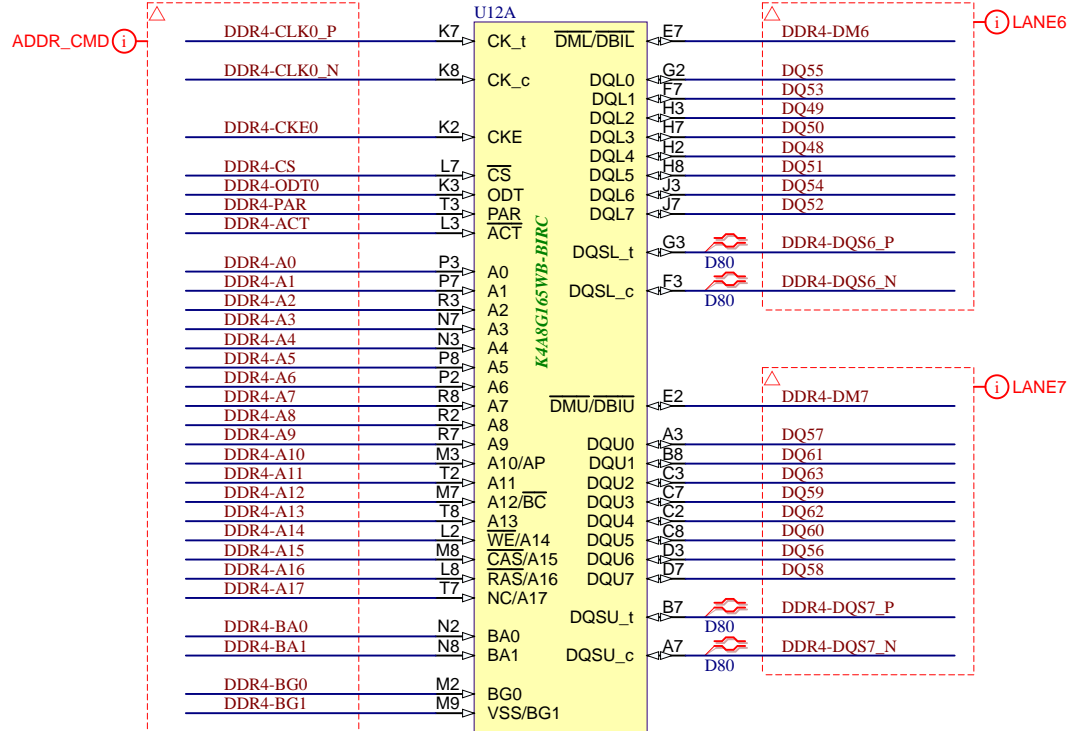
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Filename: DDR4-RAM.SchDoc		



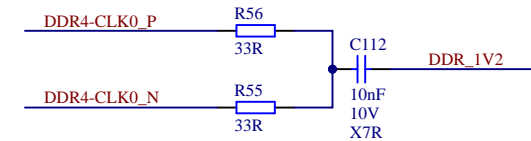
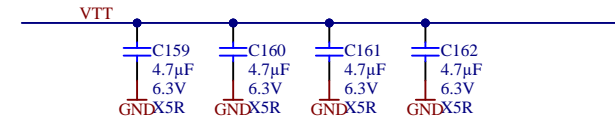
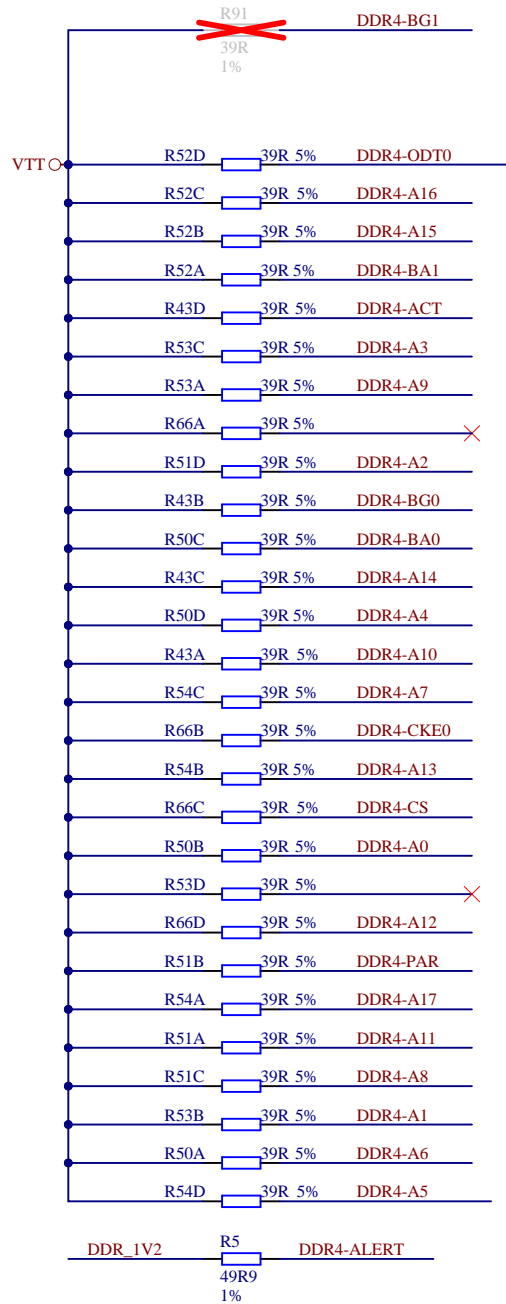
Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page21 of 30
Filename: DDR4-RAM_2.SchDoc		



Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page22 of 30
Filename: DDR4-RAM_3.SchDoc		

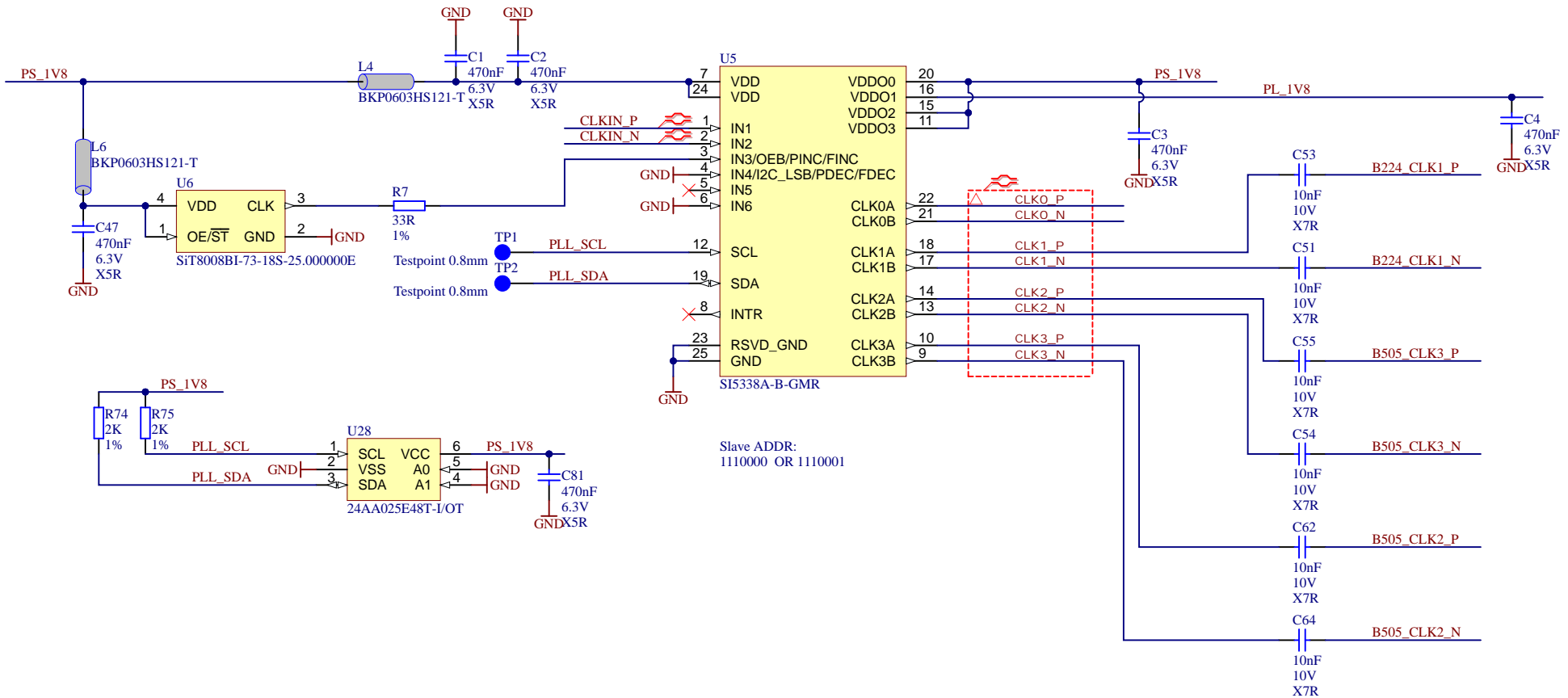


Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 23 of 30
Filename: DDR4-RAM_4.SchDoc		




Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page24 of 30
Filename: DDR4-TERM.SchDoc		

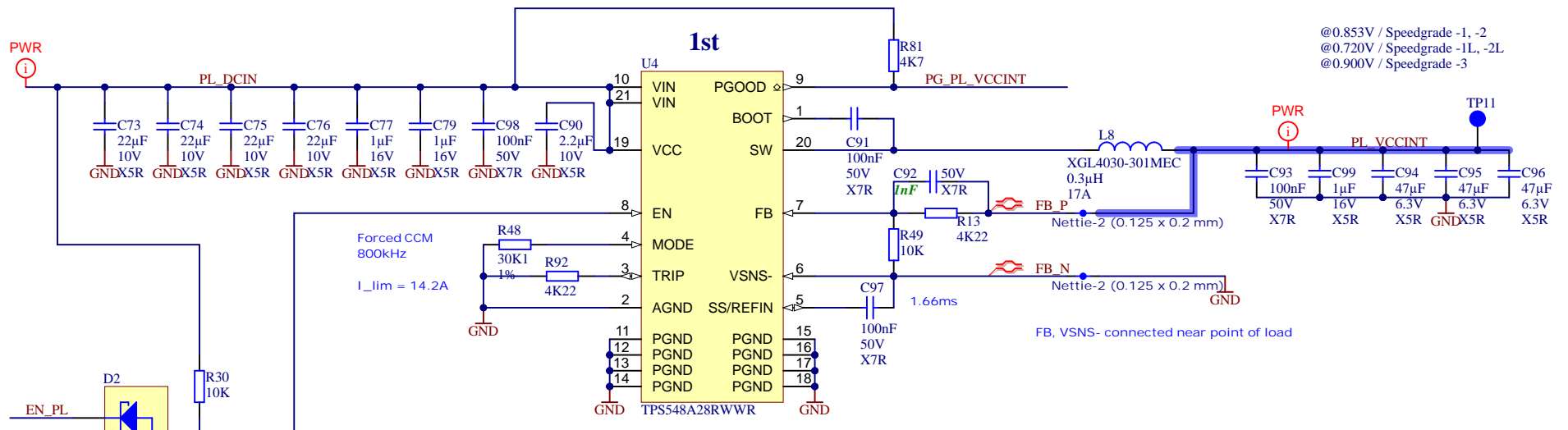




Slave ADDR:  
1110000 OR 1110001

			Title: TE0803 - CLOCK	
			A4	Number: TE0803 4DE21-L
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT		Page 25 of 30
Filename: Clock.SchDoc				

# PL VCCINT



@0.853V / Speedgrade -1, -2  
 @0.720V / Speedgrade -1L, -2L  
 @0.900V / Speedgrade -3

Forced CCM  
 800kHz  
 I\_lim = 14.2A

FB, VSNS- connected near point of load

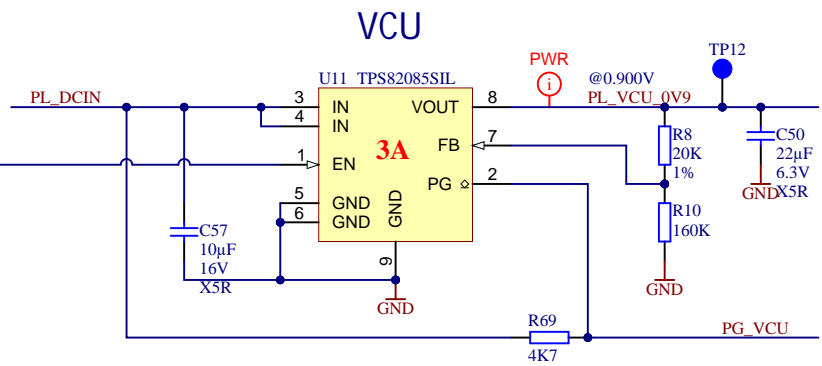
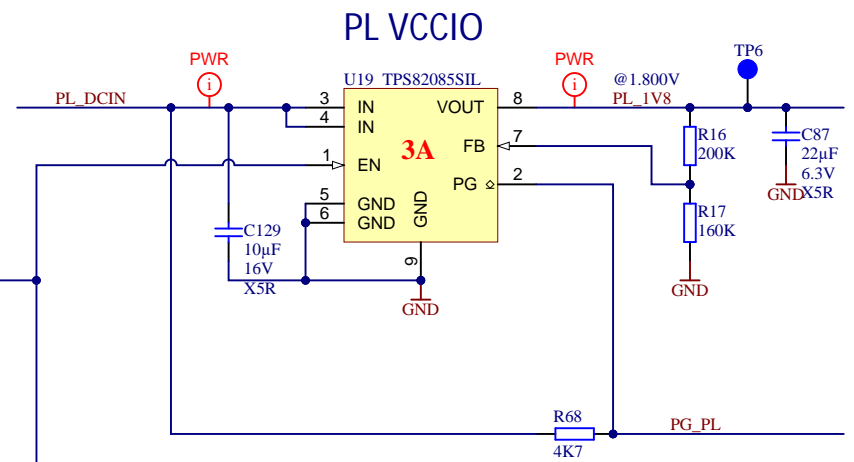
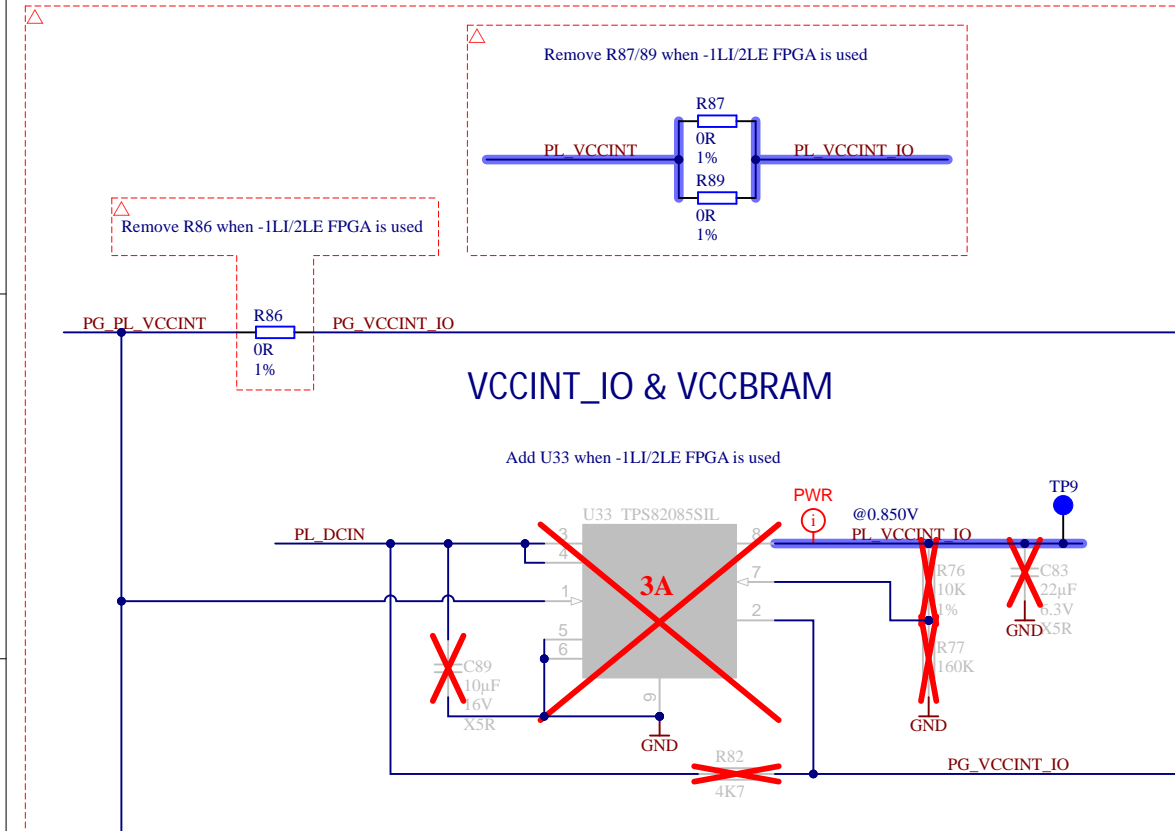
FPGA Speed grade:


-1L1 / -2LE	R13 - 2K, R49 - 10K	PL_VCCINT = 0.720V
-1 / -2	R13 - 4K22, R49 - 10K	PL_VCCINT = 0.853V
-3E	R13 - 10K, R49 - 20K	PL_VCCINT = 0.900V

U4 pin compatible with  
 -- TPS548B28 (20A)  
 -- TPS54JA20 (12A)



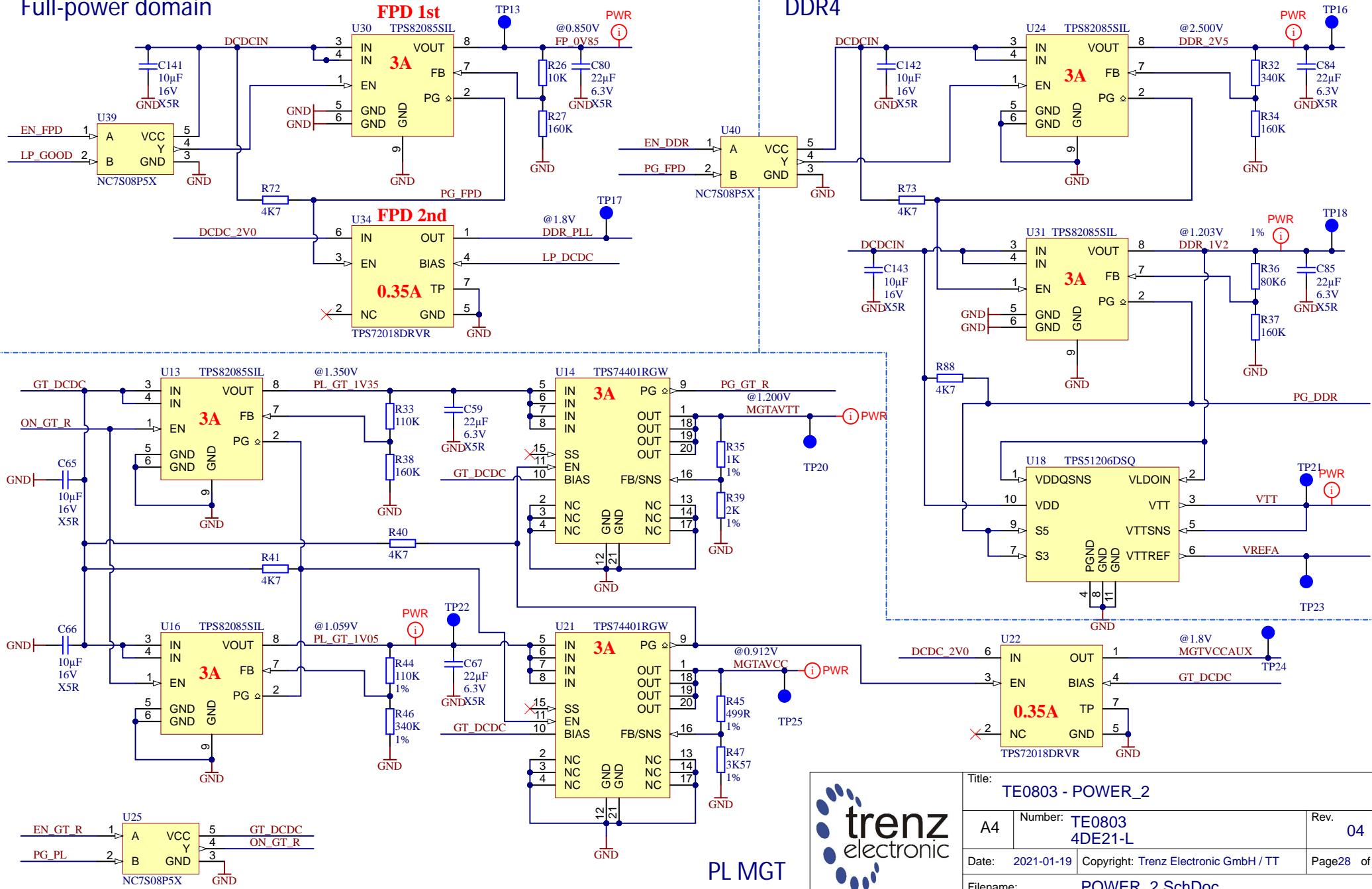
Title: TE0803 - POWER		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 26 of 30
Filename: POWER.SchDoc		



			Title: TE0803 - POWER	
			A4	Number: TE0803 4DE21-L
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT		Page 27 of 30
Filename: POWER_1.SchDoc				

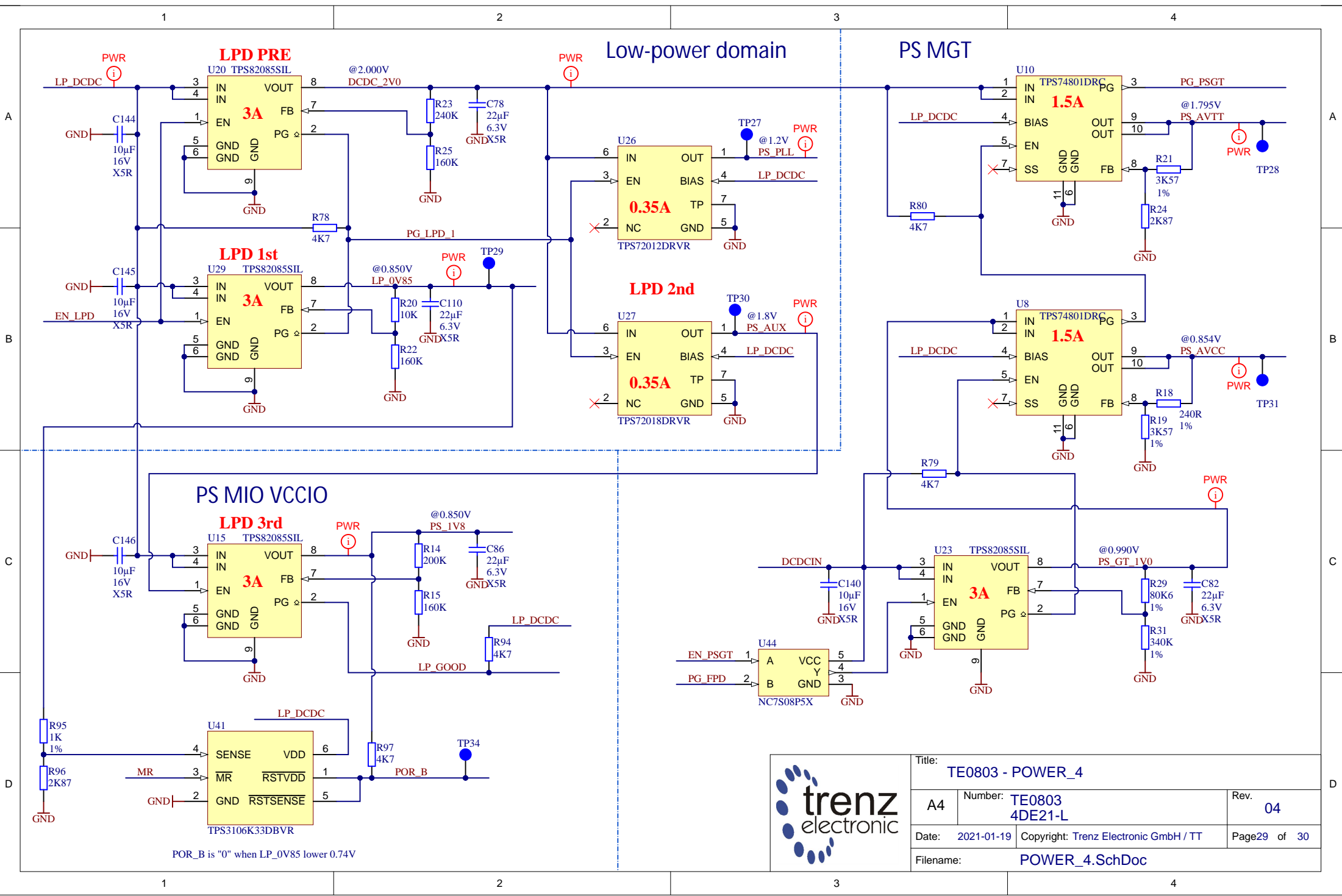
# Full-power domain

# DDR4



Title: <b>TE0803 - POWER_2</b>		
A4	Number: <b>TE0803 4DE21-L</b>	Rev. <b>04</b>
Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>28</b> of <b>30</b>
Filename: <b>POWER_2.SchDoc</b>		

PL MGT



Low-power domain

PS MGT


PS MIO VCCIO

POR\_B is "0" when LP\_0V85 lower 0.74V



Title: TE0803 - POWER_4		
A4	Number: TE0803 4DE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 29 of 30
Filename: POWER_4.SchDoc		

REV	DATE	Description	
-01		Initial revision	VT
-01a	20.11.2017	1. VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.	VT
-02	20.06.2018	1. Added LDO to DDR_PLL 2. All differential pairs wath length matched with tollerance 0.1mm (excluding package delays) 3. Added MAC EEPROM U28 4. VPS_MGTRAVCC set to 0.85V 5. Added pull-up resistors R68,R69	VT
-03	21.02.2019	1. Added support of DDP DDR4 2. Added support of Low power FPGA (-L1/L2). 3. Revised testpoints 4. Revised J1-J4 connectors net label style	VY
-04	15.12.2020	1. Revised PL_VCCINT power supply. EN63A0QI replaced by TPS548A28RWWR. PCB: revised routing and components placement; 2. Added support of wide SDRAM DDR4 packages. PCB: revised routing and components placement; 3. Added option to select POR_OVERRIDE level (R12 and R93) 4. VCCO pins if unused Bank 44 connected together. Same for unused Bank 24 (UG583 recomendation) 5. PCB: updated signal trace lengths. 6. PCB: updated silkscreen. Added company address, CE and WEEE symbols; 7. PCB: added module orientation rectangle poiner 8. Changed resistors value of R29, R31, R35, R39, R44-R47 (BOM optimization) 9. Removed traceability part (Obsolete component)	VY
-04	23.02.2022	10. Changed capacitor C92 for all variants from 100 nF to 1 nF.	ED

				Title: <b>TE0803 - Revision History</b>	
				A4	Number: <b>TE0803 4DE21-L</b>
Date: 2021-01-19		Copyright: Trenz Electronic GmbH		Page 30 of 30	
Drawn by: VY			Filename: Revision Changes.SchDoc		