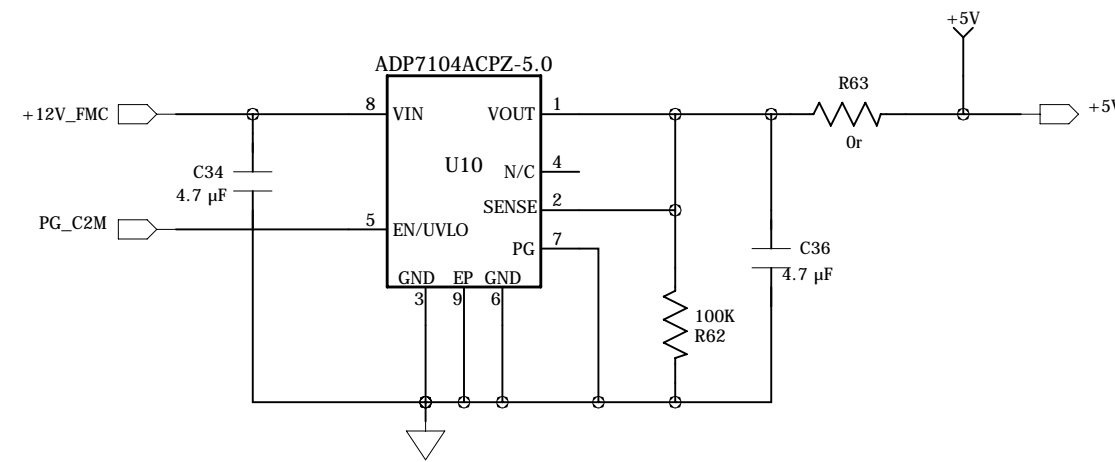
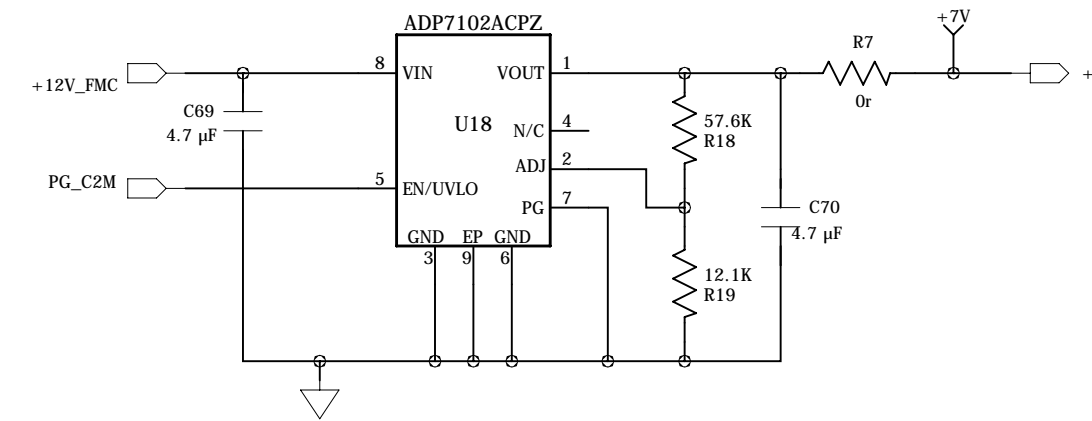


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

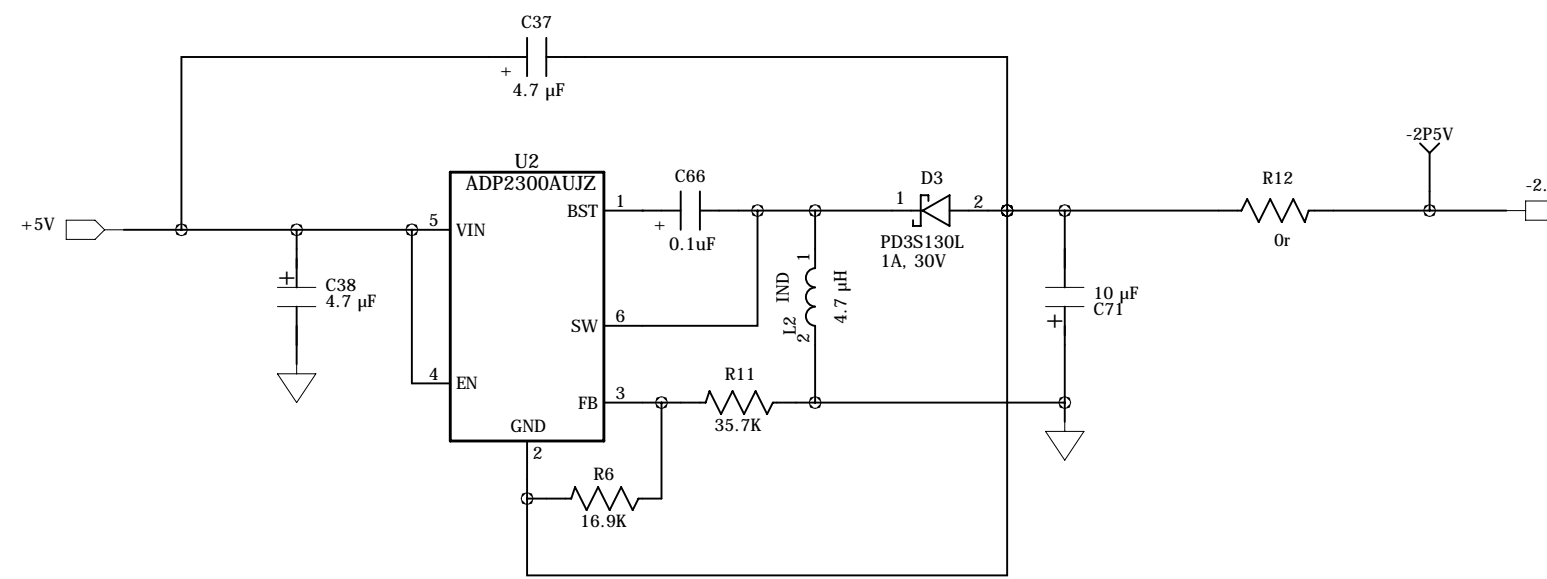
# Power Supplies



VIN = +12V , VOUT= +5V, IOU T = upto 500 mA



VIN = +12V , VOUT= +7V, IOU T = upto 300 mA



VIN = +5V , VOUT= -2.5V, IOU T = 250 mA

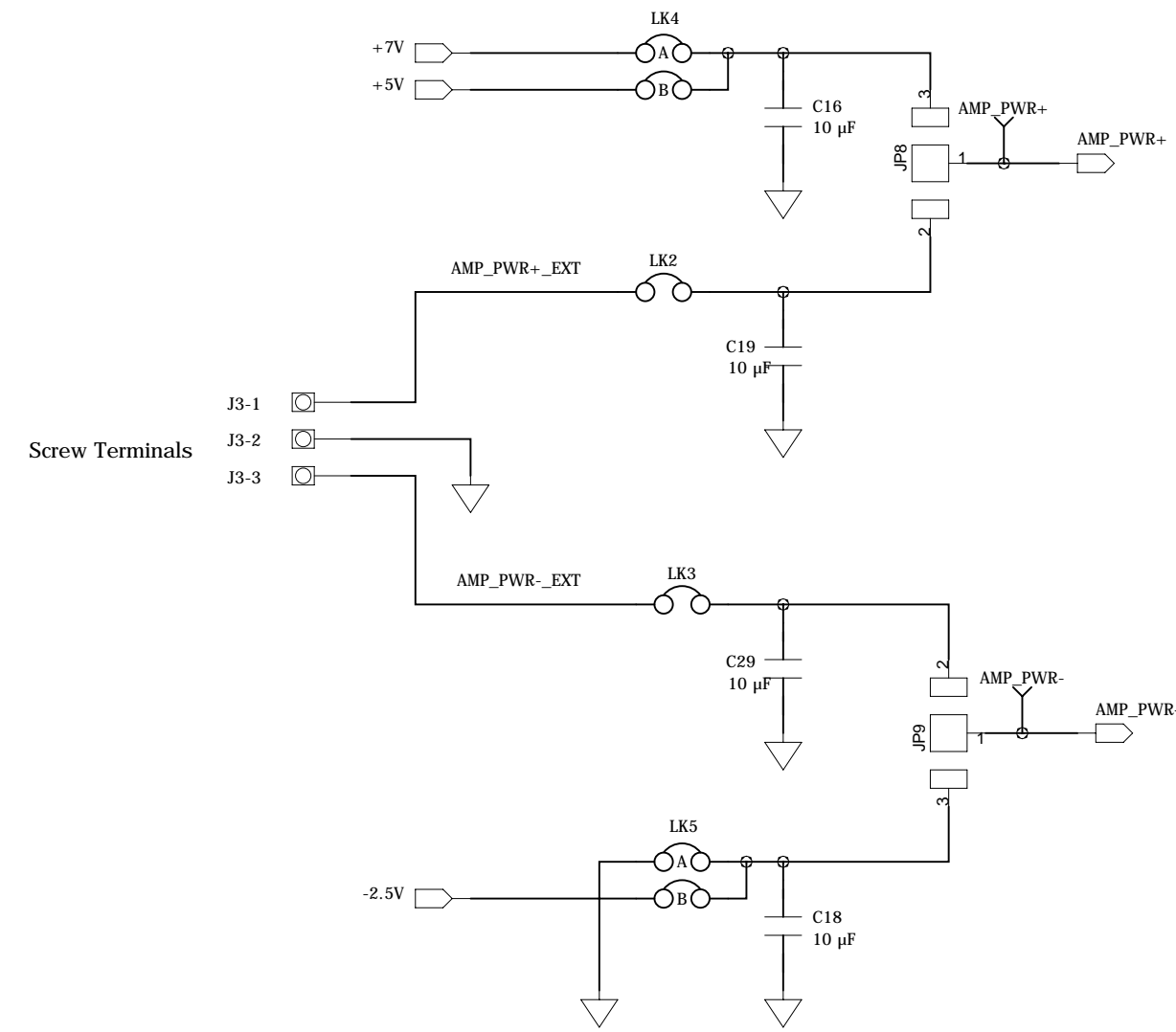
COMPANY: Analog Devices

TITLE: AD7961 Eval Board

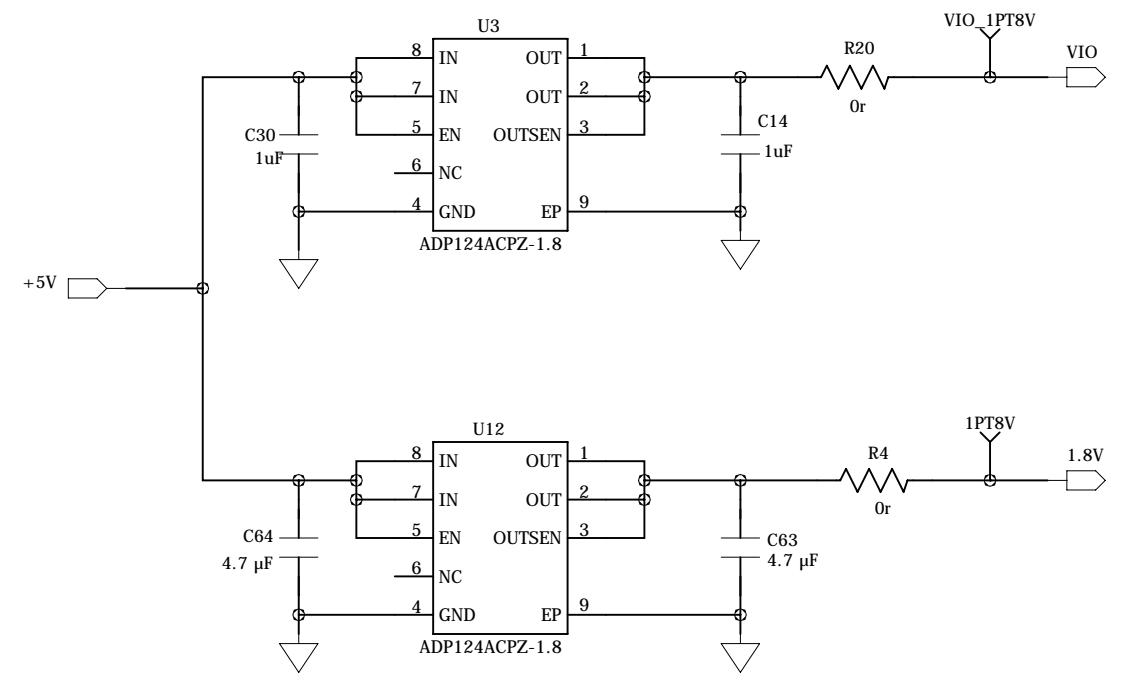
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CHECKED: <Checked By>	DATED: <Checked Date>	<Code>	A2	EVAL-AD7961FMCZ	0		
QUALITY CONTROL: <QC By>	DATED: <QC Date>						
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>				SHEET: 1 OF 6	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# Power Supplies



## OPAMP POWR SUPPLY OPTIONS

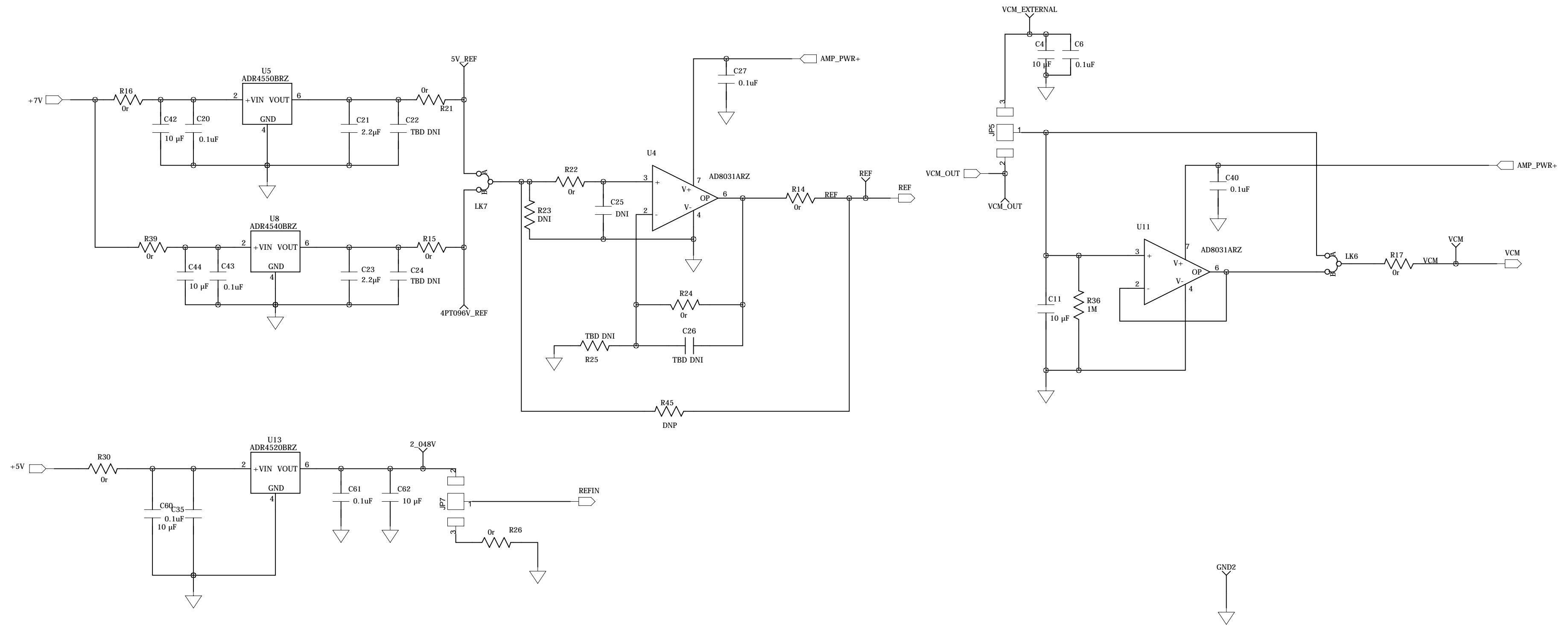


The ADP124 is available in 2mmx2mm LFCSP packages.

COMPANY:				Analog Devices			
TITLE:				AD7961 Eval Board			
DRAWN:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:		
Maithil P.	June 13	<Code>	A2	EVAL-AD7961FMCZ	0		
CHECKED:	DATED:	QUALITY CONTROL:	RELEASED:	SCALE:			
<Checked By>	<Checked Date>	<QC By>	<Release Date>	<Scale>			

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# External Reference



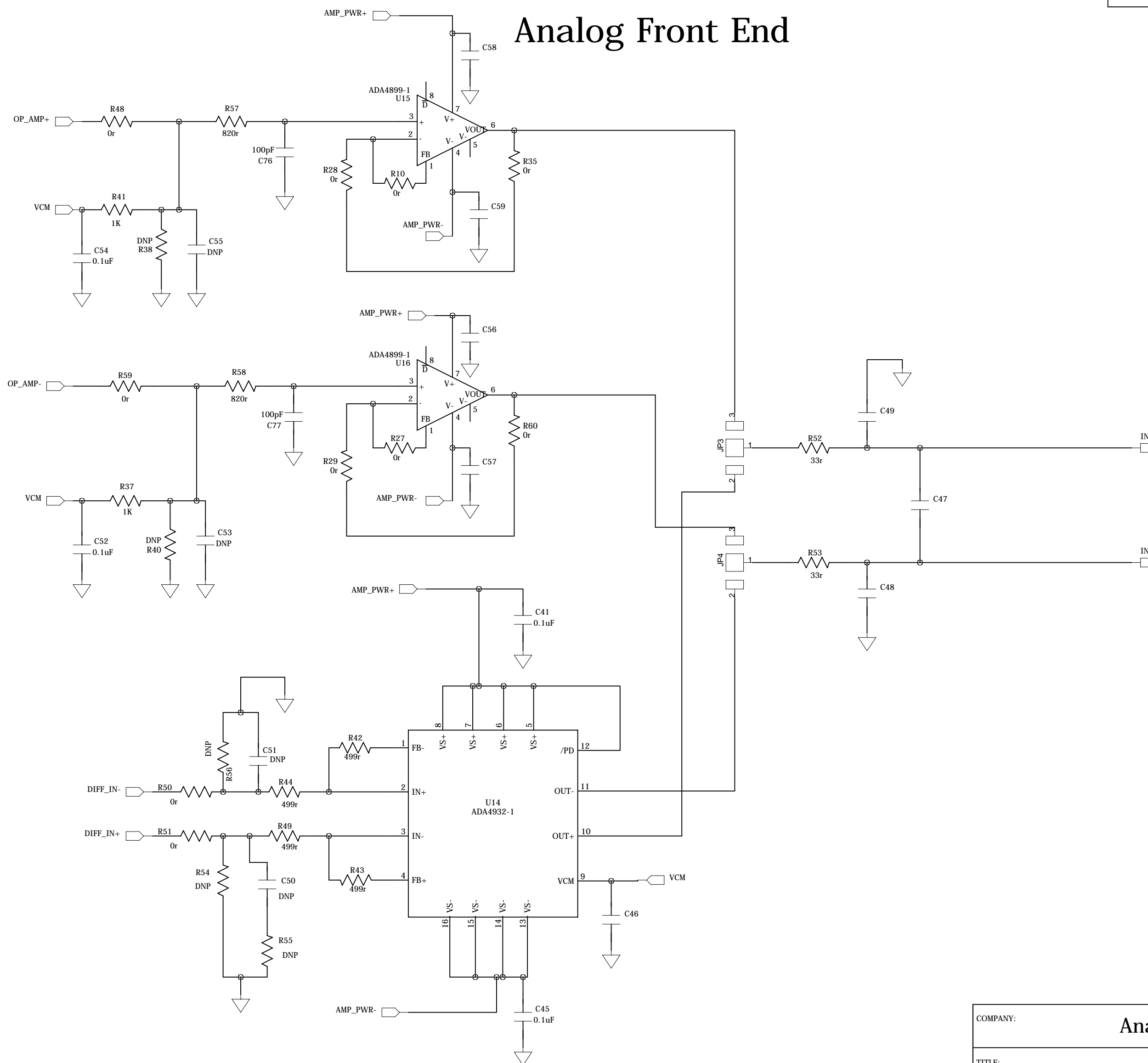
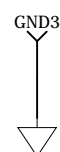
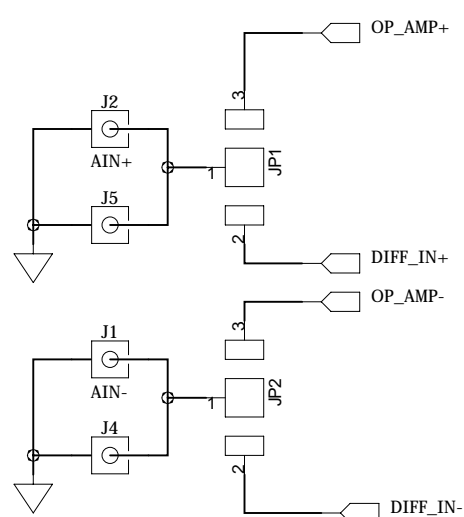
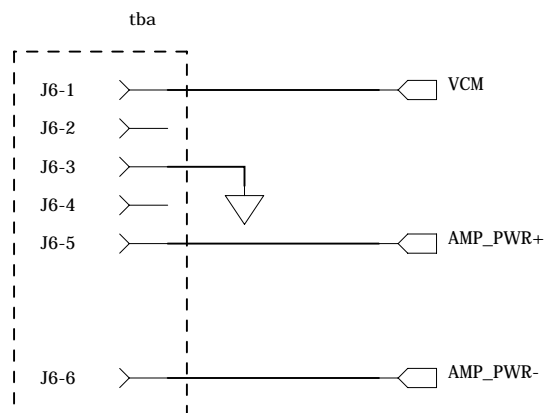
There are 3 options for using an External Reference

- 1) Externally buffered reference source of 5V applied to the REF pin.
- 2) Externally buffered reference source of 4.096V applied to the REF pin.
- 3) External reference of 2.048V applied to the REFIN pin (high impedance input). The on-chip buffer gains this by 2 and drives the REF pin with 4.096V.

COMPANY:				Analog Devices			
TITLE:				AD7961 Eval Board			
DRAWN:	Maitil P.	DATED:	June 13	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	<Checked By>	DATED:	<Checked Date>	<Code>	A2	EVAL-AD7961FMCZ	0
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>	SCALE: <Scale>		SHEET: 3 OF 6	
RELEASED:	<Released By>	DATED:	<Release Date>				

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# Analog Front End



COMPANY: Analog Devices

TITLE: AD7961 Eval Board

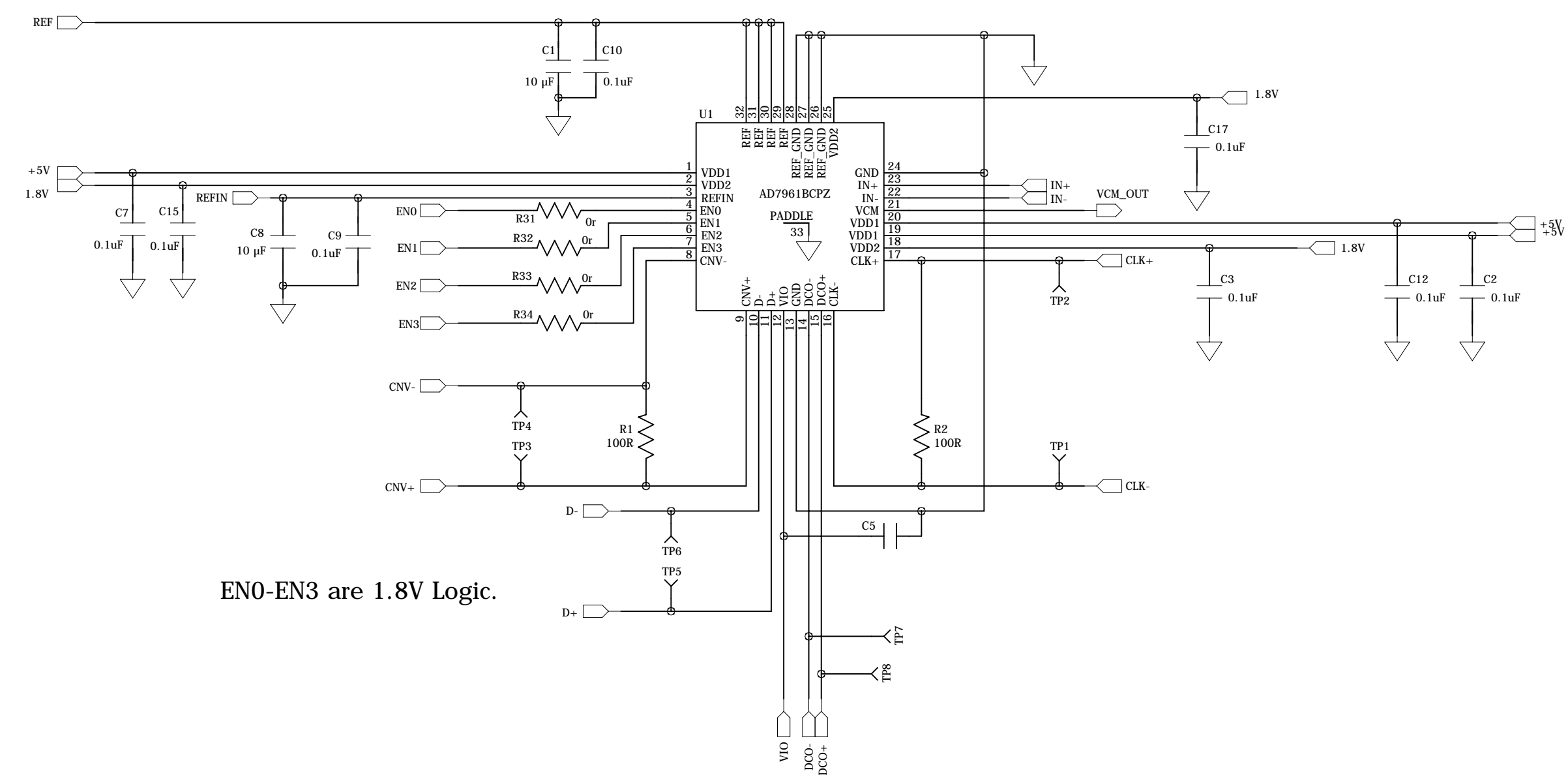
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CHECKED: <Checked By>	DATED: <Checked Date>
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RELEASED: <Released By>	DATED: <Release Date>

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	EVAL-AD7961FMCZ	0
SCALE: <Scale>			SHEET: 4 OF 6

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# AD7961

C1 and C10 should be placed between REF and REF\_GND and be placed very close to the DUT



EN0-EN3 are 1.8V Logic.

All the decoupling cap must be placed very close to the DUT

COMPANY: Analog Devices

TITLE: AD7961 Eval Board

DRAWN: Maithil P.	DATED: June 13
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	EVAL-AD7961FMCZ	0
SCALE: <Scale>			SHEET: 5 OF 6

6

5

4

3

2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# FMC-LPC Male Connector

The diagram shows the electrical connections for the FMC-LPC Male Connector. It is divided into four sections: J7-A, J7-B, J7-C, and J7-D.

- J7-A (ASP-134604-01):** Connects to an I2C EEPROM (U7, M24C02-WMN6TP) and an FPGA I2C line. The EEPROM is powered by 3P3VAUX through a resistor R9 and a capacitor C186. Its VCC is connected to pin 1, E0 to pin 2, E1 to pin 3, SCL to pin 6, WP to pin 7, and VSS to pin 4. The SDA pin (5) is connected to the FPGA I2C line. A note states: "EEPROM required in VITA standard I2C line pull-up resistors on FPGA board".
- J7-B (ASP-134604-01):** Connects to various signals including PG\_C2M, CNV+, and CNV-. It also provides power connections for 3P3VAUX, GA0, GA1, +12V, and +12V\_FMC. A green LED is connected to +12V\_FMC through a resistor R101 (560r).
- J7-C (ASP-134604-01):** Connects to signals like CLK+, CLK-, EN0\_FMC, and EN1\_FMC. It also provides power connections for 3P3VAUX, GA1, and VADJ.
- J7-D (ASP-134604-01):** Connects to signals like DCO+, DCO-, D+, D-, EN2\_FMC, and EN3\_FMC. It also provides power connections for VADJ and Board present pin.

At the bottom, a level shifter circuit (U9, FXL4TD245BQX) is shown. It is powered by 1.8V and VADJ. Its VCCA pin (1) is connected to 1.8V through a 0.1uF capacitor (C31). Its VCCB pin (16) is connected to VADJ through a 0.1uF capacitor (C28). The level shifter has four input pins (A0-A3) and four output pins (EN3\_FMC-EN0\_FMC). Its T/R0-T/R3 pins (2, 3, 4, 5) are connected to EN3, EN2, EN1, and EN0 respectively. Its T/RZ pins (10, 11, 12, 13) are connected to EN0\_FMC, EN1\_FMC, EN2\_FMC, and EN3\_FMC respectively. Its OE pin (9) is connected to PG\_C2M through an inverter (U17, NC7S04). Its EP pin (17) is connected to GND.

COMPANY: Analog Devices			
TITLE: AD7961 Eval Board			
DRAWN: Maithil P.	DATED: June 13	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: EVAL-AD7961FMCZ	REV: 0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	
RELEASED: <Released By>	DATED: <Release Date>	SHEET: 6 OF 6	