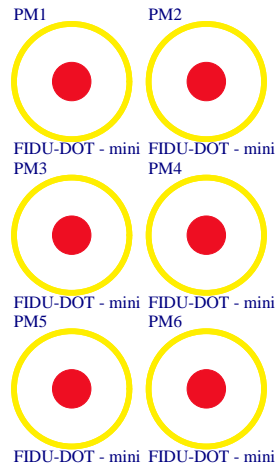
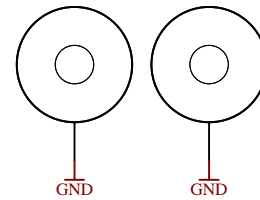


- U\_B2B-Connectors  
B2B-Connectors.SchDoc
- U\_B13  
B13.SchDoc
- U\_B14  
B14.SchDoc
- U\_B15  
B15.SchDoc
- U\_B16  
B16.SchDoc
- U\_B34  
B34.SchDoc
- U\_FPGA-MGT  
FPGA-MGT.SchDoc
- U\_FPGA-CFG  
FPGA-CFG.SchDoc
- U\_FPGA-PWR  
FPGA-PWR.SchDoc
- U\_Clock  
Clock.SchDoc
- U\_DDR3-RAM  
DDR3-RAM.SchDoc
- U\_USB  
USB.SchDoc
- U\_CPLD  
CPLD.SchDoc
- U\_PWR1  
PWR1.SchDoc
- U\_PWR2  
PWR2.SchDoc

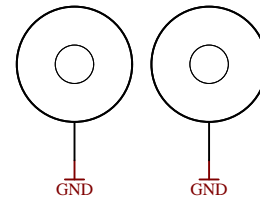
Serial  
Serialnumber 6,3 x 6.3mm



Mount.Hole 3.2mm Mount.Hole 3.2mm

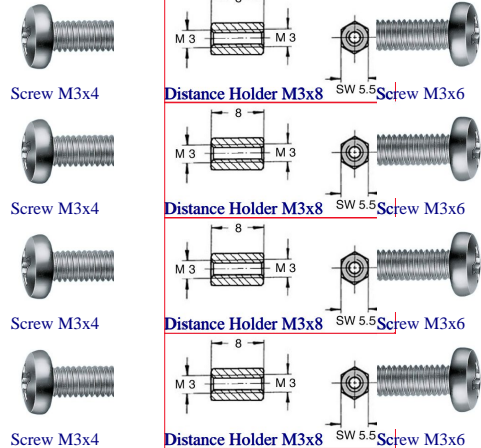


Mount.Hole 3.2mm Mount.Hole 3.2mm



LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Top of Board



		Title: TE0713	
		A4	Number: TE0713 72C46-A
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A

B

C

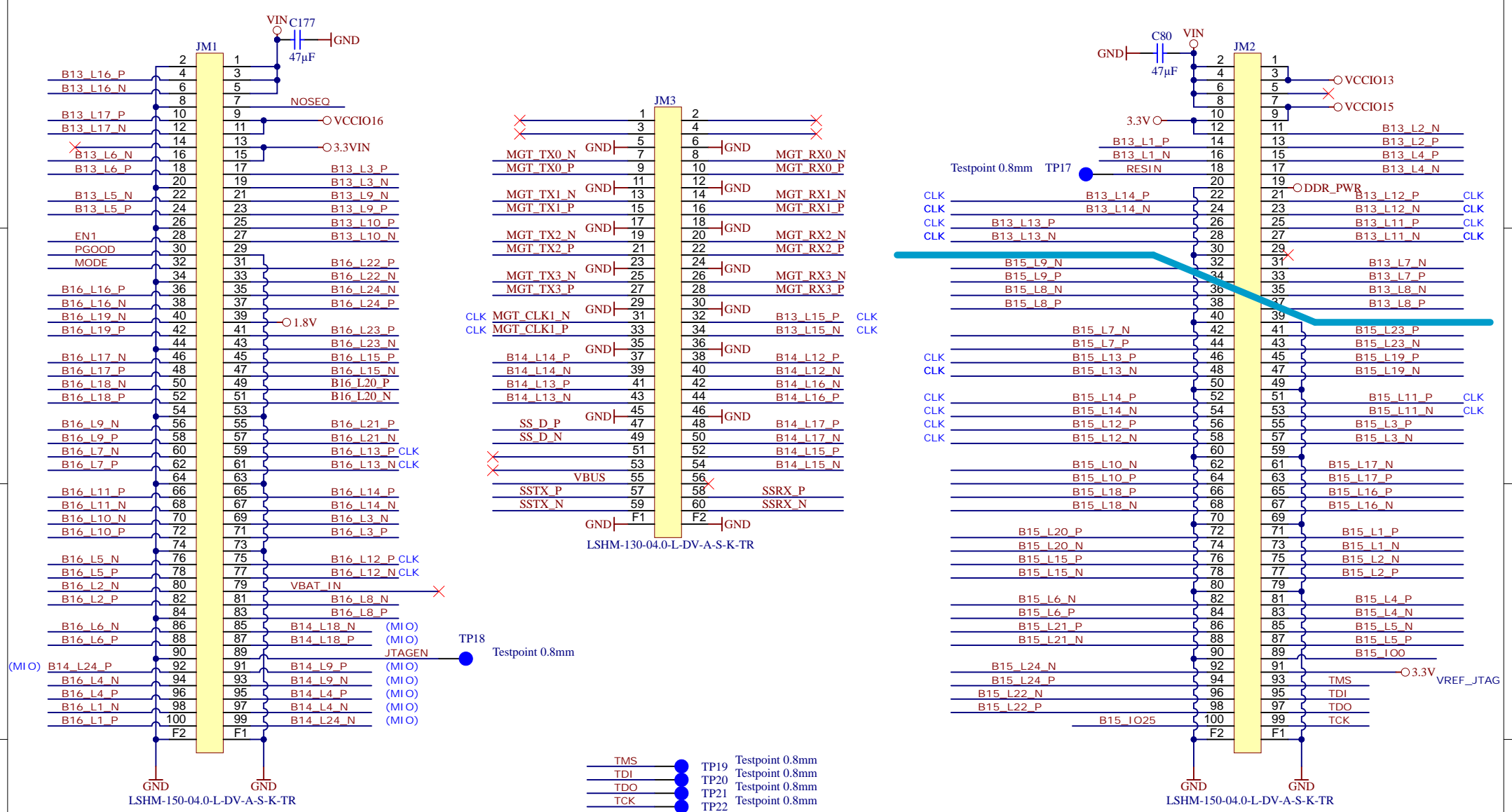
D

A

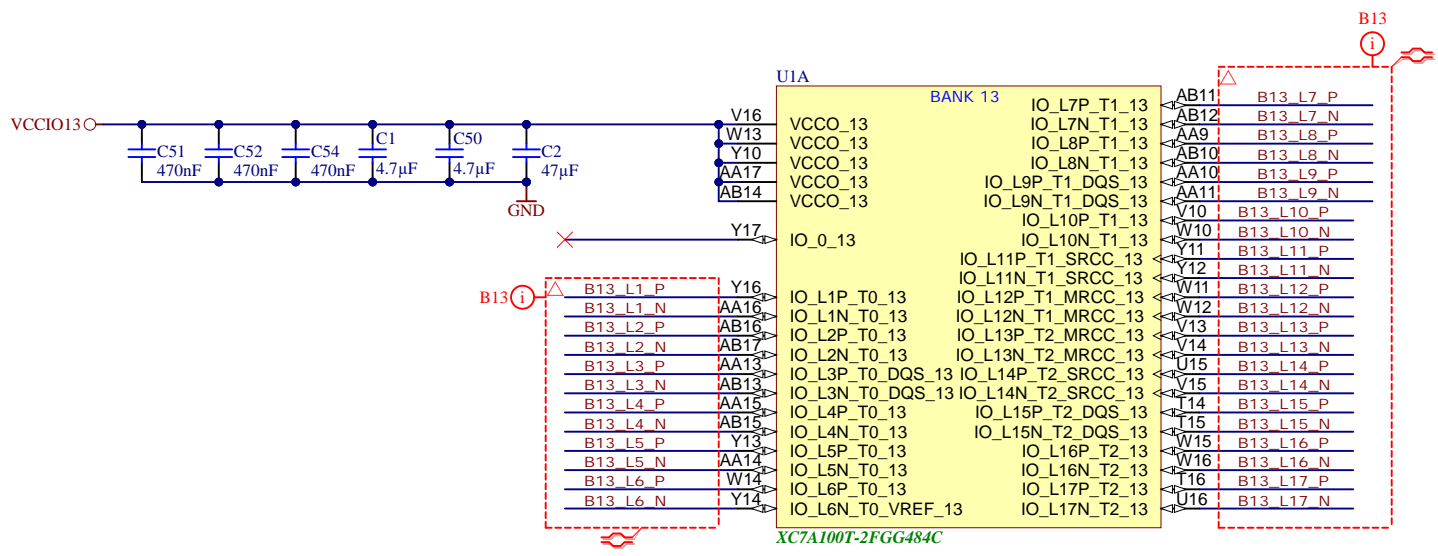
B

C

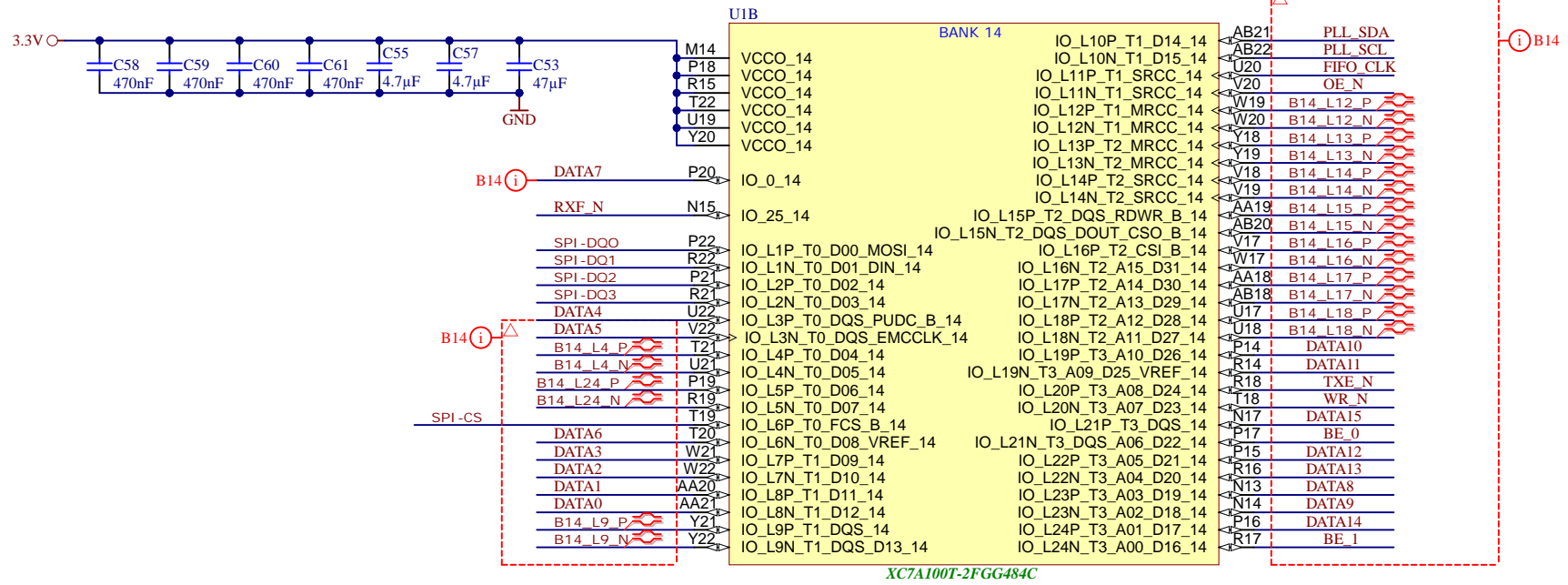
D



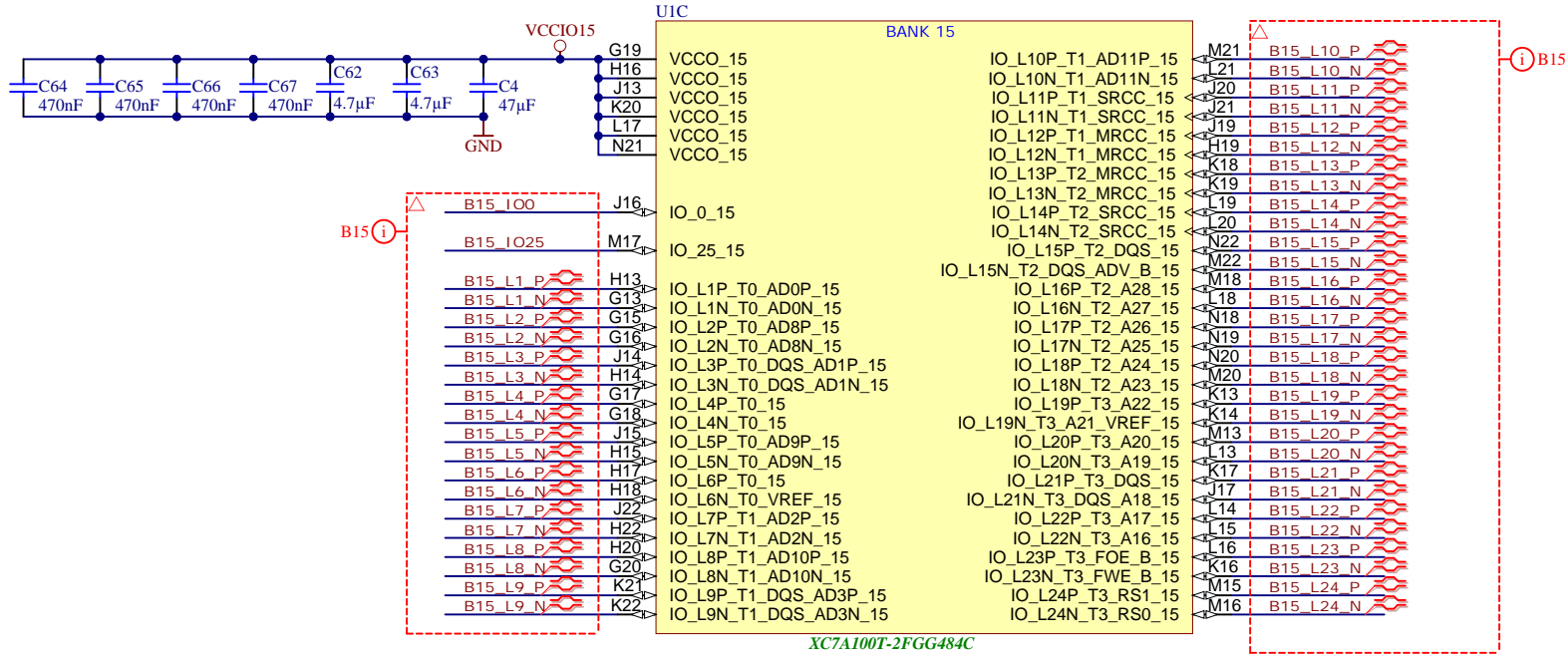
	Title: <b>B2B</b>	
	A4	Number: <b>TE0713 72C46-A</b>
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Title: <b>B13</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
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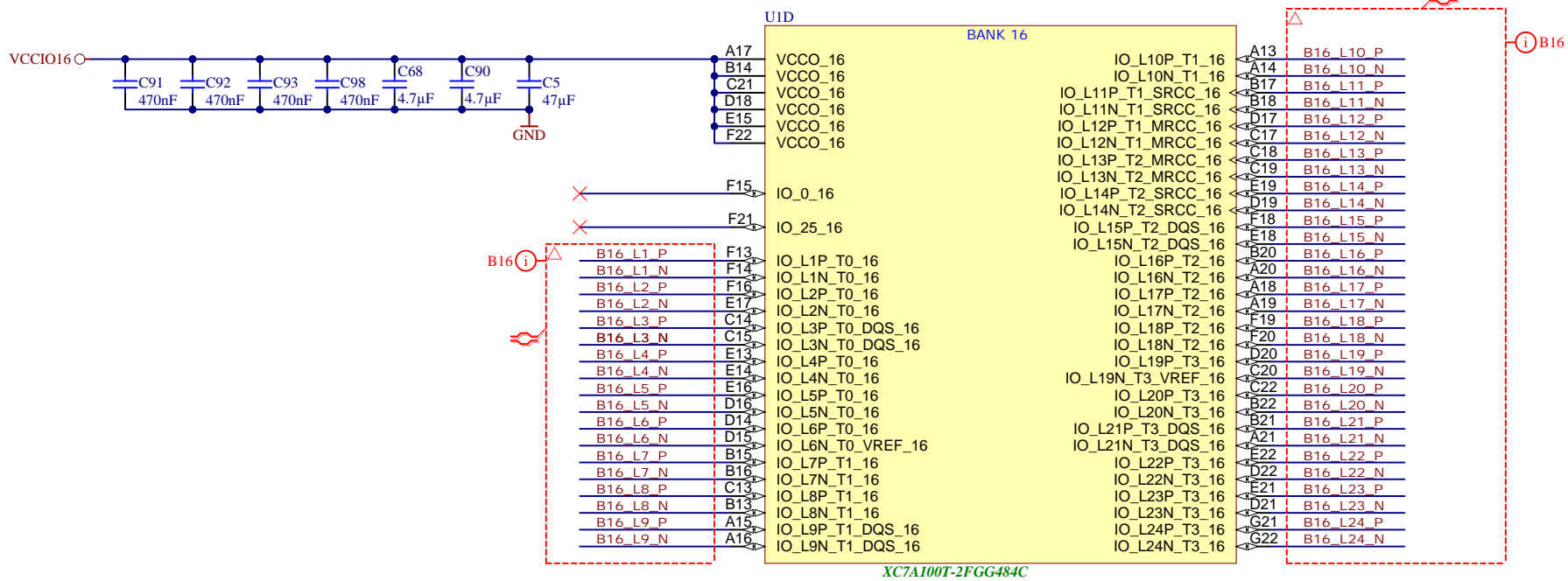
Title: <b>B14</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
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Filename: <b>B14.SchDoc</b>		



XC7A100T-2FGG484C



Title: <b>B15</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
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	Title: <b>B16</b>	
	A4	Number: <b>TE0713 72C46-A</b>
	Date: <b>2018-09-25</b>	Copyright: <b>Trenz Electronic GmbH</b>
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Filename: <b>B16.SchDoc</b>		

1

2

3

4

A

A

B

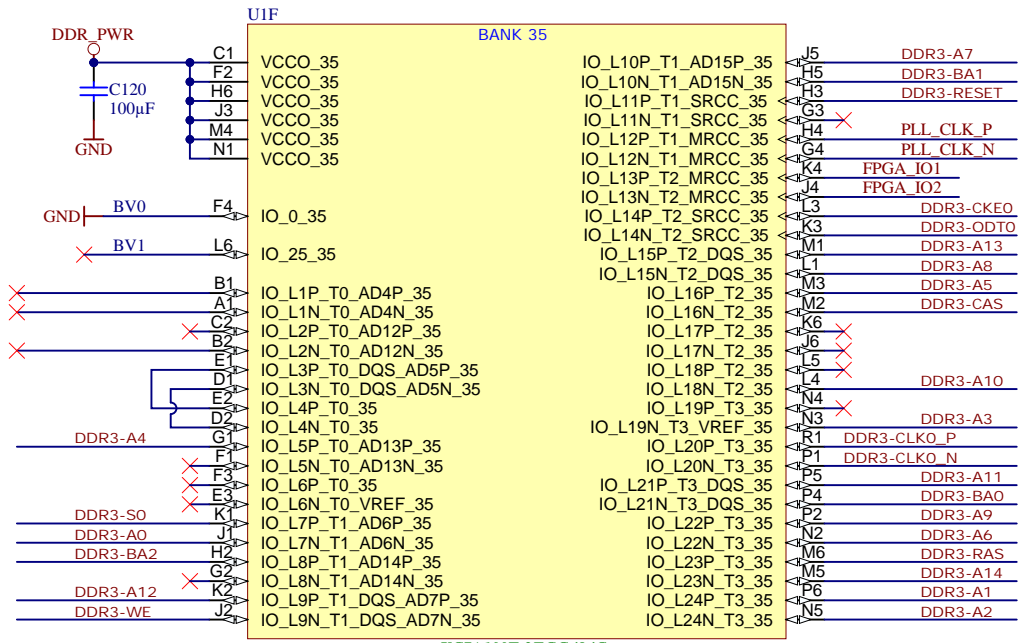
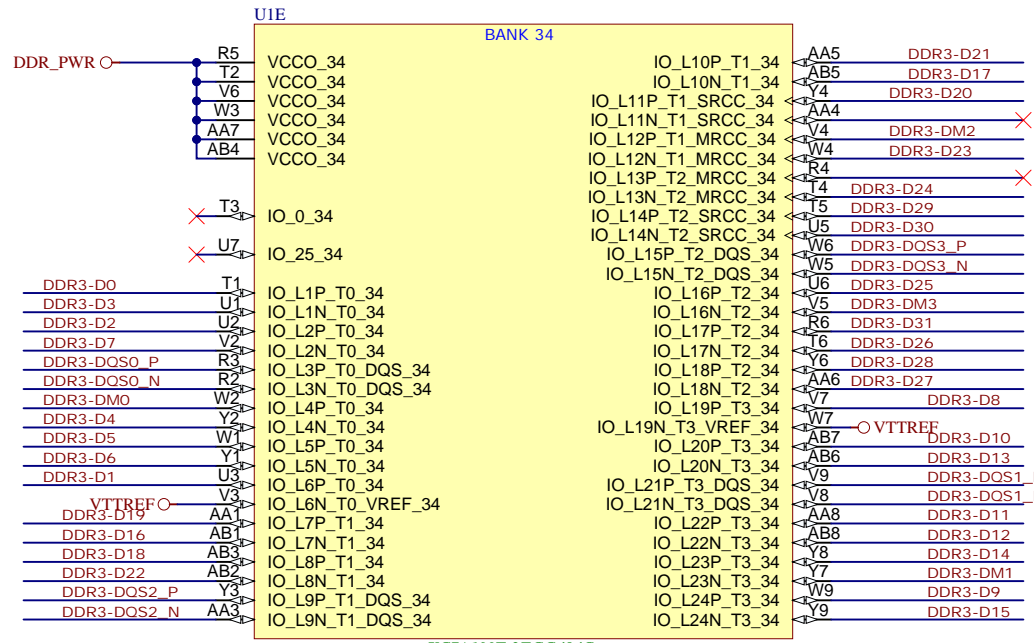
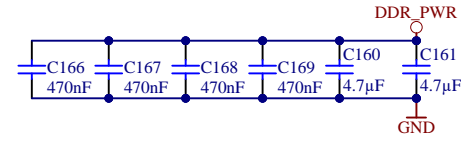
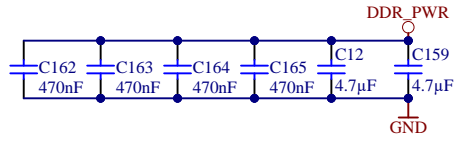
B

C

C

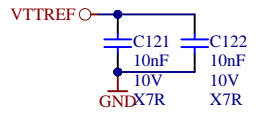
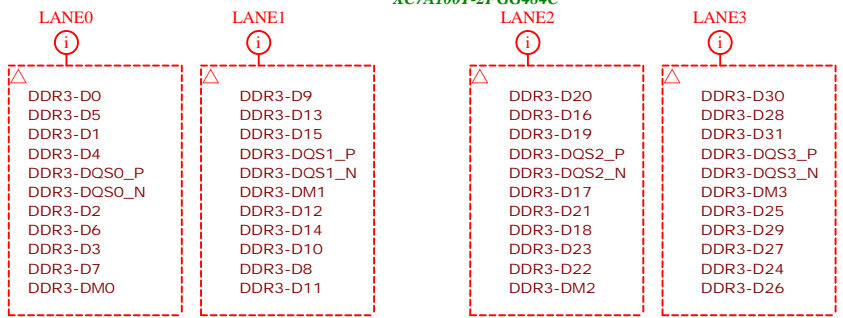
D

D



XC7A100T-2FGG484C

XC7A100T-2FGG484C



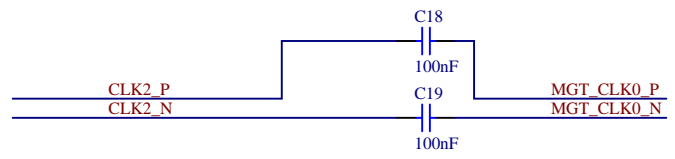
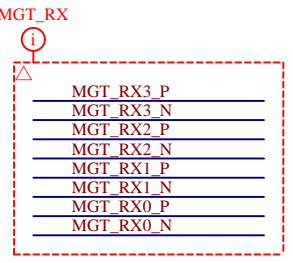
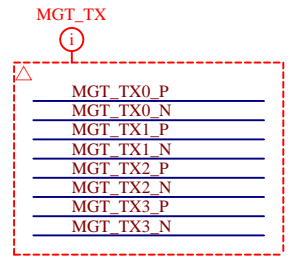
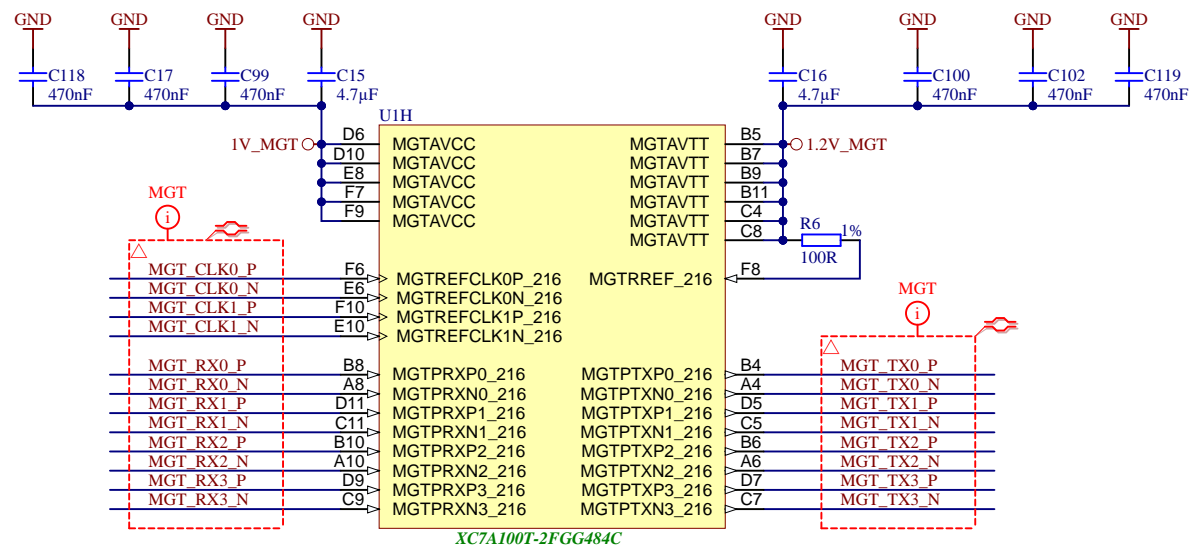
Title: B34		
A4	Number: TE0713 72C46-A	Rev. 02
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1

2

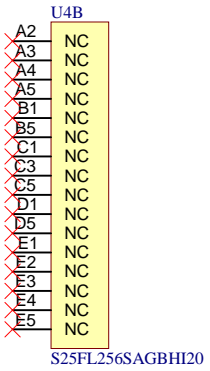
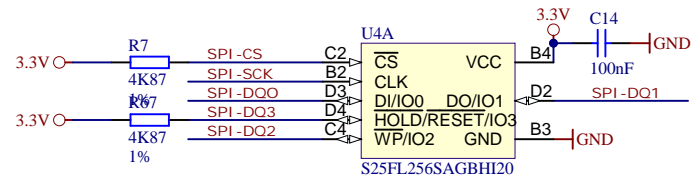
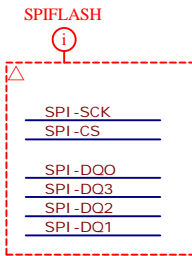
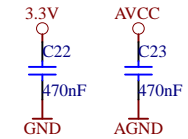
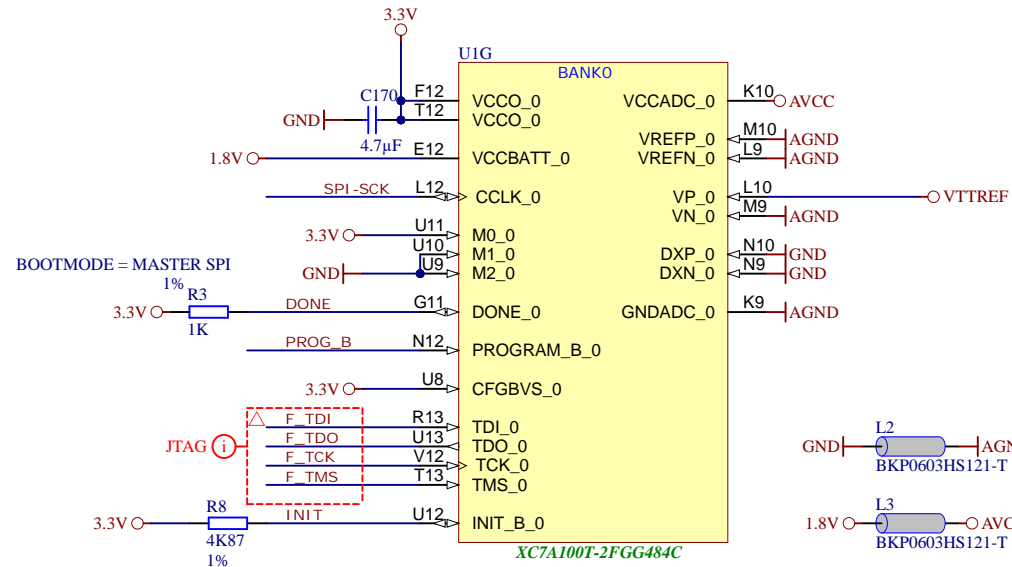
3

4



	Title: <b>MGT</b>	
	A4	Number: <b>TE0713 72C46-A</b>
	Date: <b>2018-09-25</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Filename: <b>FPGA-MGT.SchDoc</b>	
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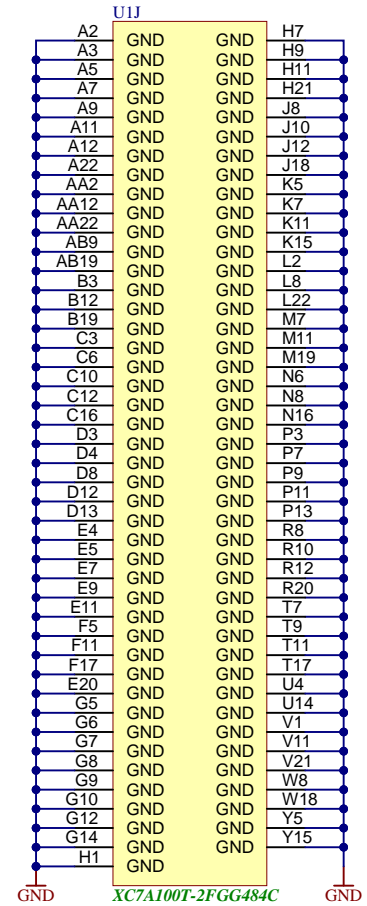
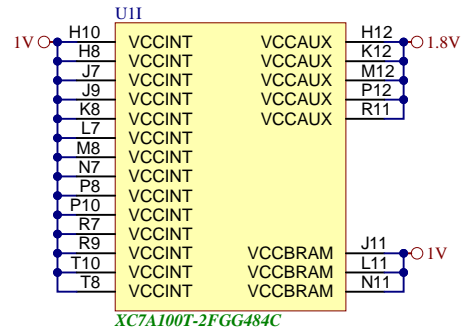
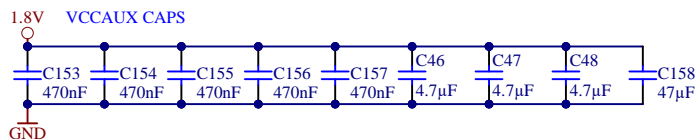
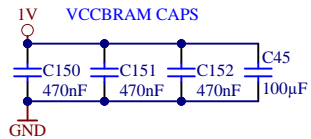
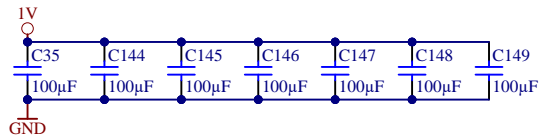
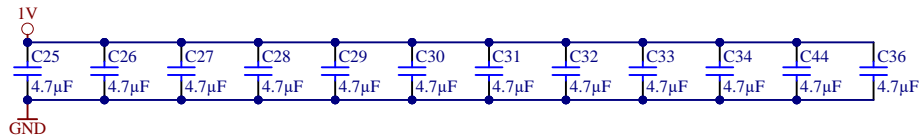
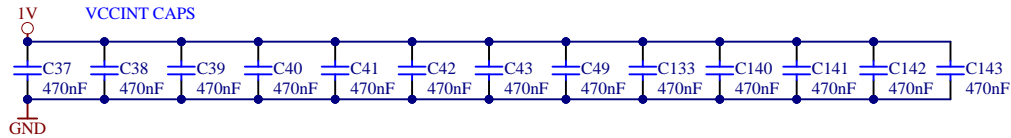





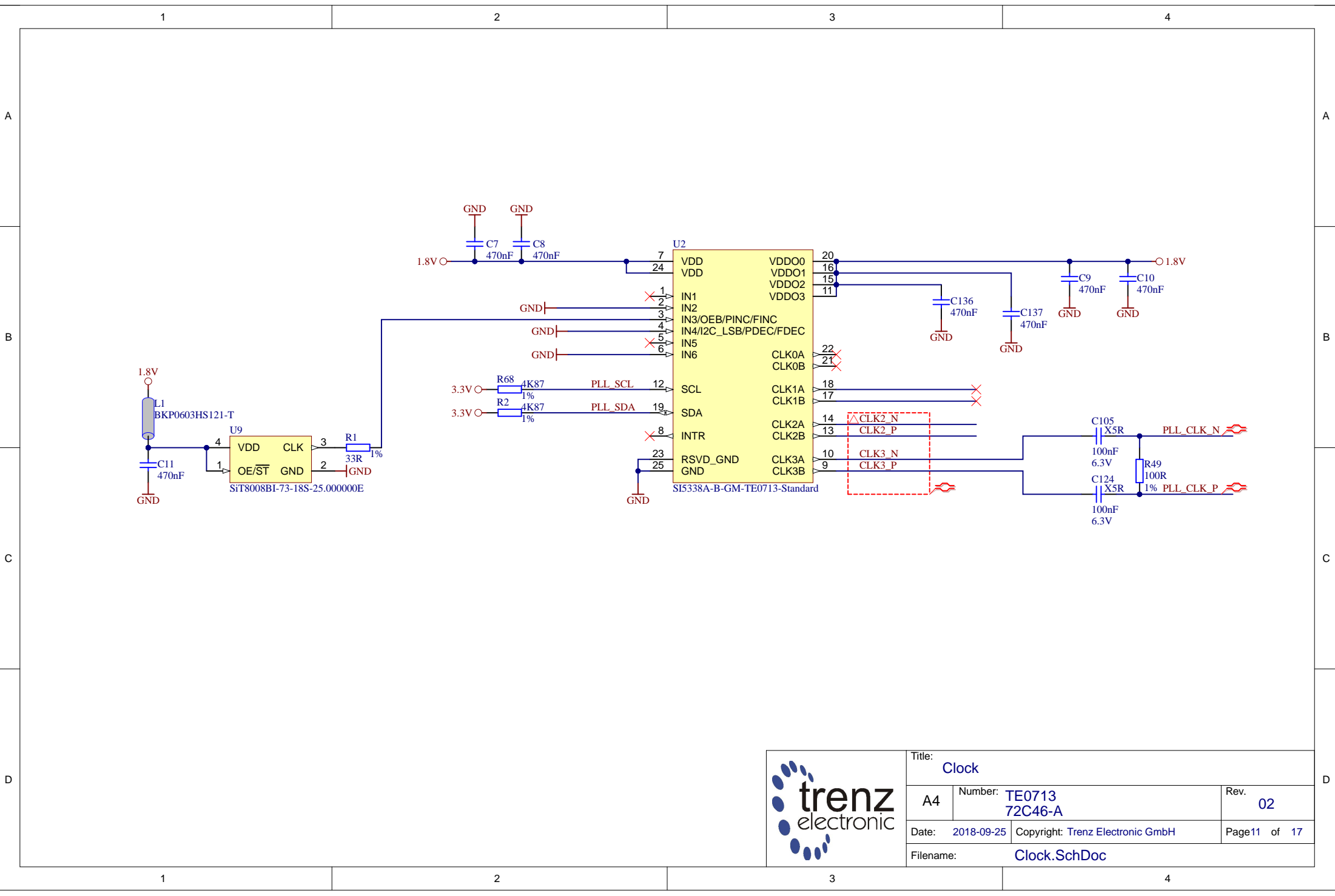
trenz electronic

Title: CFG

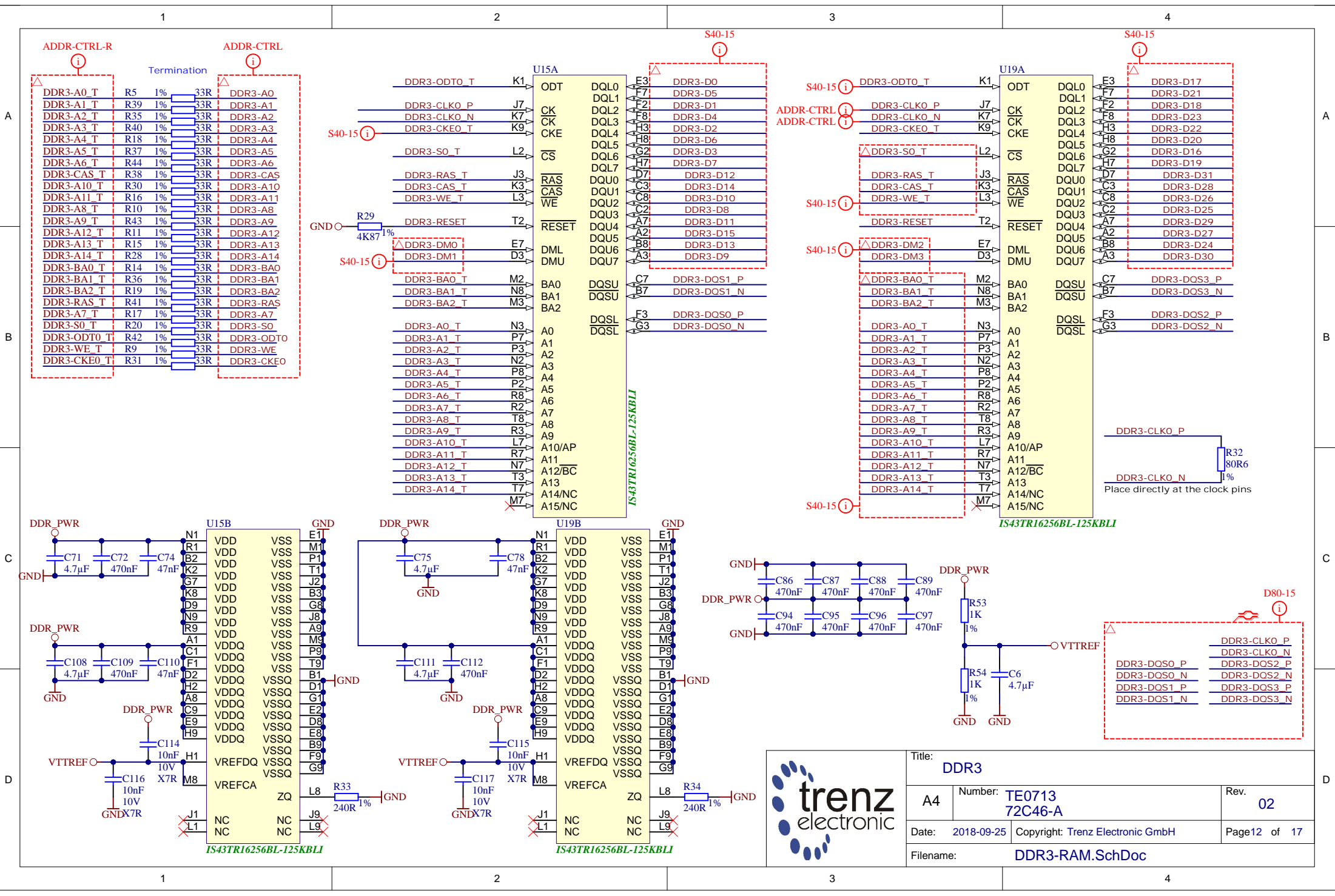
A4	Number: TE0713 72C46-A	Rev. 02
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Filename: FPGA-CFG.SchDoc		

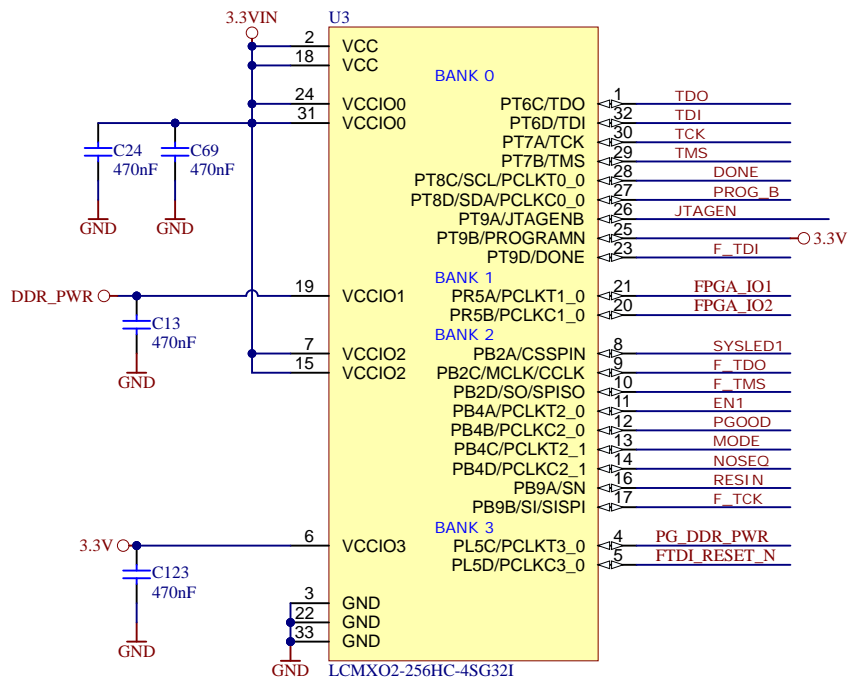
Title: PWR		
A4	Number: TE0713 72C46-A	Rev. 02
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Filename: FPGA-PWR.SchDoc		



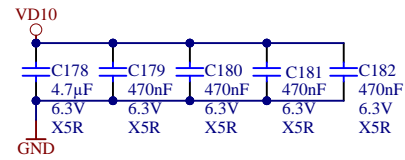
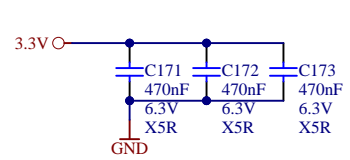
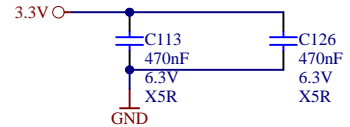
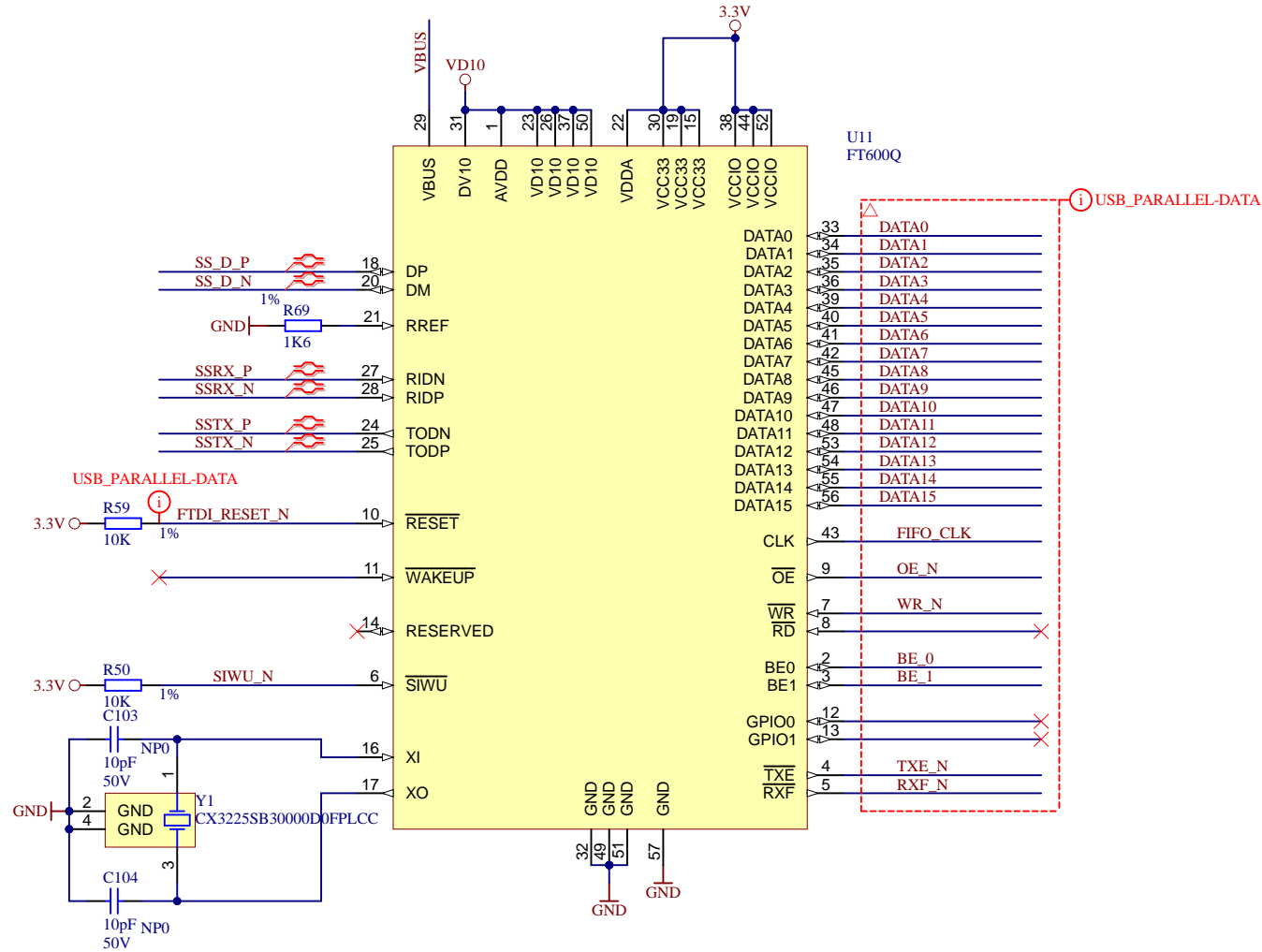
Title: Clock		
A4	Number: TE0713 72C46-A	Rev. 02
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Filename: Clock.SchDoc		



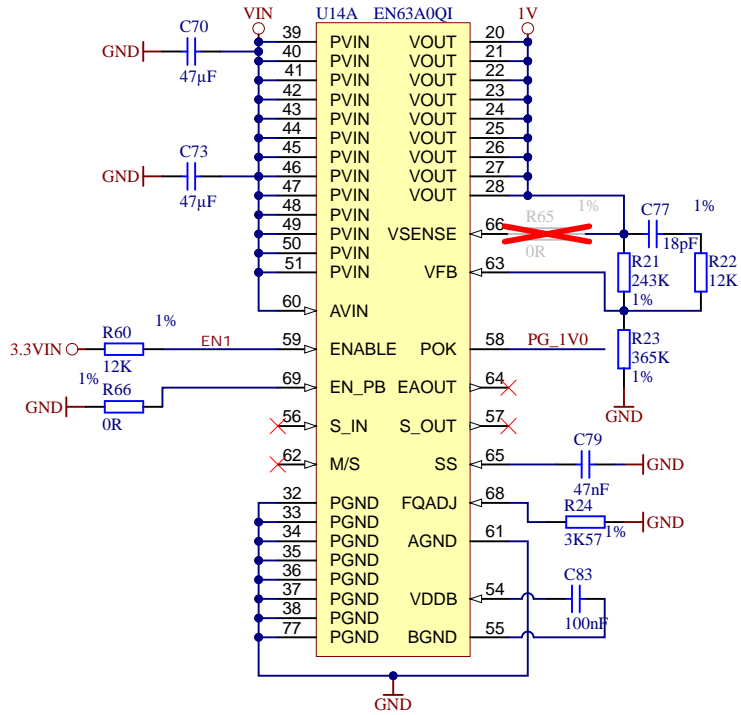
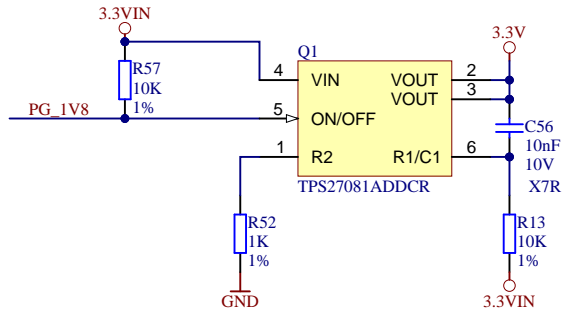
Title: <b>DDR3</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
Date: <b>2018-09-25</b>	Copyright: Trenz Electronic GmbH	
Filename: <b>DDR3-RAM.SchDoc</b>		Page <b>12</b> of <b>17</b>



	Title: <b>CPLD</b>		
	A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
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	Filename: <b>CPLD.SchDoc</b>		



Title: <b>TE0713 - FTDI USB</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
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Filename: <b>USB.SchDoc</b>		

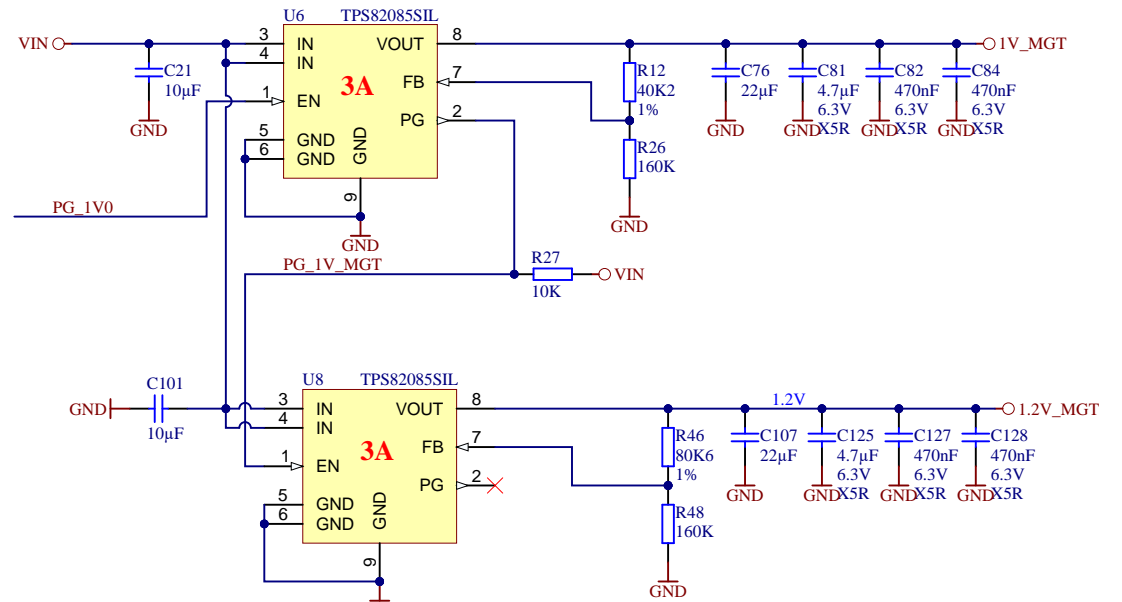
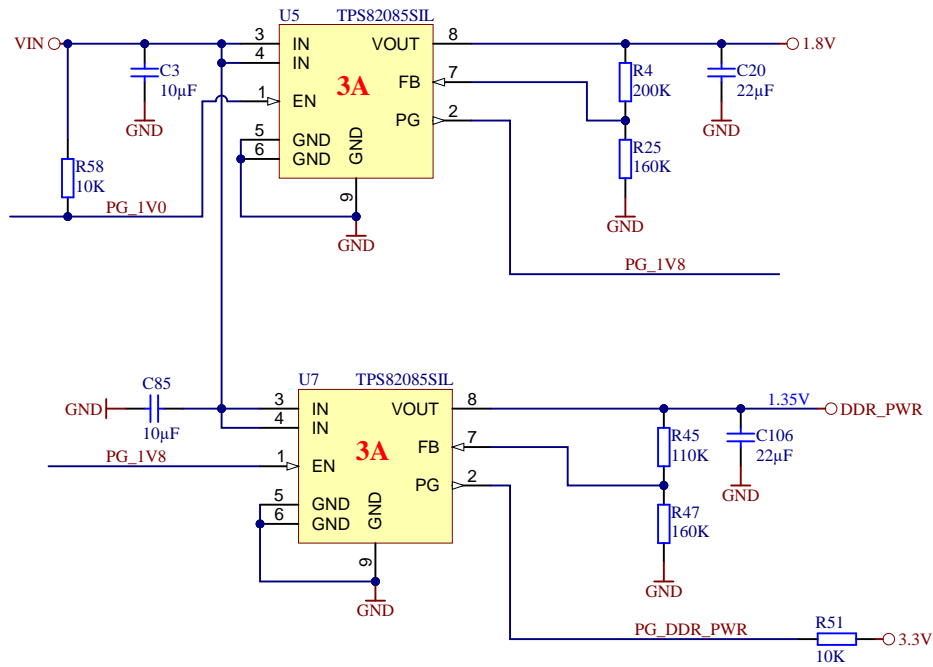


Pin	Symbol	Value	Pin	Symbol	Value
1	NC	NC	17	NC	NC
2	NC	NC	18	NC	NC
3	NC	NC	19	NC	NC
4	NC	NC	29	NC	NC
5	NC	NC(SW)	30	NC	NC
6	NC	NC(SW)	31	NC	NC
7	NC	NC	52	NC	NC
8	NC	NC	53	NC	NC
9	NC	NC	67	NC	NC
10	NC	NC	70	NC	NC
11	NC	NC(SW)	71	NC	NC
12	NC	NC(SW)	72	NC	NC
13	NC	NC	73	NC	NC
14	NC	NC	74	NC	NC
15	NC	NC	75	NC	NC
16	NC	NC	76	NC	NC

R65 R66 MODE EN63A0QI  
 -----  
 OK X | enable pre-bias start-up  
 X OK | disable pre-bias start-up

- |                                  |                                  |                              |
|----------------------------------|----------------------------------|------------------------------|
| VIN ○ TP1 ● Testpoint 0.8mm      | 1V ○ TP2 ● Testpoint 0.8mm       | GND ○ TP6 ● Testpoint 0.8mm  |
| 3.3VIN ○ TP4 ● Testpoint 0.8mm   | 1.2V_MGT ○ TP5 ● Testpoint 0.8mm | GND ○ TP9 ● Testpoint 0.8mm  |
| 3.3V ○ TP7 ● Testpoint 0.8mm     | VCCIO13 ○ TP8 ● Testpoint 0.8mm  | GND ○ TP12 ● Testpoint 0.8mm |
| 1.8V ○ TP10 ● Testpoint 0.8mm    | VCCIO15 ○ TP11 ● Testpoint 0.8mm | GND ○ TP15 ● Testpoint 0.8mm |
| DDR_PWR ○ TP13 ● Testpoint 0.8mm | VCCIO16 ○ TP14 ● Testpoint 0.8mm | GND ○ TP16 ● Testpoint 0.8mm |
| VTTREF ○ TP3 ● Testpoint 0.8mm   |                                  |                              |

	Title: PWR	
	A4	Number: TE0713 72C46-A
	Date: 2018-09-25	Copyright: Trenz Electronic GmbH
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Filename: PWR1.SchDoc		



	Title: PWR		
	A4	Number: TE0713 72C46-A	Rev. 02
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	Filename: PWR2.SchDoc		



1

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3

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Changes REV 02:

- 1. Added pull-up resistor R57 (10k) to PG\_1V8
- 2. Added pull-up resistor R58 (10k) to PG\_1V0
- 3. Added pull-up resistor R59 (10k) to FTDI\_RESET\_N
- 4. Changed NRND component Q1 TPS27082LDDCR -> TPS27081ADDCR
- 5. Removed 100R resistors (R52,R56)
- 6. Full upd LIB

A

A

B


B

C

C

D

D

	Title: <b>TE0714</b>		
	A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>02</b>
	Date: <b>2018-09-25</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>17</b> of <b>17</b>
	Filename: <b>Revision Changes.SchDoc</b>		

1

2

3

4