Si51210 Data Sheet

Two Output Factory Programmable Clock Generator

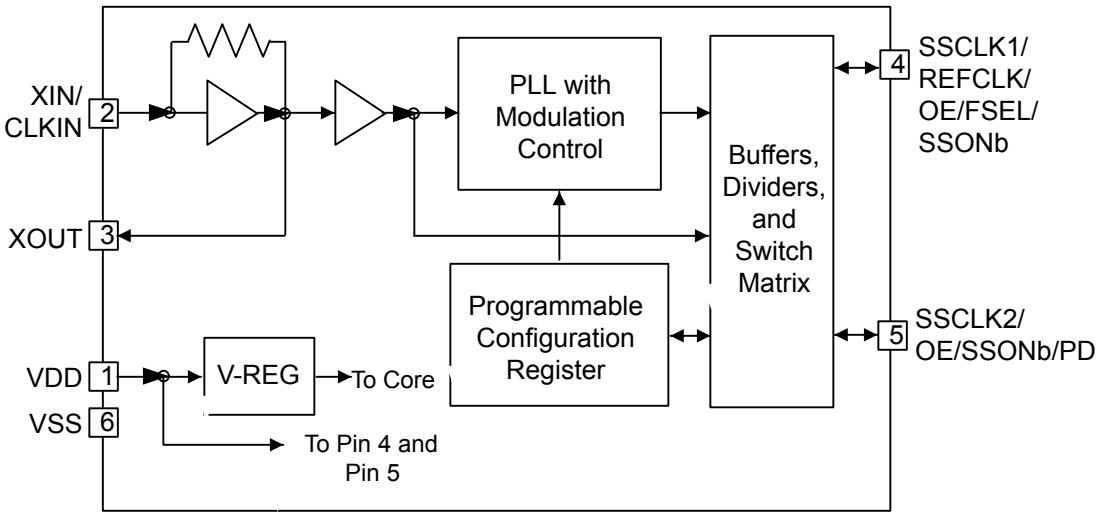
The factory programmable Si51210 is the industry's lowest power, smallest footprint and frequency flexible programmable clock generator targeting low power, low cost and high volume consumer and embedded applications. The device operates from a single crystal or an external clock source and generates 1 to 2 outputs up to 170 MHz. The device is factory programmed to provide customized output frequencies and control input such as frequency select, spread spectrum on, power down and output enable. Center spread spectrum can also be programmed to reduce EMI to meet board level system requirements.

KEY FEATURES

- Generates up to 2 CMOS clock outputs from 3 to 170 MHz
- Accepts crystal or reference clock input
  - 3 to 165 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, SSONb, PD, and OE input functions

Applications

- Crystal/XO replacement
- EMI reduction
- Portable devices
- Digital still camera
- IP phone
- Smart meter



1. Feature List

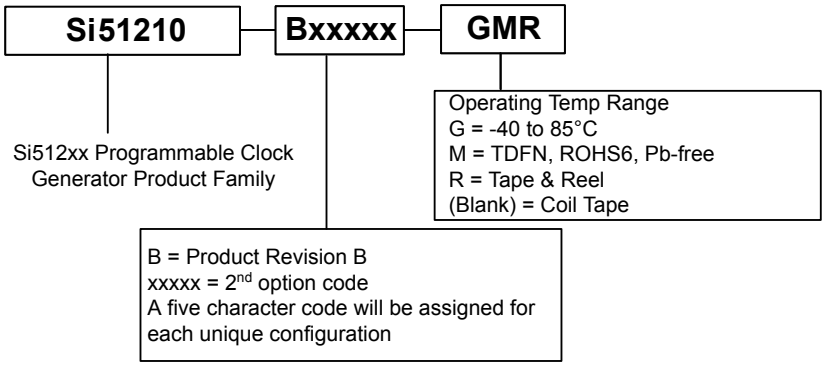
The Si51210 highlighted features are listed below.

- Generates up to 2 CMOS clock outputs from 3 to 170 MHz
- Accepts crystal or reference clock input
  - 3 to 165 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, SSONb, PD, and OE input functions
- Low power dissipation
- 2.5 to 3.3 V voltage supply range
- ±0.25%, ±0.5% or ±1% spread spectrum (center spread)
- Low cycle-cycle jitter
- Ultra small 6-pin TDFN package (1.2 mm x 1.4 mm)

2. Ordering Guide

Table 2.1. Si51210 Ordering Guide

Part Number	Package Type	Temperature
Si51210-Bxxxxx-GM	6-pin TDFN	Industrial, –40 to 85 °C
Si51210-Bxxxxx-GMR	6-pin TDFN—Tape and Reel	Industrial, –40 to 85 °C



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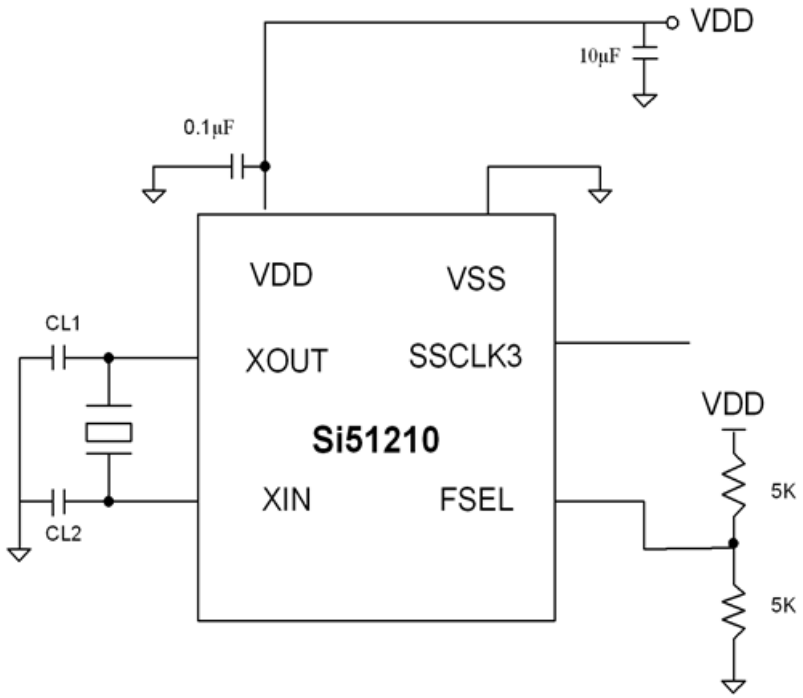
3. Design Considerations

3.1 Typical Application Schematic



3.2 Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1 µF must be used between VDD and VSS on pin 1. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin. In addition, a 10 µF capacitor should be placed between VDD and VSS.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (SSCLK or REFCLK pins) and the load is over 1 ½ inches. The nominal impedance of the SSCLK output is about 30 Ω. Use a 20 Ω resistor in series with the output to terminate a 50 Ω trace impedance and place a 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Only use a parallel resonant fundamental AT cut crystal. Do not use higher overtone crystals. To meet the crystal initial accuracy specification (in ppm) make sure that the external crystal load capacitor is matched to the crystal load specification. To determine the value of CL1 and CL2, use the following formula:

$CL1 = CL2 = 2CL - (Cpin + Cp);$

where CL is the load capacitance stated by the crystal manufacturer,

Cpin is the Si51210 pin capacitance (3 pF), and

Cp is the parasitic capacitance of the PCB traces.

Example: If a crystal with CL = 12 pF specification is used and Cp = 1 pF (parasitic PCB capacitance on PCB), 19 or 20 pF external capacitors from pins XIN (pin 2) and XOUT (Pin 3) to VSS are required. Users must verify Cp value.

Table 3.1. Crystal Specifications

Equivalent Series Resistance (ESR)	Crystal Output Capacitance (CO)	Load Capacitance (CL)
≤ 50 Ω	≤ 3 pF	≤ 13 pF

4. Electrical Specifications

Table 4.1. DC Electrical Specifications

(V_{DD} = 2.5 V ±10%, or V_{DD} = 3.3V ±-10%, C_L = 10 pF, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	V_{DD}= 3.3 V ± 10%	2.97	3.3	3.63	V
		V_{DD}= 2.5 V ± 10%	2.25	2.5	2.75	V
VDD Ramp Time	V_{DD_Ramp}	From 0 V to VDD_{min}	—	—	10	ms
Output High Voltage	V_{OH}	I_{OH}= –4 mA	V_{DD} – 0.5	—	—	V
Output Low Voltage	V_{OL}	I_{OL}= 4 mA	—	—	0.3	V
Input High Voltage	V_{IH}	CMOS Level	0.7 V_{DD}	—	—	V
Input Low Voltage	V_{IL}	CMOS Level	0	—	0.3 V_{DD}	V
Operating Supply Current[1]	I_{DD}	F_{IN} = 12 MHz, SSCLK1 = 12 MHz, SSCLK2 = 24 MHz, C_L= 5 pF, V_{DD} = 3.3 V	—	6.3	10	mA
Power Down Current	IDD_{PD}		—	0.5	0.65	mA
Nominal Output Impedance	Z_O		—	30	—	Ω
Internal Pull-up/Pull-down Resistor	R_{PUP}/R_{PD}	Pin 5	—	150k	—	Ω
Input Pin Capacitance	C_{IN}	Input pin capacitance	—	3	5	pF
Load Capacitance	C_L		—	—	10	pF

Note:

1. I_{DD} depends on input and output frequency configurations.

Table 4.2. AC Electrical Specifications

(V_{DD} = 2.5 V ±10%, or V_{DD} = 3.3 V ±10%, C_L = 10 pF, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	F_{IN1}	Crystal input	8	—	48	MHz
Input Frequency Range	F_{IN2}	Reference clock Input	3	—	165	MHz
Output Frequency Range	F_{OUT}	SSCLK1/2	3	—	170	MHz
Frequency Accuracy	F_{ACC}	Configuration dependent	—	0	—	ppm
Output Duty Cycle	DC_{OUT}	Measured at V_{DDO}/2 $F_{OUT} \leq$ 75 MHz	45	50	55	%
		Measured at V_{DDO}/2 F_{OUT} > 75 MHz	40	50	60	%
Input Duty Cycle	DC_{IN}	CLKIN, CLKOUT through PLL	30	50	70	%
Output Rise/Fall Time	t_r/t_f	C_L= 10 pF, 20 to 80%	—	1	2	ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Period Jitter	PJ_1	SSCLK1/2, at the same frequency	—	12	20	ps rms
	PJ_2	SSCLK1/2, at different output frequencies[1]	—	30	95[2]	ps rms
Cycle-to-Cycle Jitter	CCJ_1	SSCLK1/2, at the same frequency	—	85	150	ps
	CCJ_2	SSCLK1/2, at different output frequencies[1]	—	145	290[2]	ps
Power-up Time	t_{PU}	Time from 0.9 V_{DD} to valid frequencies at all clock outputs	—	1.2	5	ms
Output Enable Time	t_{OE}	Time from OE rising edge to active at outputs SSCLK1/2 (asynchronous), F_{OUT} = 133 MHz	—	—	15	ns
Output Disable Time	t_{OD}	Time from OE falling edge to active at outputs SSCLK1/2 (asynchronous) F_{OUT} = 133 MHz	—	—	15	ns
Spread Spectrum Rate[3]	SS_{DEV}		—	37	—	kHz

Note:

1. Example frequency configurations:
   - 100 MHz, 75 MHz
   - 100 MHz, 66 2/3 MHz
   - 96 MHz, 133 1/3 MHz
2. Jitter performance depends on configuration and programming parameters.
3. The SS modulation rate is a fixed ratio of the reference frequency with values in the range of 30 kHz to 50 kHz based on the frequency plan.

Table 4.3. Absolute Maximum Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	V_{DD}		–0.5	—	4.2	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	V_{DD}+0.5	V
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional, I-Grade	–40	—	85	°C
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22-A114)	–4000	—	4000	V
ESD Protection (Charge Device Model)	ESD_{CDM}	JEDEC (JESD 22-C101)	–1500	—	1500	V
ESD Protection (Machine Model)	ESD_{MM}	JEDEC (JESD 22-A115)	–200	—	200	V

5. Functional Description

5.1 Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 3.0 to 165.0 MHz.

5.2 Input Reference Power On Sequence

An external input clock should not be applied to XIN/CLKIN until VDD is stable. Wait until the voltage is approximately 90% of the final VDD value before enabling an external clock input. A crystal reference, on the other hand, can be applied anytime before or after VDD is stable.

5.3 Output Frequency Range and Outputs

Up to two outputs can be programmed as SSCLK or REFCLK. SSCLK output can be synthesized to any value from 3 to 170 MHz with spread based on valid input frequency. The spread at the SSCLK pins can be enabled or disabled by the SSONb input control pin. If SSONb is used, when this pin is pulled high (V_{DD}), the frequency at SSCLK pin is synthesized to the nominal value of the input frequency without spread. If low (GND), the frequency at SSCLK is synthesized to the nominal value of the input frequency with spread..

REFCLK is the buffered output of the oscillator and is the same frequency as the input frequency without spread. By using only low cost, fundamental mode crystals, the Si51210 can synthesize output frequency up to 170 MHz, eliminating the need for higher order crystals (Xtals) and crystal oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance, and reliability.

5.4 Programmable Spread Percent (%)

The spread percent (%) value is programmable to ±0.25%, ±0.5% or ±1% (center spread) for all SSCLK frequencies.

5.5 SSONb or Frequency Select (FSEL)

The Si51210 pins 4 and 5 can be programmed as SSONb to enable or disable the programmed spread percent value. If SSONb is used, when this pin is pulled high (V_{DD}),the frequency at SSCLK pin is synthesized to the nominal value of the input frequency without spread. If low (GND), the frequency at SSCLK is synthesized to the nominal value of the input frequency with spread. Pin 4 can also be programmed as frequency select (FSEL) function.

If FSEL function is used, the output pin can be programmed for different set of frequencies as selected by FSEL. SSCLK value can be any frequency from 3 to up to 170 MHz, but the spread % is the same percent value. REFCLK is the same frequency as the input reference clock. The set of frequencies in the table below are given as an example, using a 48 MHz crystal.

Table 5.1. Example Frequencies

FSEL Pin 4	SSCLK1 Pin 5
0	66 MHz, ±1%
1	33 MHz, ±1%

5.6 Power Down (PD) or Output Enable (OE)

The Si51210 pin 5 can be programmed as PD input. Pin 4 and pin 5 can be programmed as OE input. PD turns off both PLL and output buffers whereas OE only disables the output buffers to Hi-Z. The OE function is asynchronous. Any requirement for synchronous operations (like glitchless output clock switching) needs to be handled externally.

6. Pin Description

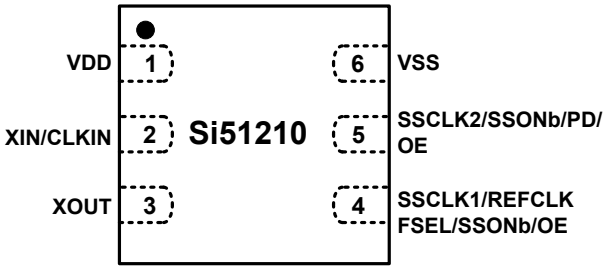


Figure 6.1. 6-Pin TDFN

Table 6.1. Si51210 6-Pin Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	2.5 to 3.3 V power supply.
2	XIN/CLKIN	I	External crystal and clock input.
3	XOUT	O	Crystal output. Leave this pin unconnected (floating) if an external clock input is used.
4	SSCLK1/REFCLK/FSEL/SSONb/OE	I/O	Programmable SSCLK1 or REFCLK output or MultiFunction control input. The frequency at this pin is synthesized by the internal PLL if programmed as SSCLK1 with or without spread. If programmed as REFCLK, the output clock is a buffered output of crystal or reference clock input. If programmed as a MultiFunction control input, it can be OE, FSEL, and SSONb.
5	SSCLK2/OE/SSONb/PD	I/O	Programmable SSCLK2 output or MultiFunction control input. The frequency at this pin is synthesized by the internal PLL if programmed as SSCLK2 with or without spread. SSCLK2 output can also be programmed as a buffered output of crystal or reference clock input divided by N, $2 \leq N \leq 8$. If programmed as a MultiFunction control input, it can be OE, PD, and SSONb. This pin cannot be programmed as FSEL control input.
6	VSS	GND	Ground.

7. Package Outline

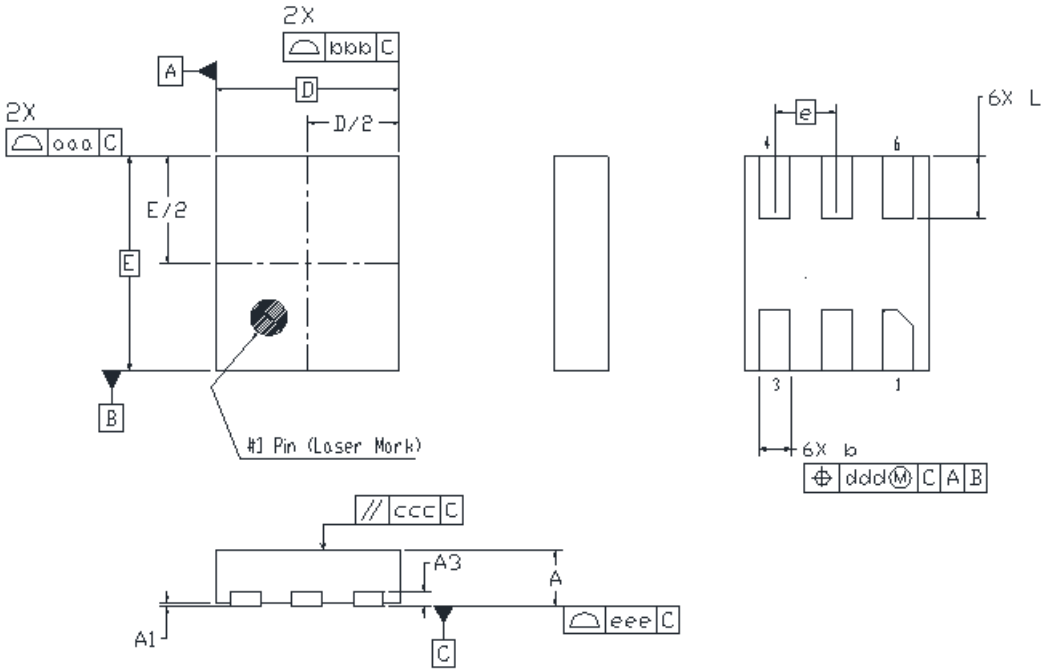


Figure 7.1. 6-pin TDFN

Table 7.1. Si51210 Package Dimensions

Dimension	Min	NOM	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D		1.20 BSC	
e		0.40 BSC	
E		1.40 BSC	
L	0.35	0.40	0.45
aaa		0.05	
bbb		0.05	
ccc		0.10	
ddd		0.07	
eee		0.08	

Dimension	Min	NOM	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the device. The table below lists the values for the dimensions shown in the illustration.

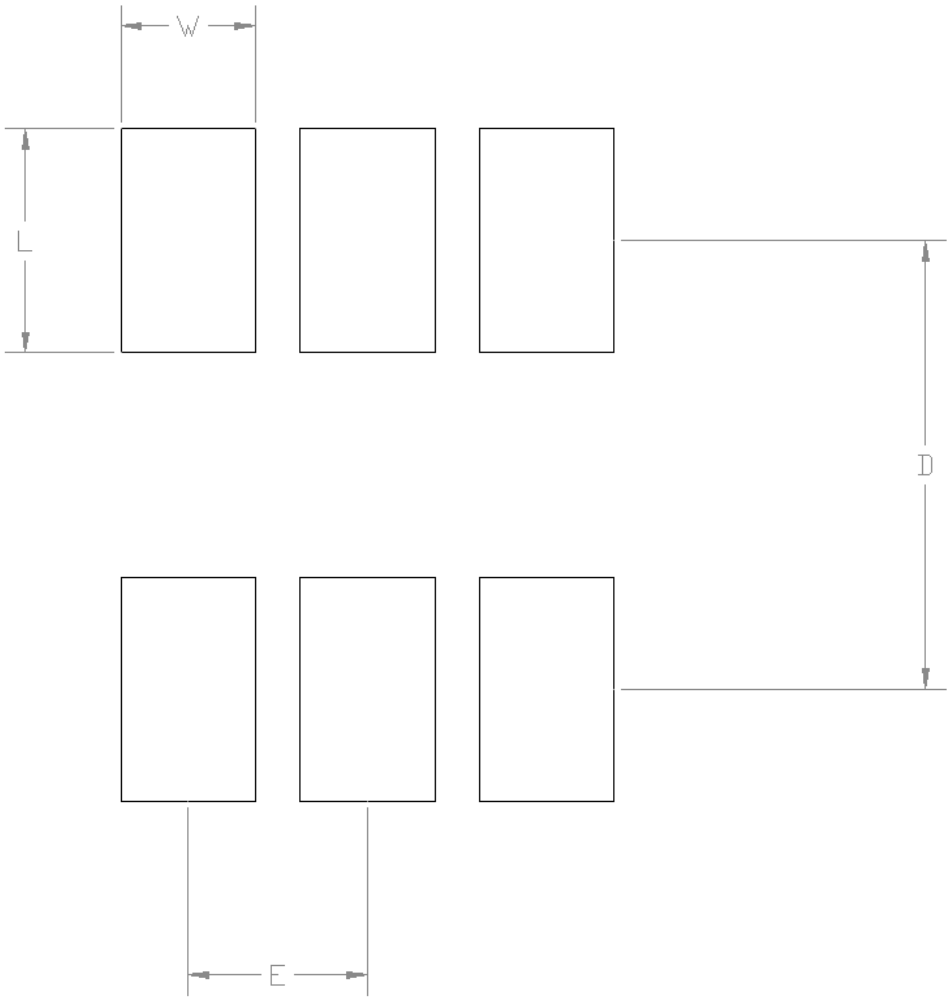


Figure 8.1. Si51210 6-pin TDFN PCB Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
D	1.00
E	0.40
L	0.5
W	0.3

Dimension	mm

Note:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x1 array of 0.55 mm square openings on 0.90 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Revision History

9.1 Revision 1.1

April 2, 2019

- Added VDD Ramp Time to Table 4.1 DC Electrical Specifications on page 6.
- Updated Ordering Guide for Product Revision B.

9.2 Revision 1.0

April 20, 2016

- Updated max output frequency to 170 MHz
- Updated max clock input frequency to 165 MHz
- Updated Operating Temperature to Industrial temperature, –40C to 85 °C
- Updated PD programmable active state
- Removed programmable output rise/fall time, SSEL
- Updated Table 4.1 DC Electrical Specifications on page 6
- Updated Table 4.2 AC Electrical Specifications on page 6
- Updated pin descriptions in Pin Description
- Updated customized part numbering nomenclature in Table 2.1 Si51210 Ordering Guide on page 3
- Added land pattern drawing

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