AK5352

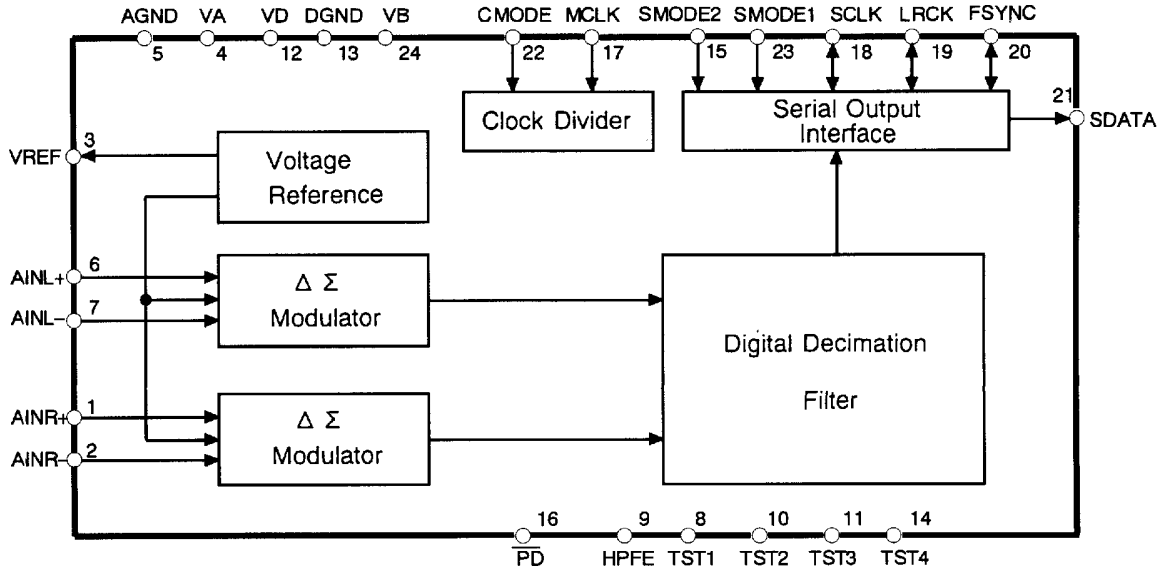
96kHz Sampling ΔΣ 20bit ADC

GENERAL DESCRIPTION

The AK5352 is a 20-bit, 96kHz sampling rate for DAT and DVD, 64x oversampling rate(64fs), 2-channel A/D converter for stereo digital systems. The ΔΣ modulator in the AK5352 uses the new developed Enhanced Dual bit architecture. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as the conventional Single bit way.
The AK5352 is available in a small 24pin VSOP package which will reduce your system space.

FEATURES

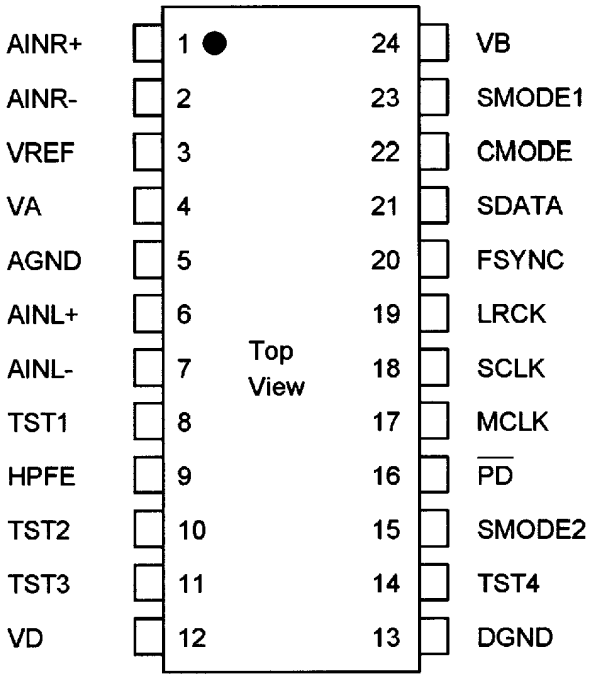
- ☐ Sampling Rate up to 96kHz
- ☐ Full-differential inputs
- ☐ S/(N+D): 97dB
- ☐ DR, S/N: 104dB
- ☐ Linear phase digital filter
  - Pass band: 0 ~ 22kHz(@fs=48kHz)
  - Pass band ripple: ±0.005dB
  - Stop band attenuation: 80dB
- ☐ Digital HPF for DC-offset cancel
- ☐ Master clock: 256fs/384fs
- ☐ Power supply: 5V±5%
- ☐ Small package: 24pinVSOP



■ Ordering Guide

AK5352-VF	-10~70°C	24pin VSOP
AKD5351/2	Evaluation Board	

■ Pin Layout



■ Replacement from AK5350 to AK5352

	AK5350	AK5352
Package	28VSOP	24VSOP *)Interchangeable with AK5352
fc of HPF(@fs=48kHz)	7Hz	1Hz

PIN/FUNCTION

No.	Pin Name	I/O	FUNCTION
1	AINR+	I	Right channel analog positive input pin
2	AINR-	I	Right channel analog negative input pin
3	VREF	O	Voltage Reference output pin (VA-2.6V) Normally connected to VA with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.
4	VA	-	Analog section Analog Power Supply, +5V
5	AGND	-	Analog section Analog Ground
6	AINL+	I	Left channel analog positive input pin
7	AINL-	I	Left channel analog negative input pin
8 10 11 14	TST1 TST2 TST3 TST4		Test pin (Pull-down pin) Should be left floating.
9	HPFE	I	High Pass Filter Enable pin (Pull-up pin) "H": ON "L": OFF
12	VD	-	Digital section Digital Power Supply pin, +5V
13	DGND	-	Digital section Digital Ground pin
16	$\overline{PD}$	I	Power Down pin "L" brings the device into power-down mode. Must be done once after power-on.
17	MCLK	I	Master Clock input pin CMODE="H" : 384fs CMODE="L" : 256fs
18	SCLK	I/O	Serial Data Clock pin Data is clocked out at the falling edge of SCLK. Slave mode: 64fs clock is input usually. Master mode: SCLK outputs a 64fs clock. SCLK stays low during the power-down mode($\overline{PD}$="L").
19	LRCK	I/O	L/R Channel Clock Select pin Slave mode: An fs clock is fed to this LRCK pin. Master mode: LRCK output an fs clock. LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H".
20	FSYNC	I/O	Frame Synchronization Signal pin Slave mode: When "H", data bits are clocked out on SDATA. As I^2S slave mode ignores FSYNC, it should hold "L" or "H". Master mode: FSYNC outputs 2fs clock. Stay low during the power-down mode($\overline{PD}$="L").

21	SDATA	O	Serial Data Output pin Data are output with MSB first, in 2's complement format. After 20 bits are output it turns to "L". It also remains "L" at a power-down mode($\overline{PD}$="L").
22	CMODE	I	Master Clock Selection pin "L": MCLK=256fs "H": MCLK=384fs
23 15	SMODE1 SMODE2	I I	Serial Interface Mode Select pin Defines the directions of LRCK, SCLK and FSYNC pins and Output Data Format. SMODE2 is pull-down pin. SMODE1 SMODE2 MODE LRCK L L Slave mode: MSB justified : H/L H L Master mode: Similar to I^2S : H/L L H Slave mode: I^2S : L/H H H Master mode: I^2S : L/H
24	VB	-	Substrate Power Supply, +5V

ABSOLUTE MAXIMUM RATINGS

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
DC Power Supply:Analog Power(VA pin)	VA	-0.3	6.0	V
Digital Power(VD pin) (Note 2)	VD	-0.3	6.0/VB+0.3	V
Substrate Power(VB pin)	VB	-0.3	6.0	
Input Current (Any pin except supplies)	IIN	-	±10	mA
Analog Input Voltage AINL+,AINL-,AINR+,AINR-pins (Note 2)	VINA	-0.3	6.0/VA+0.3	V
Digital Input Voltage (Note 2)	VIND	-0.3	6.0/VB+0.3	V
Ambient Temperature	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Note 1 : All voltage with respect to ground.

Note 2 : Absolute maximum value is the highest voltage in 6.0V, VA+0.3V and VB+0.3V.

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
DC Power Supplies: Analog Power	VA	4.75	5.0	5.25	V
Digital Power(VD pin)	VD	4.75	5.0	VB	V
Substrate Power(VB pin)(Note 3)	VB	4.75	5.0	5.25	V

Note 1 : All voltages with respect to ground.

Note 3 : The VA and VB are connected together through the chip substrate and have several ohms resistance. VA and VD must be same voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS (fs=48kHz)

(Ta=25°C; VA,VD,VB=5.0V; fs=48kHz; 20bit; Input signal frequency=1kHz,
Measurement Bandwidth=10Hz~20kHz; unless otherwise specified.)

Parameter	min	typ	max	Units
Resolution		20		Bits
Analog Input Characteristics (Analog source impedance: 330Ω)				
S/(N+D) (Note 4)	88	97		dB
Dynamic Range (A-weighted) (Note 5)	98	104		dB
S/N (A-weighted) (Note 6)	98	104		dB
Interchannel Isolation (f=1kHz)	100	120		dB
Interchannel Gain Mismatch		0.1	0.3	dB
Gain drift		±200		ppm/°C
Input Voltage Range	±3.26	±3.47	±3.68	Vp-p
Input Impedance	50	80		kΩ
Power Supplies				
Power Supply Current (Note 7)				
Normal Operation ($\overline{PD}$="H")				
VA+VB		15	25	mA
VD		6	9	mA
Power-Down mode ($\overline{PD}$="L")				
VA+VB		20		uA
VD		10		uA
Power Consumption (Note 7)				
Normal Operation		105	170	mW
Power-Down mode		150		uW
Power Supply Rejection Ratio		50		dB

Note 4 : The ratio of the rms value of the signal to the sum of all other spectral components up to 20kHz except for the signal (included harmonic component, excluded DC component, analog input signal is -0.5dB). Inversed of THD+N.

Note 5 : S/(N+D) with an input signal of 60dB below full-scale.

Note 6 : When using only 20kHzLPF, S/N and DR are 100dB(typ.). When using CCIR-ARM filter, S/N is 100dB(typ.).

Note 7 : Almost no current is supplied from VB pin.

ANALOG CHARACTERISTICS (fs=96kHz)

(Ta=25°C; VA,VD,VB=5.0V; fs=96kHz; 20bit; Input signal frequency=1kHz,
Measurement Bandwidth=10Hz ~ 40kHz; unless otherwise specified.)

Parameter	min	typ	max	Units
Resolution		20		Bits
Analog Input Characteristics (Analog source impedance: 330Ω)				
S/(N+D) (Note 8)	86	96		dB
Dynamic Range (Note 9)(Note 10)	90	99		dB
S/N (Note 10)	90	99		dB
Interchannel Isolation (f=1kHz)	100	120		dB
Interchannel Gain Mismatch		0.1	0.3	dB
Gain drift		±200		ppm/°C
Input Voltage Range	±3.26	±3.47	±3.68	Vp-p
Input Impedance	25	40		kΩ
Power Supplies				
Power Supply Current (Note 11)				
Normal Operation ($\overline{PD}$="H")				
VA+VB		15	25	mA
VD		12	18	mA
Power-Down mode ($\overline{PD}$="L")				
VA+VB		20		uA
VD		10		uA
Power Consumption (Note 11)				
Normal Operation		135	215	mW
Power-Down mode		150		uW
Power Supply Rejection Ratio		50		dB

Note 8 : The ratio of the rms value of the signal to the sum of all other spectral components up to 40kHz except for the signal (included harmonic component, excluded DC component, analog input signal is -0.5dB). Inversed of THD+N.

Note 9 : S/(N+D) with an input signal of 60dB below full-scale.

Note 10 : These value are measured by 40kHz flat, without A-weighted. When using A-weighted, S/N and DR are 104dB(typ.).

Note 11 : Almost no current is supplied from VB pin.

DIGITAL FILTER CHARACTERISTICS

(Ta=25°C; VA,VD,VB=5.0V±5%; fs=48kHz)

Low Pass Filter characteristics	Symbol	min	typ	max	Units
Passband -0.005dB (Note 12)	PB	0		21.5	kHz
-0.02dB				21.768	
-0.06dB				22.0	
Stopband (Note 13)	SB	26.5			kHz
Passband Ripple (Note 14)	PR			±0.005	dB
Stopband Attenuation (Note 13 ,Note 15)	SR	80			dB
Group Delay Distortion	ΔGD			0	us
Group Delay (Note 16)	GD		29.3		1/fs
High Pass Filter characteristics					
Frequency Response -3dB (Note 12)	FR		1.0		Hz
-0.5dB			2.9		Hz
-0.1dB			6.5		Hz

Note 12 : These frequencies scale with the sampling frequency(fs).

Note 13 : Stopband is 26.5kHz to 3.0455MHz at fs=48kHz.

Note 14 : Passband is DC to 21.5kHz at fs=48kHz.

Note 15 : The analog modulator samples the input at 3.072MHz for a system sampling rate of fs=48kHz. These is no rejection of input signals at those bandwidths which are multiples of the sampling frequency (n x 3.072MHz ±22kHz ;n=0,1,2,3···).

Note 16 : The calculation delay time occurred by digital filtering. This is the time from the input of analog signal to setting the 20bit data of both channels to the output registers. GD=29.3/fs.

ELECTRICAL CHARACTERISTICS

■ Digital Characteristics

(Ta=25°C; VA,VD,VB=5.0V±5%)

Parameter	Symbol	min	typ	max	Units
High-Level Input voltage	V_{IH}	70%VD	-	-	V
Low-Level Input voltage	V_{IL}	-	-	30%VD	V
High-Level Output voltage Iout=-20uA	V_{OH}	VD-0.1	-	-	V
Low-Level Output voltage Iout=20uA	V_{OL}	-	-	0.1	V
Input Leakage Current (Note 17)	Iin	-	-	±10	uA

Note 17 : Except for pull-down and pull-up pins. TST1, TST2, TST3, TST4, SMODE2 pins have internal pull-down device, HPFE pin has internal pull-up device. (TYP.50kΩ)

■ **SWITCHING CHARACTERISTICS**

(Ta=25°C; VA,VD,VB=5.0V±5%; C_L=20pF)

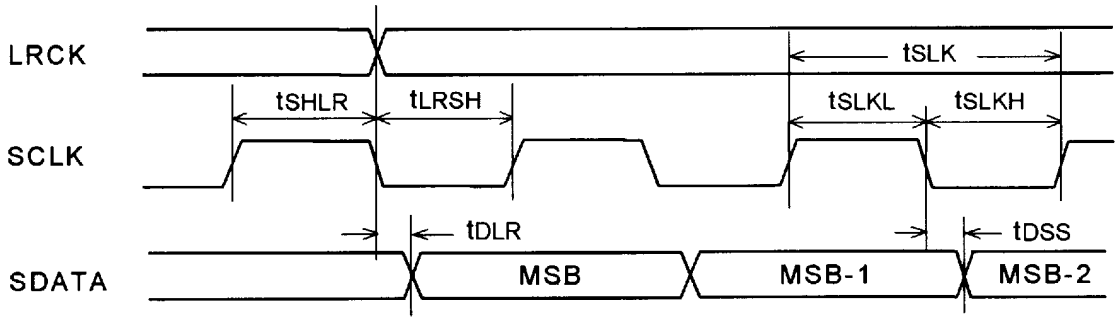
Parameter	Symbol	min	typ	max	Unit
Control Clock Frequency					
Master Clock 256fs: (fs = ~98kHz)	f_{CLK}	4.096	12.288	25.088	MHz
Pulse width Low	t_{CLKL}	15.9			ns
Pulse width High	t_{CLKH}	15.9			ns
384fs: (fs = ~54kHz)	f_{CLK}	6.144	18.432	20.736	MHz
Pulse width Low	t_{CLKL}	20.83			ns
Pulse width High	t_{CLKH}	20.83			ns
Serial Data Output Clock	f_{SLK}		3.072	6.144	MHz
Channel Select Clock(Sampling Frequency)	f_s	16	48	98	kHz
Duty Cycle		25		75	%
Serial Interface Timing (Note 18)					
Slave Mode(SMODE1="L")					
SCLK Period	t_{SLK}	159.4			ns
SCLK Pulse width Low	t_{SLKL}	65			ns
Pulse width High	t_{SLKH}	65			ns
SCLK Rising to LRCK Edge (Note 19)	t_{SLR}	30			ns
LRCK Edge to SCLK Rising (Note 19)	t_{LRS}	30			ns
LRCK Edge to SDATA MSB Valid	t_{DLR}			50	ns
SCLK Falling to SDATA Valid	t_{DSS}			50	ns
SCLK Rising to FSYNC Edge (Note 19)	t_{SF}	30			ns
FSYNC Edge to SCLK Rising (Note 19)	t_{FS}	30			ns
Master Mode(SMODE1="H")					
SCLK Frequency	f_{SLK}		64fs		Hz
Duty Cycle			50		%
FSYNC Frequency	f_{FSYNC}		2fs		Hz
Duty Cycle			50		%
SCLK Falling to LRCK Edge	t_{SLR}	-20		20	ns
LRCK Edge to FSYNC Rising	t_{LRF}		1		tslk
SCLK Falling to SDATA Valid	t_{DSS}			50	ns
SCLK Falling to FSYNC Edge	t_{SF}	-20		20	ns
Power down timing					
$\overline{PD}$ Pulse width	t_{PDW}	150			ns
$\overline{PD}$ Rising to SDATA Valid (Note 20)	t_{PDV}		516		1/fs

Note 18 : Refer to Serial Data Interface.

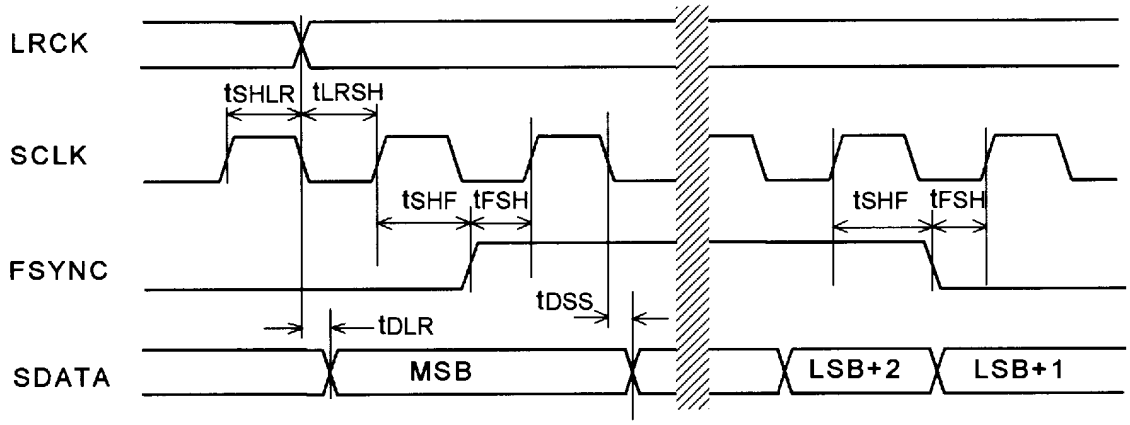
Note 19 : Specified LRCK and FSYNC edges not to coincide with the rising edges of SCLK.

Note 20 : The number of LRCK rising edges after $\overline{PD}$ brought high. The value is in master mode. In slave mode it becomes one LRCK clock(1/fs) longer.

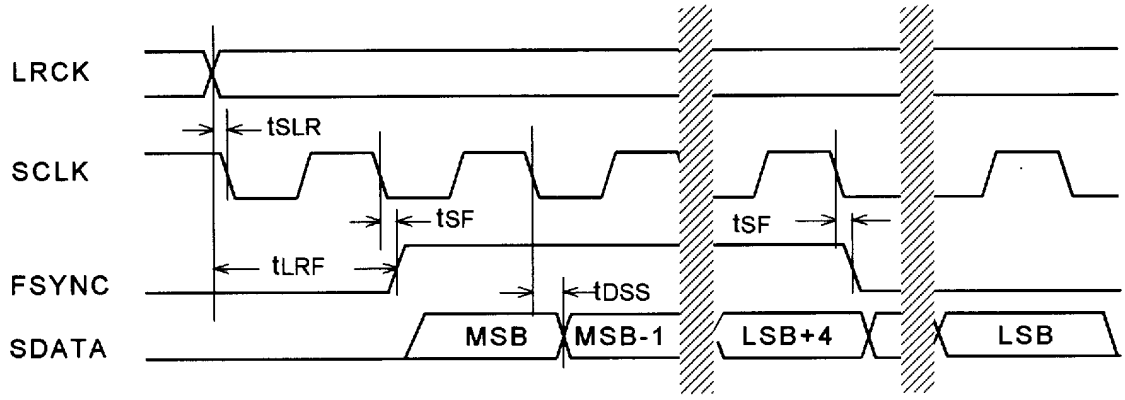
■ **Timing Chart**



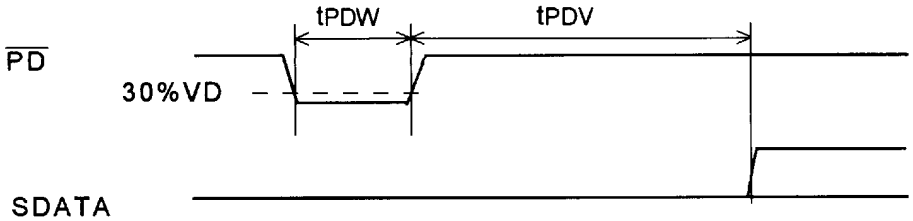
SERIAL DATA TIMING (SLAVE MODE, FSYNC = "H")



SERIAL DATA TIMING (SLAVE MODE)



SERIAL DATA TIMING (MASTER MODE)



POWER DOWN TIMING

OPERATION OVERVIEW

■ System clock

In slave mode, MCLK(256fs/384fs), LRCK(fs) and SCLK(64fs) are required for AK5352. Use a signal divided from the MCLK for LRCK. In master mode, only MCLK is needed. A LRCK clock rate meets standard audio rates (32kHz, 44.1kHz, 48kHz, 96kHz). MCLK=384fs does not correspond to 96kHz sampling. In slave mode, the MCLK should be synchronized with LRCK but the phase is free of care.

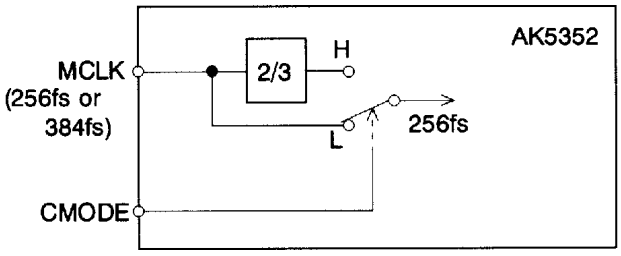
The AK5352 includes the phase detect circuit for LRCK clock, the AK5352 is reset automatically when the synchronization is out of phase by changing the clock frequencies. (Please refer to the "Asynchronization - reset.") When changing sampling frequency(fs) after power-up, AK5352 should be reset.

During the operation ($\overline{PD}$="H") following external clocks should never be stopped : CLK in master mode and MCLK, SCLK and LRCK in slave mode. When the clocks stop there is a possibility that the device comes into a malfunction because of over currents in the dynamic logic. If the external clocks are not present, the AK5352 should be in the power-down mode. ($\overline{PD}$="L")

fs	Master Clock (MCLK)		SCLK(64fs)
	256fs	384fs	
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz
96.0kHz	24.5760MHz	N/A	6.1440MHz

Table 1 . System Clock

■ Clock Circuit



CMODE	MCLK
L	256fs
H	384fs

AK5352 has an internal divider as shown in the above figure. The device can interface either or an external MCLK(256fs or 384fs) by controlling CMODE pin.

■ **Serial Data Interface**

Audio Serial Interface has four kinds of mode, it can be changed by SMODE1 and SMODE2 pins. Data format is MSB first, 2's complement.

Figure	SMODE1	SMODE2	Mode	L/R polarity
Figure 1	L	L	Slave Mode: 20bit, MSB justified	Lch=H, Rch=L
Figure 2	H	L	Master Mode: Similar to I^2S	Lch=H, Rch=L
Figure 3	L	H	Slave Mode: I^2S	Lch=L, Rch=H
Figure 4	H	H	Master Mode: I^2S	Lch=L, Rch=H

Table 2 . Serial Interface

1) SLAVE mode

An output channel is defined by LRCK. Both channel data are output in sequence, in order of the Lch first then Rch at the rate of fs. Data bits are clocked out via the SDATA pin at SCLK rate. Figure 1 and Figure 3 shows data output timing at SCLK=64fs. FSYNC enables SCLK to start clocking out data. The MSB is clocked out by the LRCK edge. SCLK causes the ADC to output succeeding bits when FSYNC is high. However, as I^2S slave mode ignores FSYNC, it should hold "L" or "H".

2) MASTER mode

In MASTER mode, the A/D converter is driven from a master clock(MCLK:256fs/384fs) and outputs all other clocks(LRCK, SCLK). The falling edge of SCLK causes the ADC to output each bit. Figure 2 and Figure 4 shows the output timing. 2x fs clock of 50% duty is output via the FSYNC pin. FSYNC rises one SCLK cycle after the transition of LRCK edges and stays high during 16 serial clocks(16*t_{SLK}). Upper 16 bit data is output during FSYNC "H", lower 4 bit is output after FSYNC "L" transition.

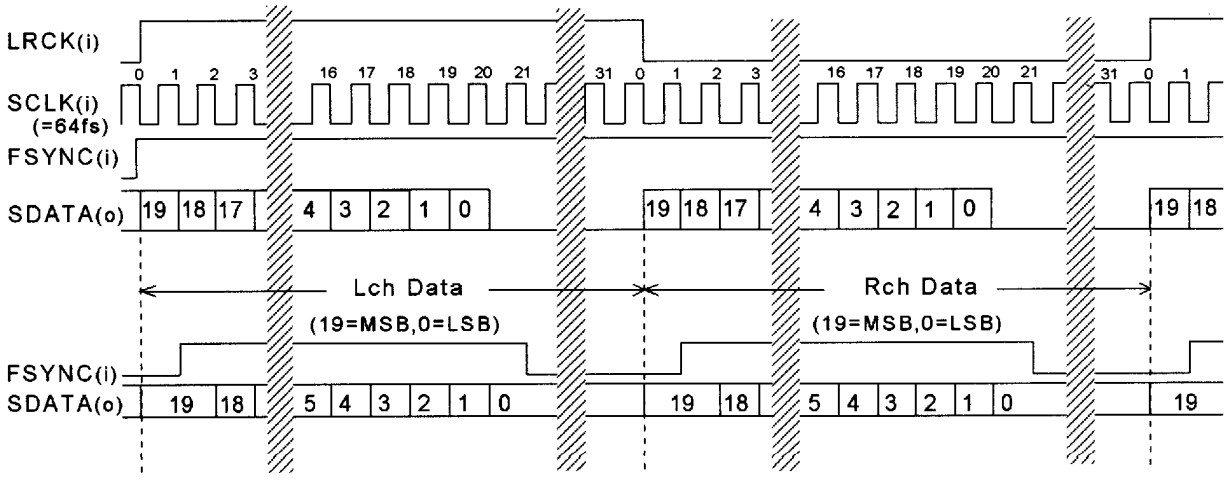


Figure 1 . Data Output Timing (Slave mode)

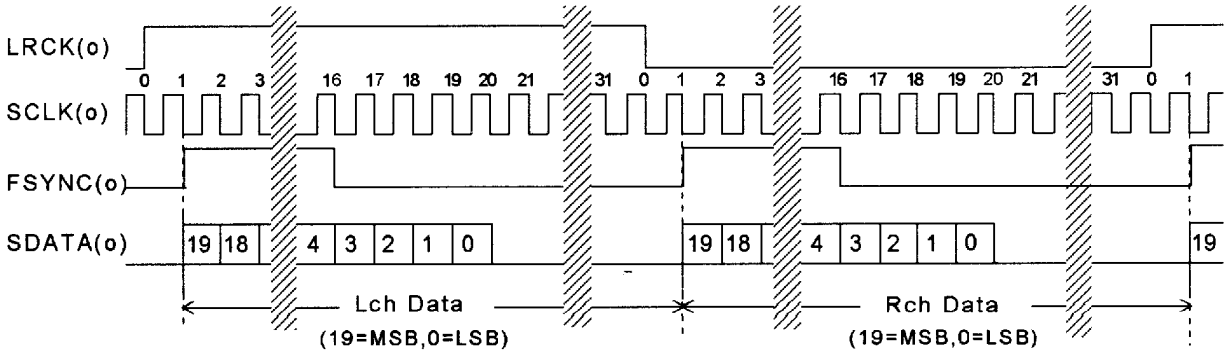


Figure 2. Data Output Timing(Master mode)

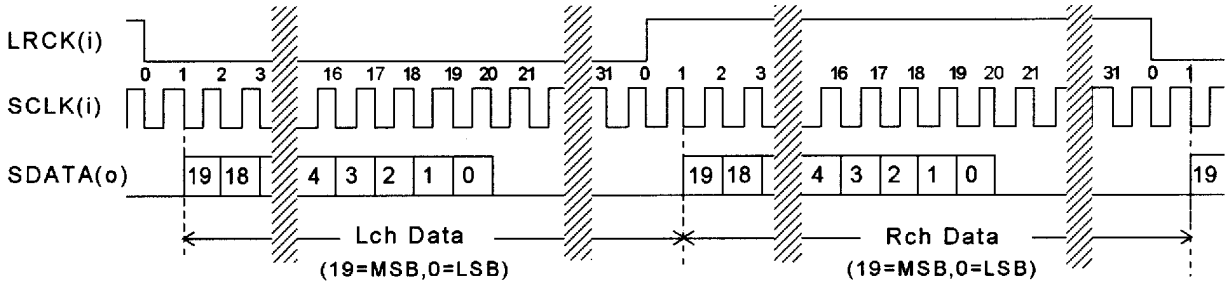


Figure 3. Data Output Timing(I ^{2} S Slave mode)

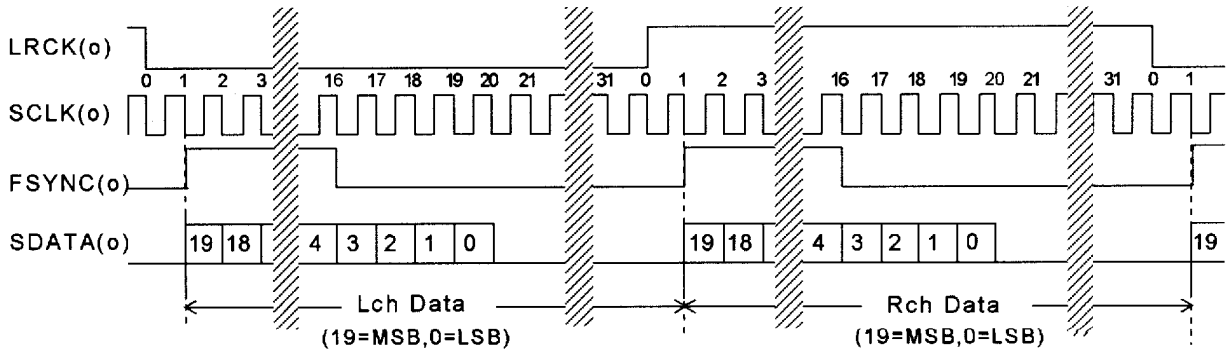


Figure 4. Data Output Timing (I ^{2} S Master mode)

■ **Power-down mode**

The AK5352 has to be reset once by bringing $\overline{PD}$ "L" upon power-up. All internal registers of the digital filter and so on in the AK5352 are reset by this operation. When exiting the power-down mode($\overline{PD}$="H"), the internal timing starts clocking by first MCLK "↑"(rising edge). In master mode internal counter starts at once, in slave mode internal counter starts after synchronizing with the first rising edge of LRCK. The serial output data is available after 516 counting clock of LRCK cycle.

■ **Asynchronization-reset**

In slave mode, if the phase difference between LRCK and internal control signals is larger than +1/16 ~ -1/16 of word period(1/fs), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK.

■ **High Pass Filter(HPFE pin)**

The AK5352 has a Digital High Pass Filter(HPF) for DC-offset cancel. When HPFE pin goes "H", HPF is enabled. The cut-off frequency of the HPF is 1Hz(@fs=48kHz). It also scales with the sampling frequency(fs). The HPF can be disabled by bringing HPFE pin "L". In this case, the AK5352 has the DC-offset of a few mV.

SYSTEM DESIGN

Figure 5 shows the system connection diagram. Figure 6 shows the input buffer circuit. An evaluation board[AKD5351/2] is available which demonstrates the optimum layout, power supply arrangement and measurement results.

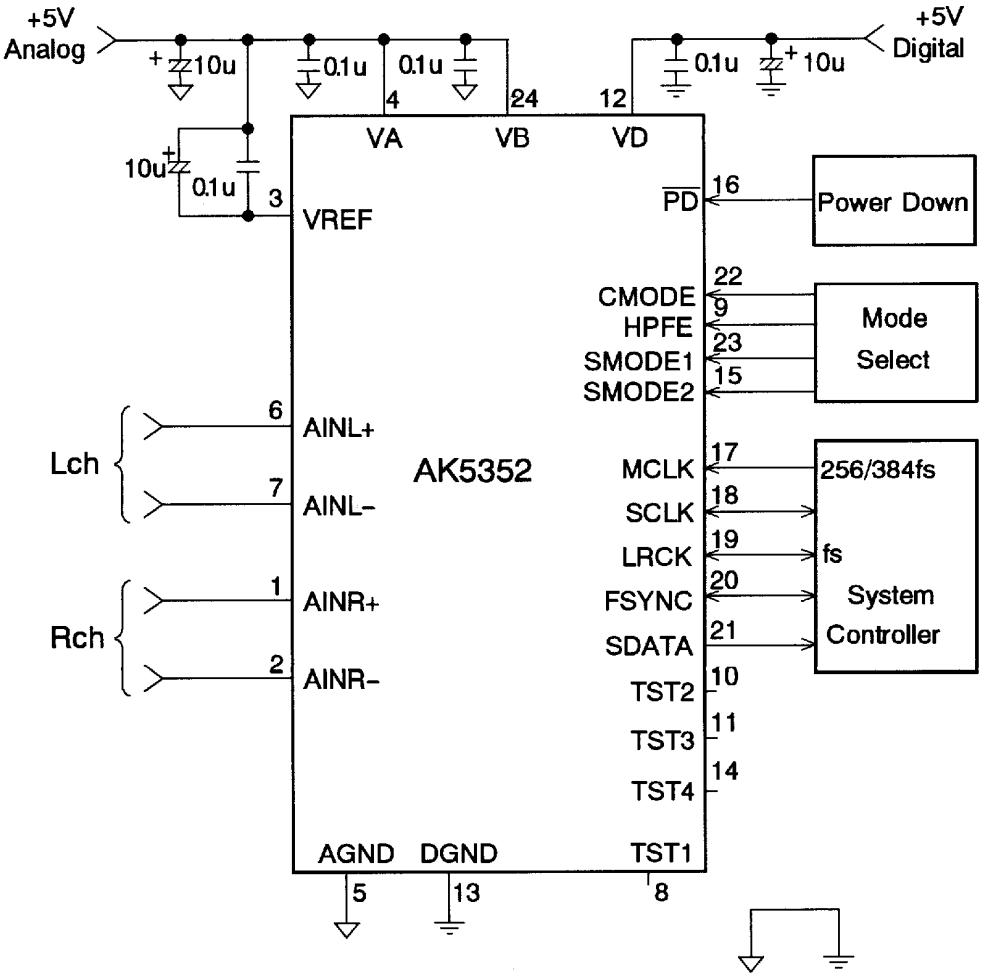


Figure 5 . System Connection Diagram Example

NOTE: +5V Analog should be powered the same time or earlier than +5V Digital.

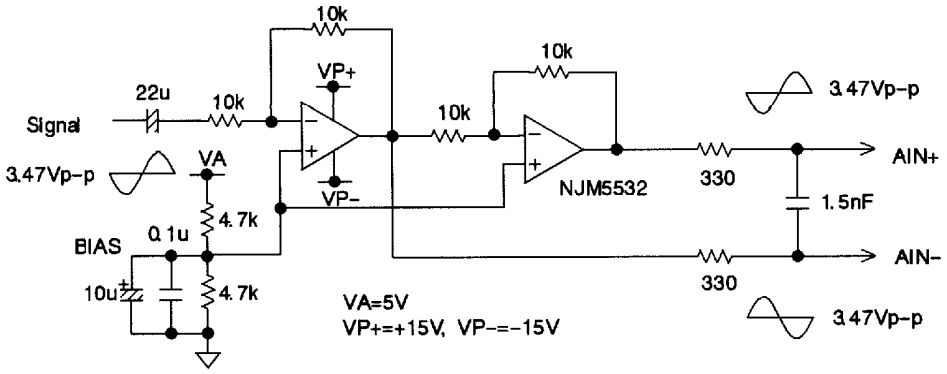


Figure 6 . Input Buffer Circuit Example

■ **Grounding and Power Supply Decoupling**

The AK5352 requires careful attention to power supply and grounding arrangements. The VA and VB are connected together through the chip substrate and have several ohm resistance. The power to VB should come up at the same time or faster than the power to VD, when they are fed separately to the device (Figure 5). As to the connections of decoupling capacitors, refer to Figure 5 . The 0.1uF of decoupling capacitors connected power supply pins should be as near as possible to the power supply pin.
As AINL± pins is near VD pin, ground pattern should be inserted between VD line and AINL±lines to avoid digital noise coupling. Refer to evaluation board manual of AKD5352/1 Rev.B about board layout.

■ **Analog connections**

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is ±3.47Vp-p on its reference voltage(VREF). In case that the positive input is more than its full-scale, the AK5352 outputs positive 7FFFFH(Hex, Full-scale). In case that the negative input is more than its full-scale, the AK5352 outputs negative 80000H(Hex, Full- scale). In case of an ideal value of no input, outputs 00000H(@20bit). DC offset is removed by internal HPF.

AK5352 samples the analog inputs at 3.072MHz with fs=48kHz. The digital filter rejects all noise between 26.5kHz and 3.0455MHz. However, the filter will not reject frequencies right around 3.072MHz (and multiples of 3.072MHz). Most audio signals do not have significant noise energy at 3.072MHz. Hence, a simple RC filter is sufficient to attenuate any noise energy at 3.072MHz.

The reference voltage for A/D converter is supplied from the VREF pin at VA reference. In order to eliminate the effects of high frequency noise on the VREF pin, a 10uF or less electrolytic capacitor and a 0.1uF ceramic capacitor should be connected parallel between the VREF and the VA pins. No current should be driven from the VREF pin.

The AK5352 accepts +5V supply voltage. Any voltage which exceeds the upper limit of (VA+)+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AINL±, AINR±) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits.
Use caution specially in case of using ±15V in surrounding analog circuit.

■ **Digital Connections**

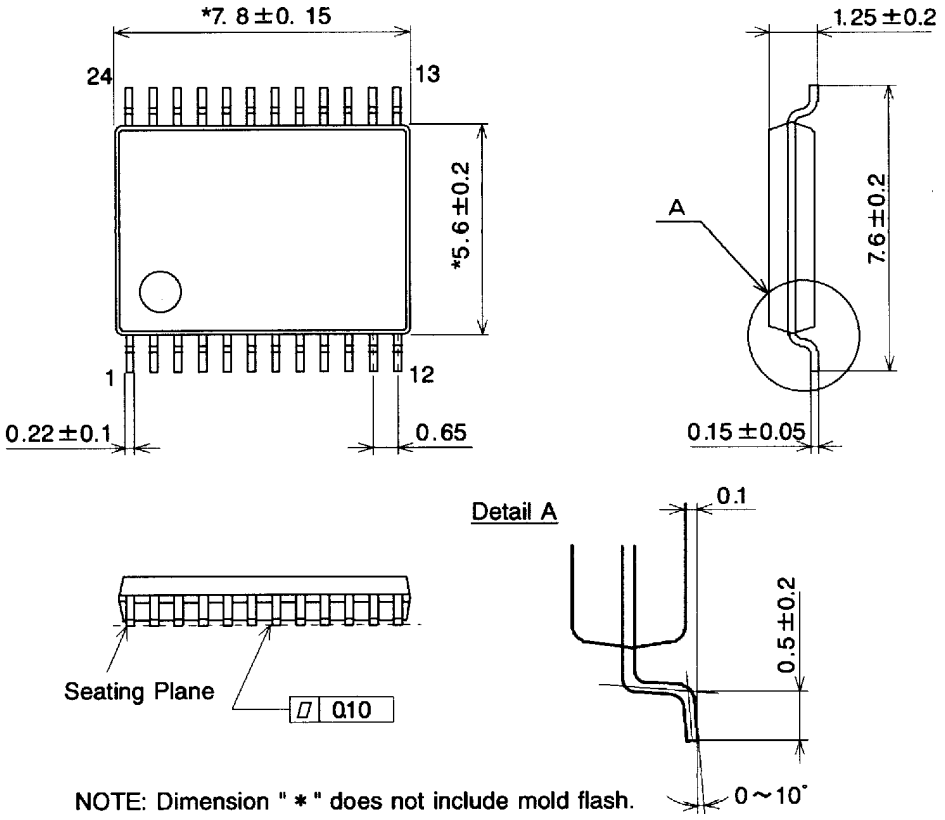
To minimize digital originated noise, connect the ADC digital outputs only to CMOS inputs. Logic families of 4000B, 74HC, 74AC, 74ACT and 74HCT series are suitable.

■ **Multiple AK5352**

In systems where multiple ADC's are required, care must be taken to insure the internal clocks are synchronized between converters to make simultaneous sampling. In slave mode, synchronous sampling is achieved by supplying the same MCLK and LRCK to all converters. In master mode, the same $\overline{PD}$ signal is supplied to each ADC. The $\overline{PD}$ state is released at the first rising edge of MCLK after bringing $\overline{PD}$ into high. Hence, if the rising edge of $\overline{PD}$ and rising edge of MCLK coincides together the sampling difference among the ADC's modulator would occur. The difference could be 1/256fs in the sampling clock(64fs) of the modulator, typically 81ns at fs=48kHz.

PACKAGE

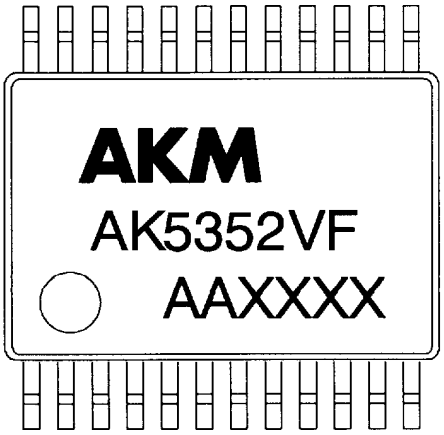
● **24pin VSOP (Unit: mm)**



■ **Material & Lead finish**

Package:	Epoxy
Lead-frame:	Copper
Lead-finish:	Soldering plate

MARKING



Contents of AAXXXX

AA: Lot#

XXXX: Date Code

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