

# Silicon Carbide (SiC) MOSFET – EliteSiC, 80 mohm, 1200 V, M1, D2PAK-7L

## NTBG080N120SC1

### Features

- Typ.  $R_{DS(on)} = 80\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_{G(tot)} = 56\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss} = 79\text{ pF}$ )
- 100% Avalanche Tested
- $T_J = 175^\circ\text{C}$
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb-Free 2LI (on second level interconnection)

### Typical Applications

- UPS
- DC-DC Converter
- Boost Inverter

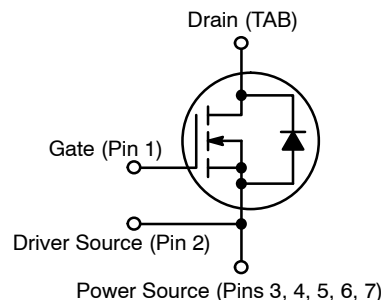
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	1200	V	
Gate-to-Source Voltage		$V_{GS}$	-15/+25	V	
Recommended Operation Values of Gate-Source Voltage		$T_C < 175^\circ\text{C}$ $V_{GSop}$	-5/+20	V	
Continuous Drain Current (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	30	A
			$P_D$	179	W
Power Dissipation (Note 1)	Steady State	$T_C = 100^\circ\text{C}$	$I_D$	21	A
			$P_D$	89	W
Pulsed Drain Current (Note 2)		$T_C = 25^\circ\text{C}$	$I_{DM}$	110	A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	18	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 18.5\text{ A}_{pk}$ , $L = 1\text{ mH}$ ) (Note 3)		$E_{AS}$	171	mJ	
Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		$T_L$	300	$^\circ\text{C}$	

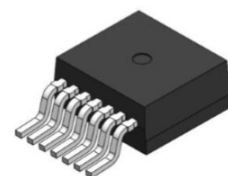
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Repetitive rating, limited by max junction temperature.
3.  $E_{AS}$  of 171 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1\text{ mH}$ ,  $I_{AS} = 18.5\text{ A}$ ,  $V_{DD} = 120\text{ V}$ ,  $V_{GS} = 18\text{ V}$ .

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
1200 V	110 m $\Omega$ @ 20 V	30 A

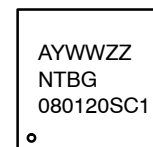


N-CHANNEL MOSFET



D2PAK-7L  
CASE 418BJ

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Lot Traceability
- NTBG080120SC1 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTBG080N120SC1	D2PAK-7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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**Table 1. THERMAL CHARACTERISTICS**

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-to-Case (Note 1)	$R_{\theta JC}$	0.84	°C/W
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	40	°C/W

**Table 2. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}$ , refer to $25^\circ\text{C}$		0.5		V/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	$T_J = 25^\circ\text{C}$		100	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$		1	mA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +25/-15\text{ V}, V_{DS} = 0\text{ V}$			$\pm 1$	$\mu\text{A}$

**ON CHARACTERISTICS** (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 5\text{ mA}$	1.8	3	4.3	V
Recommended Gate Voltage	$V_{GOP}$		-5		+20	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 25^\circ\text{C}$ $V_{GS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 150^\circ\text{C}$		80	110	m $\Omega$
				121		m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 20\text{ V}, I_D = 20\text{ A}$		11		S

**CHARGES, CAPACITANCES & GATE RESISTANCE**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 800\text{ V}$		1154		pF
Output Capacitance	$C_{OSS}$			79		
Reverse Transfer Capacitance	$C_{RSS}$			7.9		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 600\text{ V}, I_D = 20\text{ A}$		56		nC
Threshold Gate Charge	$Q_{G(TH)}$			10		
Gate-to-Source Charge	$Q_{GS}$			18		
Gate-to-Drain Charge	$Q_{GD}$			11		
Gate-Resistance	$R_G$	$f = 1\text{ MHz}$		1.2		$\Omega$

**SWITCHING CHARACTERISTICS**

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 800\text{ V}, I_D = 20\text{ A}, R_G = 4.7\text{ }\Omega$ , Inductive Load		12	22	ns
Rise Time	$t_r$			12	22	
Turn-Off Delay Time	$t_{d(OFF)}$			21	34	
Fall Time	$t_f$			9	18	
Turn-On Switching Loss	$E_{ON}$			135		$\mu\text{J}$
Turn-Off Switching Loss	$E_{OFF}$			46		
Total Switching Loss	$E_{TOT}$			181		

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Continuous Drain-Source Diode Forward Current	$I_{SD}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$			18	A
Pulsed Drain-Source Diode Forward Current (Note 2)	$I_{SDM}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$			110	A
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 10\text{ A}, T_J = 25^\circ\text{C}$		3.9		V

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**Table 2. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -5/20\text{ V}$ , $I_{SD} = 20\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$		16.2		ns
Reverse Recovery Charge	$Q_{RR}$			61.6		nC
Reverse Recovery Energy	$E_{REC}$			4.1		$\mu\text{J}$
Peak Reverse Recovery Current	$I_{RRM}$			7.6		A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

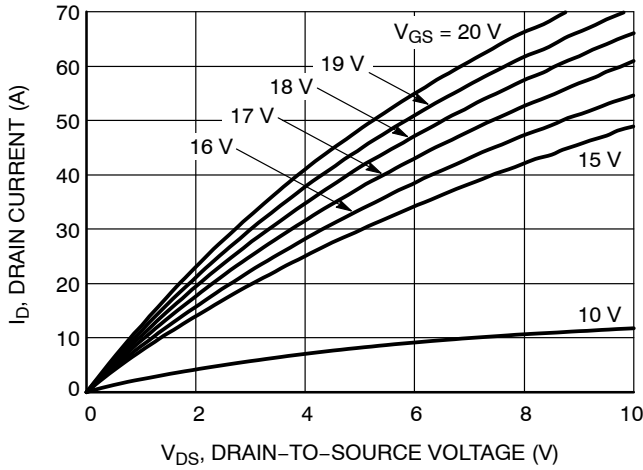


Figure 1. On-Region Characteristics

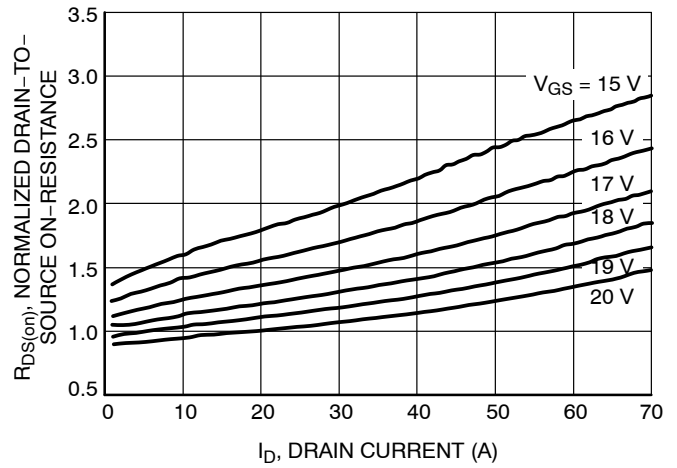


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

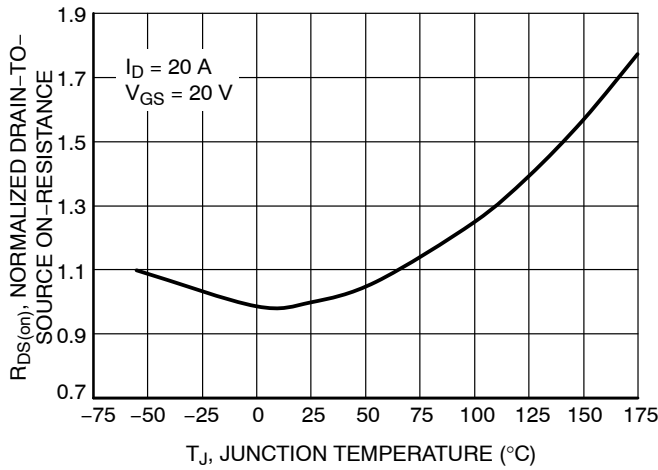


Figure 3. On-Resistance Variation with Temperature

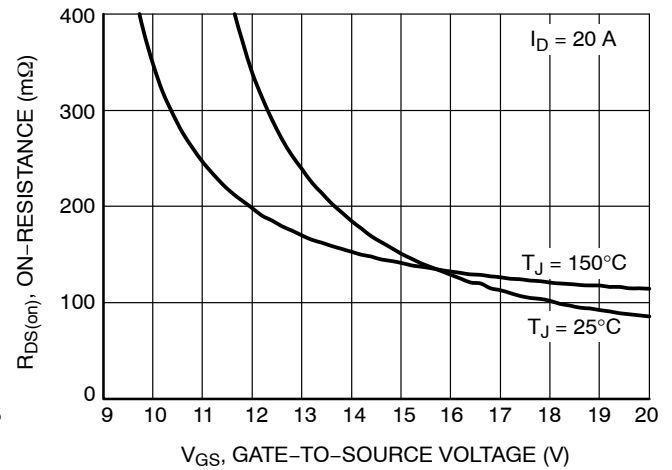


Figure 4. On-Resistance vs. Gate-to-Source Voltage

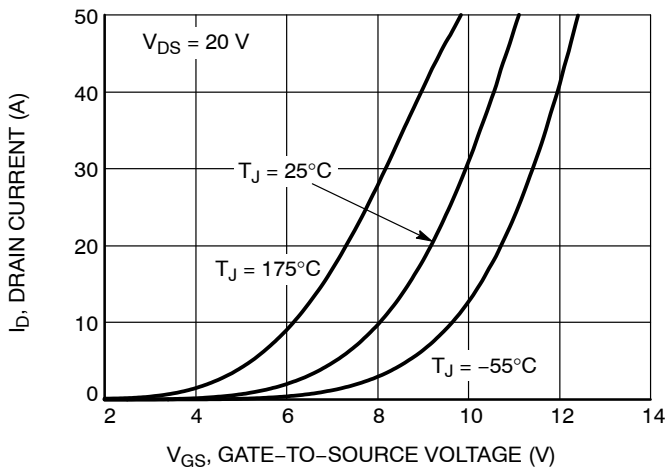


Figure 5. Transfer Characteristics

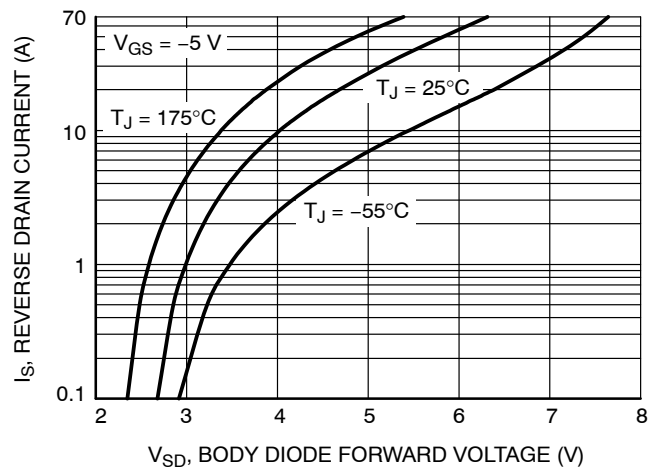
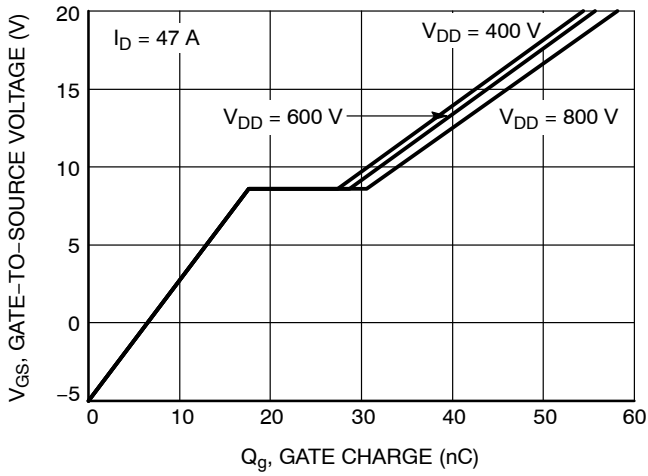


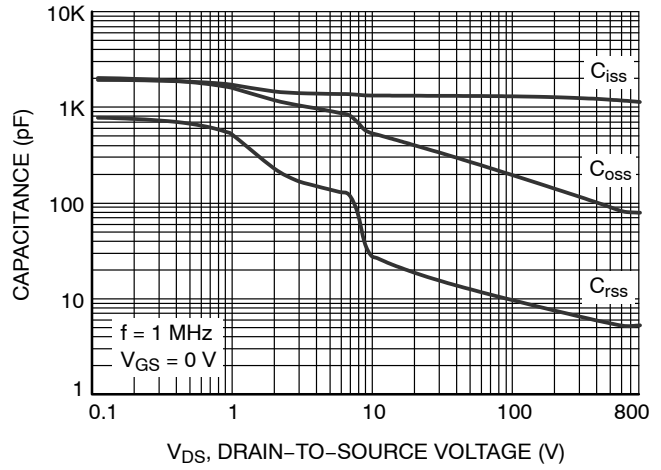
Figure 6. Diode Forward Voltage vs. Current

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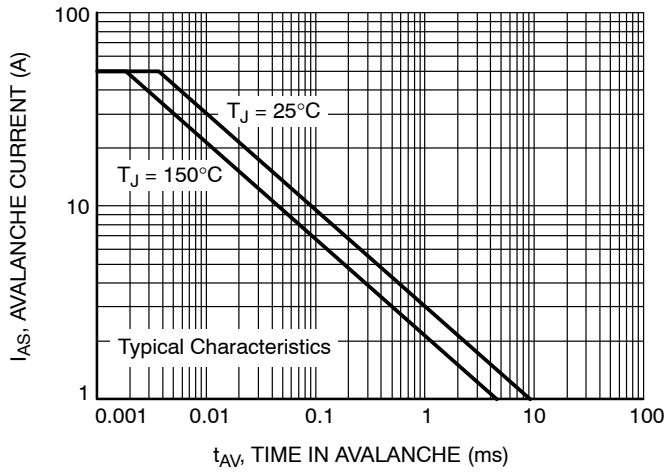
## TYPICAL CHARACTERISTICS (continued)



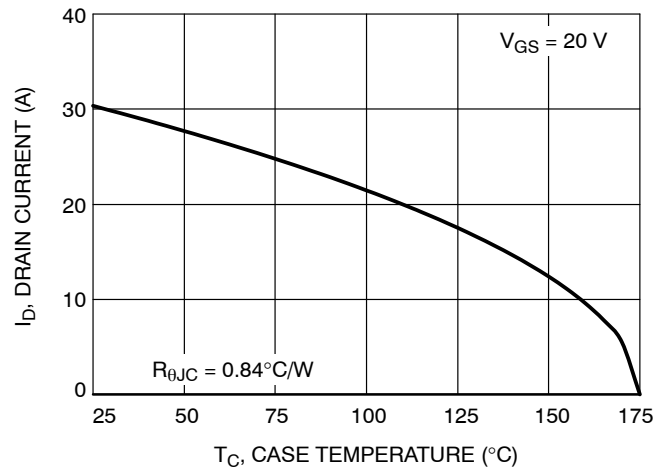
**Figure 7. Gate-to-Source Voltage vs. Total Charge**



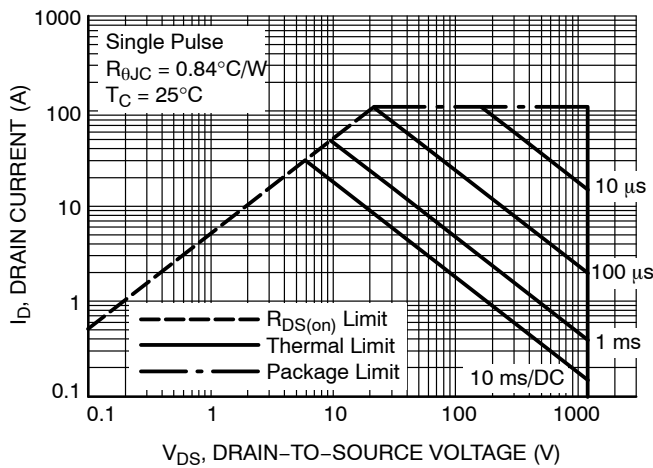
**Figure 8. Capacitance vs. Drain-to-Source Voltage**



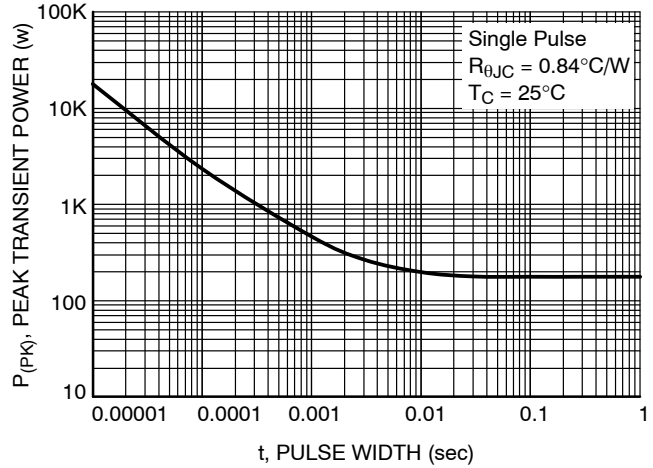
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11. Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

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## TYPICAL CHARACTERISTICS (continued)

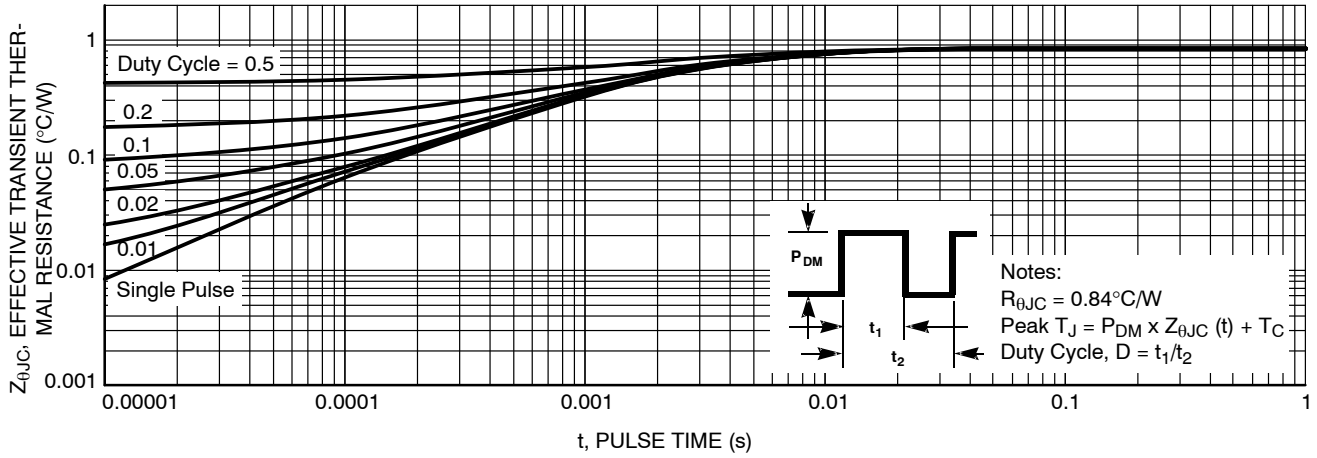
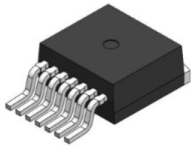


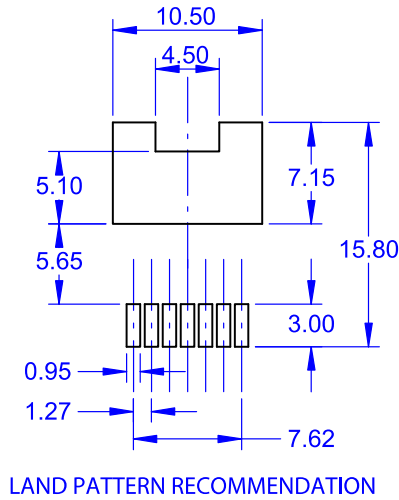
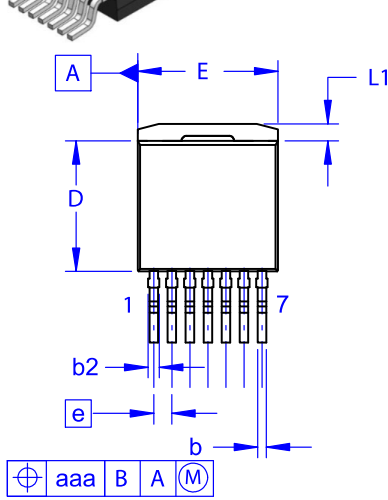
Figure 13. Junction-to-Case Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## D<sup>2</sup>PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

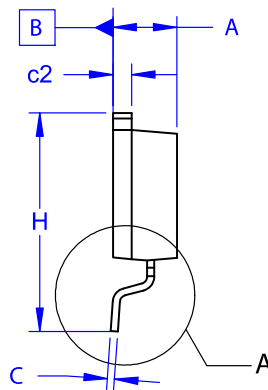
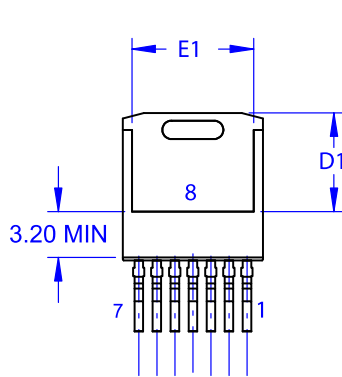
DATE 16 AUG 2019



NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

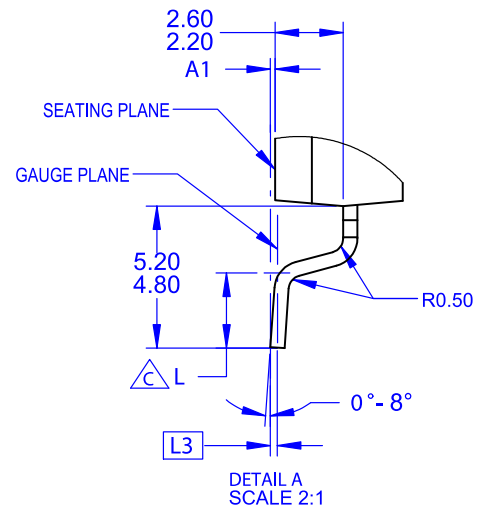


### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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