Freescale Semiconductor
Product Brief

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MPC5602D Microcontroller Product Brief

1 Introduction

1.1 Document overview

This document provides an overview and describes the features of the MPC5601D/2D series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. For electrical specifications, pin assignments, and package diagrams, refer to the device data sheet.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the

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Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations (refer to Section 5, "Developer environment for more information).

The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

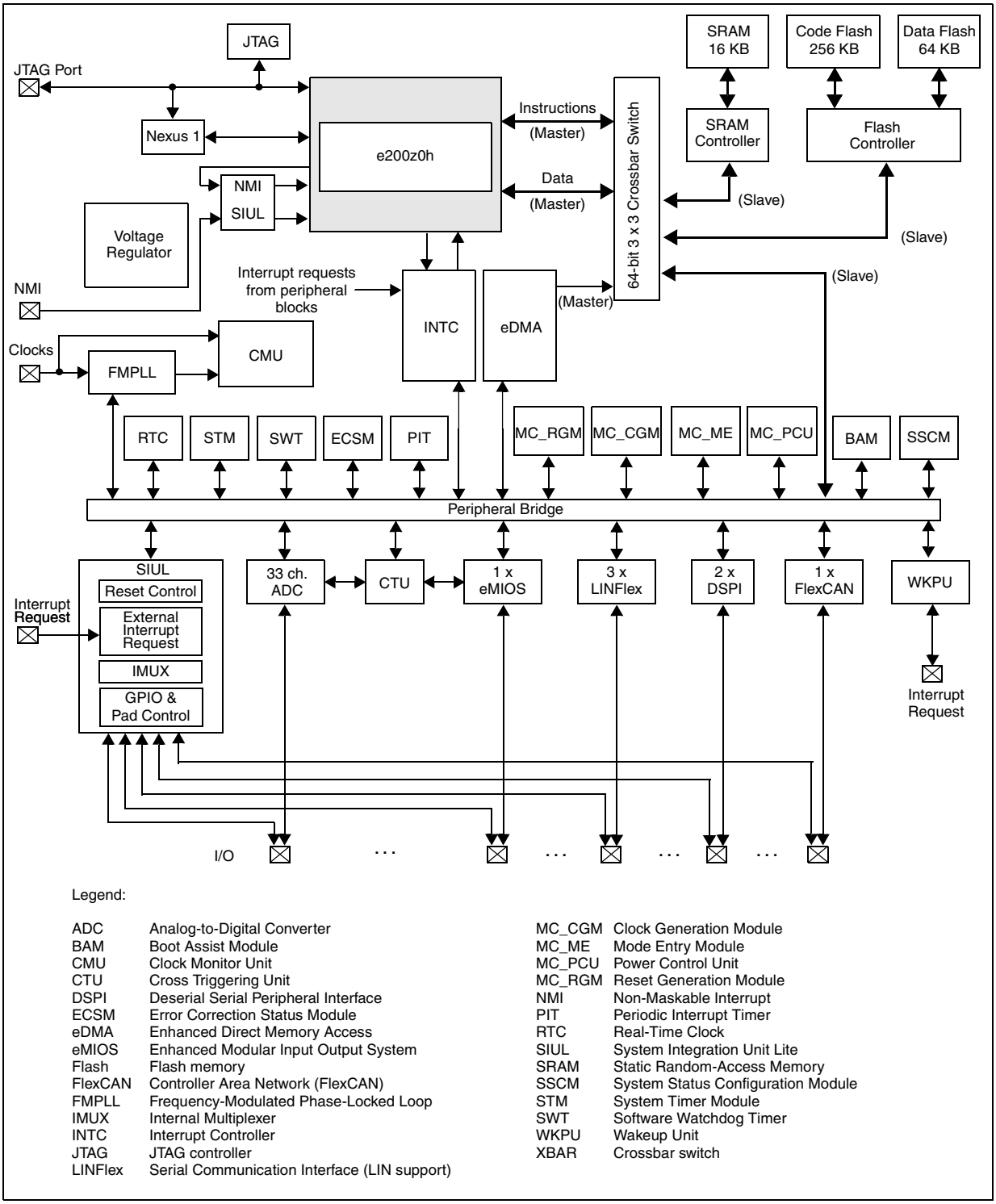
1.3 MPC5602D features

- Single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with the Power Architecture® embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 256 KB on-chip Code Flash supported with Flash controller and ECC
- 64 KB on-chip Data Flash with ECC
- Up to 16 KB on-chip SRAM with ECC
- Interrupt controller (INTC) with multiple interrupt vectors, including 20 external interrupt sources and 18 external interrupt/wakeup sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, Flash, or SRAM from multiple bus masters
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- Up to 33 channel 12-bit analog-to-digital converter (ADC)
- 2 serial peripheral interface (DSPI) modules
- 3 serial communication interface (LINFlex) modules
  - LINFlex 1 and 2: Master capable
  - LINFlex 0: Master capable and slave capable; connected to eDMA
- 1 enhanced full CAN (FlexCAN) module with configurable buffers
- Up to 79 configurable general purpose pins supporting input and output operations (package dependent)
- Real Time Counter (RTC) with clock source from 128 kHz or 16 MHz internal RC oscillator supporting autonomous wakeup with 1 ms resolution with max timeout of 2 seconds
- Up to 4 periodic interrupt timers (PIT) with 32-bit counter resolution

- 1 System Timer Module (STM)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class 1 standard
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602D family. Table 1 provides further details on the block functions.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
ECSM	Error Correction Status Module
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
Flash	Flash memory
FlexCAN	Controller Area Network (FlexCAN)
FMPLL	Frequency-Modulated Phase-Locked Loop
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit
XBAR	Crossbar switch

Figure 1. MPC5602D series block diagram

Table 1. MPC5602D series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to digital-converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “*n*” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU

Table 1. MPC5602D series block summary (continued)

Block	Function
Real-time counter (RTC)	Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Device family overview

This section presents the device's critical performance parameters, and lists both the chip-level and module features as well as the available packages.

Table 2 provides a comparison summary of the different MPC5602D family members and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family.

Table 2. MPC5602D device comparison

Feature	Device			
	MPC5601DxLH	**MPC5601DxLL**	**MPC5602DxLH**	**MPC5602DxLL**
CPU	e200z0h			
Execution speed	Static – up to 48 MHz			
Code flash memory	128 KB		256 KB	
Data flash memory	64 KB (4 × 16 KB)			
SRAM	12 KB		16 KB	
eDMA	16 ch			
ADC (12-bit)	16 ch	33 ch	16 ch	33 ch
CTU	16 ch			
Total timer I/O[1] eMIOS	14 ch, 16-bit	28 ch, 16-bit	14 ch, 16-bit	28 ch, 16-bit
• Type X[2]	2 ch	5 ch	2 ch	5 ch
• Type Y[3]	—	9 ch	—	9 ch
• Type G[4]	7 ch	7 ch	7 ch	7 ch
• Type H[5]	4 ch	7 ch	4 ch	7 ch
SCI (LINFlex)	3			
SPI (DSPI)	2			
CAN (FlexCAN)	1			
GPIO[6]	45	79	45	79
Debug	JTAG			
Package	64 LQFP	100 LQFP	64 LQFP	100 LQFP

NOTES:
1 Refer to eMIOS chapter of device reference manual for information on the channel configuration and functions.
2 Type X = MC + MCB + OPWMT + OPWMB + OPWFMB + SAIC + SAOC
3 Type Y = OPWMT + OPWMB + SAIC + SAOC
4 Type G = MCB + IPWM + IPM + DAOC + OPWMT + OPWMB + OPWFMB + OPWMCB + SAIC + SAOC
5 Type H = IPWM + IPM + DAOC + OPWMT + OPWMB + SAIC + SAOC
6 I/O count based on multiplexing with peripherals

3.1 Critical performance parameters

The critical performance parameters of the MPC5602D feature the following:

- Fully static design operation up to a maximum of 48 MHz, based on 125 °C ambient temperature
- Low-power design
  - Designed for dynamic power management of core and peripherals
  - Software-controlled clock gating of peripherals
  - Multiple power domains to minimize leakage in low-power modes
- Internal voltage regulator (VREG) enables control with a single input voltage for device operation below 100 mA with optional external ballast resistor for supporting maximum performance
  - 3.3 or 5 V ± 10% input supply voltage
- ADC analog supply 3.3 V or 5 V ± 10%
- Configurable pins
  - Selectable pull-up, pull-down, or no pull on all GPIO pins
  - Selectable open-drain pin
- Frequency modulated phase-locked loop
- –40 to 125 °C ambient operating temperature range[1]

Table 3. Operating mode summary[1]

Operating modes	SOC features				Clock sources				Periodic wakeup	Wakeup input	VREG mode	Wakeup time[2]						
	Core	Peripherals	Flash	SRAM	PLL	16 MHz FIRC	XOSC	128 kHz SIRC				VREG startup	IRC wakeup	Flash recovery	OSC stabilization	PLL lock	S/W reconfiguration	Mode switch over
RUN	On	OP	OP	On	OP	On	OP	On	—	—	FP	—	—	—	—	—	—	—
HALT	CG	OP	OP	On	OP	On	OP	On	OP	OP	FP	—	—	—	—	—	—	TBD[3]
STOP	CG	OP	APD	On	CG	OP	OP	On	OP	OP	LP	25 µs	8 µs	>125 µs	8 ms	200 µs	—	33 µs
STANDBY	Off	Off	Off	16 KB[4]	Off	OP	Off	OP	OP	OP	LP	25 µs	8 µs	>125 µs	8 ms	200 µs	Var	33 µs
POR	—	—	—	—	—	—	—	—	—	—	—	250 µs	8 µs	>125 µs	8 ms	200 µs	—	BAM

1. Assuming that the absolute maximum of 150 °C junction temperature is respected

NOTES:
1 Table key:
APD: Analog power-down
BAM: Boot Assist Module Software and Hardware used for device startup and configuration
CG: Clock Gated, Powered but clock stopped
FP: VREG Full Performance mode
LP: VREG Low Power mode, reduced output capability of VREG but lower power consumption
Off: Powered off and clock gated
On: Powered and clocked
OP: Optionally configurable to be enabled or disabled (clock gated)
POR: Power-on reset
Var: Variable duration, based on the required reconfiguration and execution clock speed configuration
2 A high level summary of some key durations that need to be considered when recovering from low-power modes. This does not account for all durations at wakeup. Other delays will be necessary to consider including, but not limited to the external supply startup time.
IRC wakeup time must not be added to the overall wakeup time as it starts in parallel with the VREG.
All other wakeup times must be added to determine the total startup time. For example, out of STANDBY, if Flash is needed, the total wakeup time will be 120 µs.
3 TBD: To be defined
4 16 KB of SRAM content retained but not accessible in STANDBY mode

3.2 Low power operation

MPC5602D devices provide two dynamic power modes—RUN and HALT—and two static low-power modes—STANDBY and STOP.

Both low-power modes use clock gating to halt the clock for all or part of the device. Additionally, the STANDBY mode uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.

RUN modes are the main operating modes where the entire device can be powered and clocked. Four dynamic RUN modes are supported—RUN0 – RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and systems clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the core system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, Flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the core and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wakeup from STOP mode is triggered by an external event or by the internal periodic wakeup, if enabled.

STANDBY mode halts the clock to the entire device and turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be woken up from STANDBY mode by any of up to 18 external wakeup pins, a reset, or from a periodic wakeup using a low-power oscillator. If required by the user, it is possible to enable the internal 16 MHz or 128 kHz RC oscillator.

In STANDBY mode, the contents of the cores, on-chip peripheral registers and potentially some of the volatile memory are not held. STANBDY mode retains 16 KB of the SRAM

A fast wakeup using the on-chip 16 MHz internal RC oscillator allows rapid execution from SRAM on exit from low-power modes. This oscillator supports low speed code execution and clocking of peripherals through selection as the system clock, and it can be used as the PLL input clock source to provide fast startup without the external oscillator delay.

In low power modes, the internal 16 MHz RC oscillator also supports the operation of ADCs.

Additionally, up to 18 external wakeup pins are available for wakeup, and a fast startup internal voltage regulator provides a rapid exit from low-power modes.

3.3 Chip-level features

On-chip modules available within the family include the following features:

- Single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with the Power Architecture embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 256 KB on-chip code flash memory supported with the Flash controller
- 64 KB on-chip data flash memory
- Up to 16 KB on-chip SRAM
- Interrupt controller (INTC) capable of handling 155 selectable-priority interrupt sources
- Frequency-modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash memory, or SRAM from multiple bus masters
- 16-channel eDMA controller with multiple transfer request sources using DMAMUX
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- One 12-bit analog-to-digital converter (ADC)
- Cross Trigger Unit (CTU) to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- 2 serial peripheral interface (DSPI) modules
- 3 serial communication interface (LINFlex) modules

- 1 enhanced full CAN (FlexCAN) module with configurable buffers
- Up to 79 configurable general purpose pins supporting input and output operations (package dependent)
- Real-Time Counter (RTC)
  - Clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
- Up to 4 periodic interrupt timers (PITs) with 32-bit counter resolution
- Device/board boundary scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

3.4 Module features

The following sections provide more details of the modules implemented on the MPC5602D.

3.4.1 e200z0h core processor

The e200z0h core includes the following features:

- High performance, low cost e200z0h core processor for managing peripherals and interrupts
- Single issue 4-stage pipelined in-order execution, 32-bit Power Architecture CPU
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in efficient code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Harvard architecture with separate instruction and load/store buses
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Multi-cycle divide word (divw), and load multiple word (lmw) store multiple word (smw) multiple class instructions, can be interrupted to prevent increases in interrupt latency
- Nexus1 support

3.4.2 Crossbar switch (XBAR)

The following summarizes the MPC5602D's implementation of the crossbar switch:

- 3 master ports:

  - CPU instruction bus
  - CPU load/store bus
  - eDMA
- Multiple bus slaves to enable access to flash memory, SRAM and peripherals
- Crossbar supports up to 2 consecutive transfers at any one time
- 32-bit internal address bus, 32-bit internal data bus
- Fixed priority arbitration based on port master

3.4.3 Interrupt controller (INTC)

The MPC5602D implements an interrupt controller that features the following:

- Unique 9-bit vector for each of the 155 separate interrupt sources
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
- External high priority interrupt directly accessing the main core critical interrupt mechanism

3.4.4 System integration unit lite (SIUL)

The SIUL features the following:

- Up to 4 levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control of up to 79 input/output pins (package dependent)
- All GPIO pins independently configurable to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs, with selected pins able to also support outputs
- Direct readback of the pin value supported on all digital output pins through the SIUL
- Configurable digital input filter that can be applied to up to 16 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset
- Support for two 32-bit virtual ports via the DSPI serialization

3.4.5 Flash memory

The on-chip flash memory on the MPC5602D features the following:

- Up to 256 KB code flash

  - 2 × 16 KB, 3 × 32 KB and 1 × 128 KB sectors
  - Typical flash memory access time: 0 wait-state for buffer hits, 2 wait-states for page buffer miss at 48 MHz
  - Page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
  - 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Censorship protection scheme to prevent flash-memory content visibility
- Separate dedicated data flash for EEPROM emulation
  - 4 erase sectors each containing 16 KB of memory
  - Offers read-while-write functionality from main program space
- Small block flash memory arrangement in main array to support features such as boot block, operating system block
- Hardware managed flash memory writes, erase and verify sequence
- Error correction status
  - Configurable error-correcting codes (ECC) reporting for SRAM and flash memory
  - Supports optional reporting of single-bit errors
  - Protected mechanism for reporting of corrected ECC values
  - Error address recorded including Access type and Master
  - Flash-memory ECC reporting registers mirrored into ECSM address space but data comes from the flash-memory module
  - Flash-memory module can be interrogated to provide ECC bit error location
  - Margin read for flash-memory array supported for initial program verification

3.4.6 SRAM

The on-chip SRAM on the MPC5602D features the following:

- Up to 16 KB general purpose RAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block
- 32-bit ECC with single-bit correction, double-bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses

3.4.7 Boot assist module (BAM)

The device implements a Boot Assist Module (BAM):

- Block of read-only memory containing VLE code which is executed according to boot mode of the device
- Download of code into internal SRAM possible via FlexCAN or LINFlex, after which code can be executed

3.4.8 Enhanced modular input output system (eMIOS)

The MPC5602D implements a scaled-down version of the eMIOS module:

- Up to 28 timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Supports configurable trigger outputs for ADC conversion for synchronization to channel output waveforms
- Edge-aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- DMA transfer support available

Table 4 shows the supported eMIOS modes.

Table 4. Supported eMIOS channel modes

Mode		Channel type			
Description	Name	Counter / OPWM / ICOC	O(I)PWM / OPWFMB / OPWMCB / ICOC	O(I)PWM / ICOC	OPWM / ICOC
Double action output compare	DAOC	x	x	x	—
General purpose input / output	GPIO	x	x	x	x
Input filter	IPF	x	x	x	x
Input period measurement	IPM	x	x	x	—
Input pulse width measurement	IPWM	x	x	x	—
Modulus counter	MC	x	—	—	—
Modulus counter buffered (up / down)	MCB	x	x	—	—
Output pulse width and frequency modulation buffered	OPWFMB	x	x	—	—
Output pulse width modulation buffered	OPWMB	—	x	x	x
Center aligned output PWM buffered with dead time	OPWMCB	—	x	—	—
Output pulse width modulation trigger	OPWMT	x	x	x	x
Pulse edge accumulation	PEA	x	—	—	—
Pulse edge counting	PEC	x	—	—	—
Quadrature decode	QDEC	x	—	—	—
Single action input capture	SAIC	x	x	x	x
Single action output compare	SAOC	x	x	x	x

Table 5 shows the maximum eMIOS channel allocation.

Table 5. eMIOS configuration

Channel type	Maximum number of channels
Counter / OPWM / ICOC[1]	5
O(I)PWM / OPWFMB / OPWMCB / ICOC[2]	7
O(I)PWM / ICOC[3]	7
OPWM / ICOC[4]	9

NOTES:
1 Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.
2 Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.
3 Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.
4 Each channel supports a range of modes including PWM generation, Input Capture, Output Compare.

3.4.9 Deserial serial peripheral interface module (DSPI)

MPC5602D devices have two DSPI modules. Features include:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- 6 chip select lines for DSPI_0 and 5 for DSPI_1, depending on package and pin multiplexing, to enable 64 external devices to be selected using external muxing from a single DSPI
- Up to 8 transfer types, independently configurable for each DSPI using the clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA
- 32-bit serialization of data enabling virtual GPIO ports on two DSPI modules

3.4.10 Controller area network module (FlexCAN)

MPC5602D devices have one FlexCAN module. Features include:

- Compliant with CAN protocol specification, version 2.0B active
- 32 mailboxes
  - Mailboxes configurable while module remains synchronized to CAN bus

  - Each mailbox configurable as transmit or receive
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - 2 mailboxes filtered
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen-only mode capabilities

3.4.11 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5602D:

- System clock can be derived from the following sources
  - External crystal oscillator
  - FMPLL
  - 16 MHz fast internal RC oscillator
- Programmable output clock divider of system clock (÷1, ÷2, ÷4)
- Separate programmable peripheral bus clock divider ratio (÷1, ÷2, ÷4) applied to system clock
- Frequency-modulated phase-locked loop (FMPLL)
  - Input clock frequency from 4 MHz to 16 MHz
  - Clock source: external oscillator
  - Lock detect circuitry continuously monitors lock status
  - Loss of clock (LOC) detection for reference and feedback clocks
  - On-chip loop filter
    Improves electromagnetic interference performance
    Reduces number of external components required
- On-chip fast external crystal oscillator supporting 4 MHz to 16 MHz
- Dedicated 16 MHz fast internal RC oscillator
  - Used as default clock source out of reset
  - Provides clock for rapid startup from low-power modes
  - Provides back-up clock in the event of FMPLL or external oscillator clock failure
  - Offers independent clock source for the watchdog timer
  - 5% accuracy over the operating temperature range
  - Trimming registers to support frequency adjustment with in-application calibration

- Dedicated 128 kHz slow internal RC oscillator for low-power mode operation and self wakeup
  - 10% accuracy
  - Trimming registers to support improve accuracy with in-application calibration

3.4.12 System timers

3.4.12.1 Introduction

The system timers include:

- Peripheral Interrupt Timer (PIT) timers (including ADC trigger)
- 1 Real-time Counter (RTC) timer

The PIT is an array of timers that can be used to raise interrupts, trigger CTU channels, and ADC conversions. The RTC supports wakeup from low-power modes or real-time clock generation.

3.4.12.2 Periodic interrupt timer module (PIT)

The PIT features the following:

- 4 general purpose interrupt timers
- 1 interrupt timer for triggering ADC injected conversions (12-bit ADC)
- Up to 2 interrupt timers for triggering DMA transfers
- 1 interrupt timer for triggering CTU
- 32-bit counter resolution
- Clocked by system clock frequency

3.4.12.3 Real-time counter (RTC)

The RTC features the following:

- Configurable resolution for different timeout periods
  - 1 sec resolution for > 1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources
  - 128 kHz slow internal RC oscillator (SIRC)
  - Divided 16 MHz fast internal RC oscillator (FIRC)
- Supports continued operation through all resets except POR (power-on reset)

3.4.13 System watchdog timer

The watchdog on the MPC5602D features the following:

- Activation by software or out of reset
- 32-bit modulus counter

- Clock source: robust 128 kHz slow internal RC oscillator (divisible by 1 to 32)
- Supports normal or windowed mode
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Reset by writing a software key to memory mapped register
- Support for protected access to watchdog control registers with optional soft and hard locks
  - Soft lock allows temporary locking of configuration
  - Once enabled, hard lock prevents any changes until after a reset
- Supports halting during low power modes

3.4.14 On-chip voltage regulator (VREG)

The on-chip voltage regulator includes the following features:

- Optional support for internal and external ballast resistor based on power consumption
- Regulates 3.3 or 5 V ±10% input to generate all internal supplies for internal control
- Manages power gating
- Low-power regulators support operation when in STOP and STANDBY modes to minimize power consumption
- Fast startup on-chip regulators for rapid exit from low power modes
- Low voltage reset supported on all internal supplies

3.4.15 Analog-to-digital converter module (ADC)

The ADC features the following:

- One 12-bit ADC module supporting synchronous conversions on channels
- 0–V_{DD} common mode conversion range
- Conversions times of < 2 µs available[1]
- Up to 33 single-ended input channels, expandable to 61 channels with external multiplexers
- Internally multiplexed channels
  - Up to 33 channels of which 16 high-accuracy
  - Dedicated result register available for every internally muxed channel
- Externally multiplexed channels
  - Internal control to support generation of external analog multiplexor selection
  - 4 internal channels optionally used to support externally multiplexed inputs, providing transparent control for additional ADC channels
  - Each of the 4 channels supports up to 8 externally muxed inputs
  - Individual dedicated result register also available for externally muxed conversion channels

1. Please refer to the data sheet for up-to-date values on current consumption. This value is only estimates and has not been validated.

  - 3 independently configurable sample and conversion times for high occurrence channels, internally muxed channels and externally muxed channels
- Support for one-shot, scan and injection conversion modes
- Independently configurable sampling duration for each type of channel
- Conversion triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT) or timed I/O module (eMIOS) through cross triggering unit (CTU)
  - Internal conversion triggering from PIT
  - 1 input pin configurable as external conversion trigger source
- Up to 6 configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range
- All unused analog pins available as general purpose input pins
- Unused 12-bit ADC analog pins, with the exception of the 16 dedicated high accuracy channels, available as general purpose output pins
- Power-down mode
- Supports DMA transfer of results based on end of conversion chain or each conversion
- Separate dedicated DMA request for injection mode

3.4.16 Enhanced direct memory access controller (eDMA)

The following summarizes the MPC5602D's implementation of the eDMA controller:

- 16 channels to support independent 8-, 16-, or 32-bit single value or block transfers
- Support of variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by peripheral, CPU, periodic timer interrupt or eDMA channel request
- Peripheral DMA request sources include DSPIs, 12-bit ADC, eMIOS and GPIOs
- Each eDMA channel able to optionally send interrupt request to CPU on completion of single value or block transfer
- DMA transfers possible between system memories and all accessible memory mapped locations including peripheral and registers
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with total of up to 16 potential request sources

3.4.17 Cross trigger unit (CTU)

The CTU enables the synchronization of ADC conversions with a timer event. Its key features are:

- Single cycle delayed trigger output trigged by up to 29 input flags/events connected to different timers in the system
- Triggers ADC conversions from any eMIOS channel
- Triggers ADC conversions from one dedicated PIT
- Maskable interrupt generation whenever a trigger output is generated
- 1 event configuration register dedicated to each timer event allows to define the corresponding ADC channel
- Acknowledgment signal to eMIOS/PIT for clearing the flag
- Synchronization with ADC to avoid collision

3.4.18 Serial communication interface module (LINFlex)

The LINFlex on the MPC5602D features the following:

- 3 LINFlex modules supported
- Supports LIN master mode, LIN slave mode and UART mode
- 1 module supporting LIN master and slave mode; 2 modules supporting LIN master mode
- LIN state machine compliant to LIN 1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store identified and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors
    - Sync field
    - Delimiter
    - ID parity
    - Bit, framing
    - Checksum and timeout errors
  - Classic or extended checksum calculation
  - Configurable break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features
    - Loop back
    - Self Test
    - LIN bus stuck dominant detection
  - Interrupt driven operation with 16 interrupt sources

- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - 16 ID filters for discarding irrelevant LIN responses
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-bytes receive, 4-bytes transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with 4 interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud rate modulus counter; baud rate can be fractioned with 1/16 granularity
  - 2 receiver wakeup methods

MPC5602D devices include two functionally different LINFlex controller types. These are distinguished in the documentation by the abbreviations “LINFlex” and “LINFlexD”. The latter name represents the DMA support available on this controller type. The MPC5602D devices combine these two types to provide up to three modules supporting the LINFlex protocol. The module (instance) numbers and the corresponding functional controller type are listed below:

- Module 0—LINFlexD
- Module 1—LINFlex
- Module 2—LINFlex

3.4.19 JTAG controller (JTAGC)

JTAG features the following:

- JTAG low pin count interface (IEEE 1149.1) test access port (TAP) interface
- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Supports boundary scan testing
- All JTAG pins reusable in application as standard I/Os

3.5 Packages

MPC5602D family members are offered in the following package types:

- 64-pin LQFP, 0.5 mm pitch, 10 mm × 10 mm outline
- 100-pin LQFP, 0.5 mm pitch, 14 mm × 14 mm outline

4 Application example

The MPC5602D is designed to address central body, vehicle body controllers, smart junction box and front module applications, and to support sensorless motor control with ripple counting within the vehicle. As shown in the following example, the MCU is central to the application and provides the flexibility to add or remove peripheral components in a modular design.

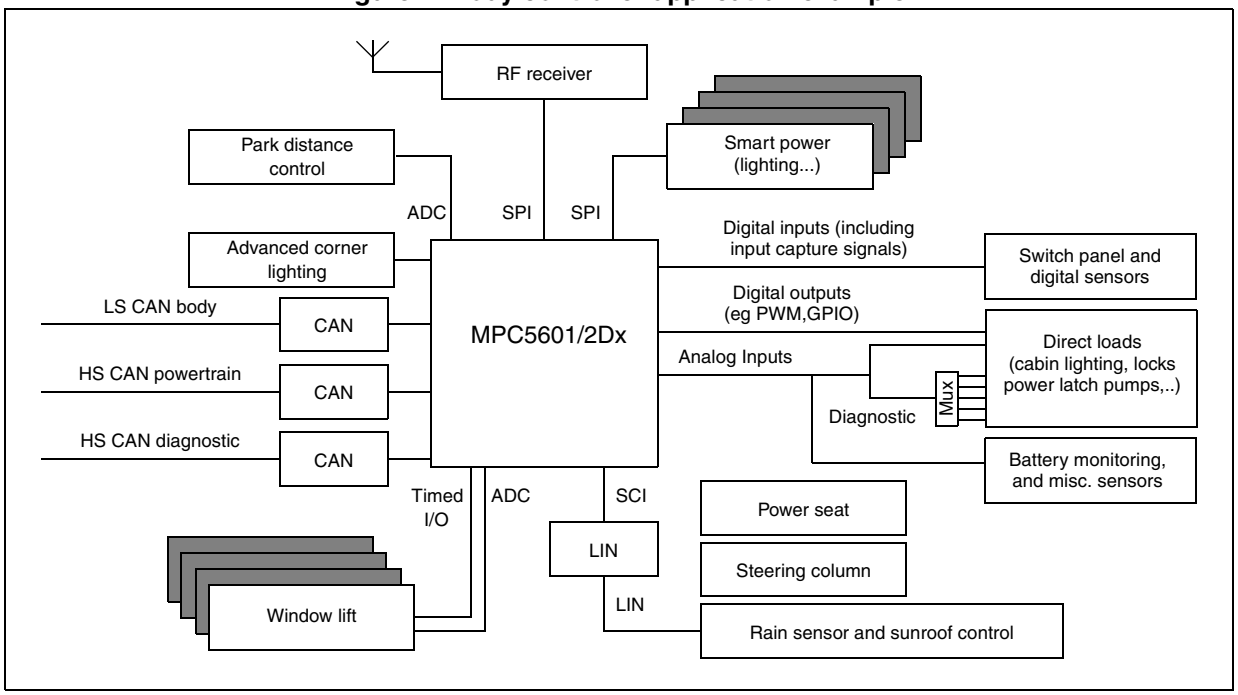
4.1 Body controller application example

Body controller modules primarily control the following:

- Comfort features—doors, seats, interior lighting
- Security/access features—passive entry, immobilizer, Tire-pressure monitoring system (TPMS)
- Lighting—headlights, brake lights, turn lights
- Centralized diagnostic and network management
- Vehicle communications network routing— Controller Area Network (CAN)

Figure 2 shows the MPC5602D used in a typical body controller application.

Figure 2. Body controller application example



5 Developer environment

The MPC5602D MCU family is supported by tools and third-party developers similar to those supporting Freescale MPC5500 products, offering a widespread, established network of tools and software vendors.

The following development support is available:

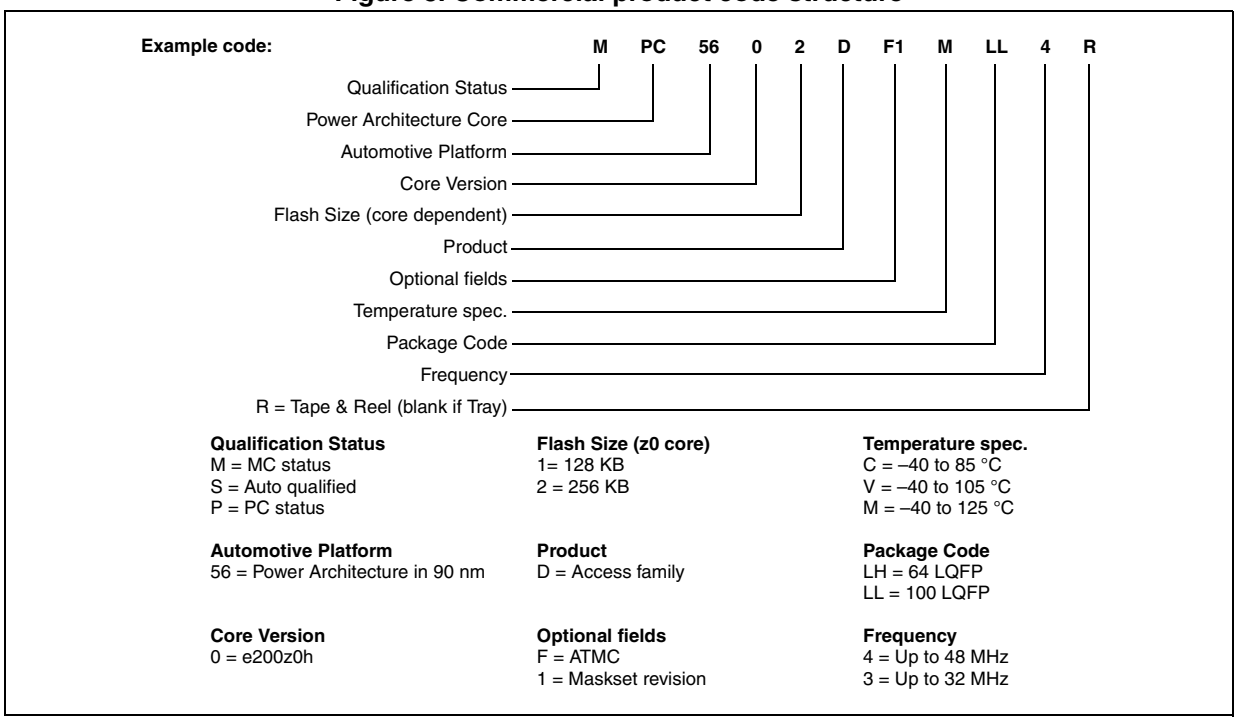
- Automotive evaluation boards (EVB) featuring CAN, LIN interfaces, and more
- Compilers
- Debuggers
- JTAG and Nexus1 interfaces

The following software support is available:

- OSEK solutions is available from multiple third parties
- CAN and LIN drivers
- AUTOSAR package

6 Orderable parts

Figure 3. Commercial product code structure



7 Revision history

Table 6 summarizes revisions to this document.

Table 6. Document revision history

Revision	Date	Substantive changes
1	11 Feb 2009	Initial release
2	28 May 2010	Updated the entire document
2.1	14 Jul 2010	Corrected the security classification of this document (is FCP)
3	27 Ago 2010	Replaced all occurrences of “e200z0” with “200z0h” Added contents concerning eDMA and I^2C blocks in the “MPC5602D series block summary” table. Removed “Current consumption estimates” table Removed second level bullet from “Interrupt Controller (INTC)” section Removed “Flash partitioning” table Updated the footnote of “Analog to Digital Converter Module (ADC)” section Rewrote first bullet within “Cross Trigger Unit (CTU)” section Updated the “Serial Communication Interface Module (LINFlex)” section Removed “P/I” from the blocks of “Body controller application example” figure Removed “Order code” table
3.1	23 Feb 2011	Deleted the “Freescale Confidential Proprietary” label (the document is public)

Table 6. Document revision history (continued)

Revision	Date	Substantive changes
4	16 Jun 2011	Editorial and formatting changes throughout Section 1.3, “MPC5602D features: added an explanation of which LINFlex modules support master mode and slave mode; changed “LINFlex 0: Master capable and slave capable” to “LINFlex 0: Master capable and slave capable; connected to eDMA” MPC5602D device comparison: changed “13 ch” to “14 ch” for Total timer I/O eMIOS Section 3.1, “Critical performance parameters: Removed I/O characteristics tables and FMPLL characteristics table (these characteristics can be found in the device datasheet) Commercial product code structure: Added character for frequency; updated optional fields character and description

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