HEF4060B

14-stage ripple-carry binary counter/divider and oscillator

Rev. 9 — 8 July 2019 **Product data sheet**

1. General description

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, REXT and CEXT), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset input (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The clock input' s Schmitt-trigger action makes it highly tolerant to slower clock rise and fall times. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13 = LOW), independent of other input conditions.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40 ° C to +85 ° C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from -40 ° C to +85 ° C.

Type number	Package		
	Name	**Description**	**Version**
HEF4060BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4060BTT	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

nexperia

4. Functional diagram

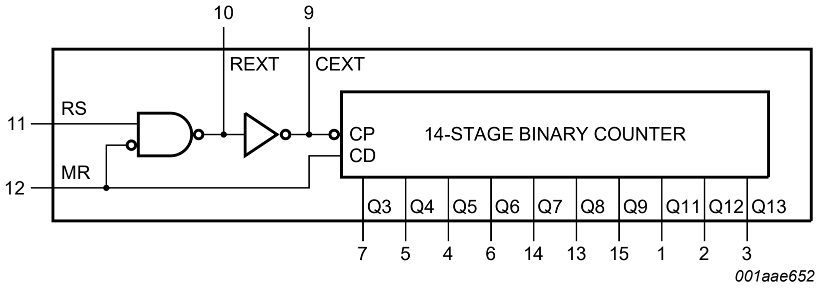


Fig. 1. Functional diagram

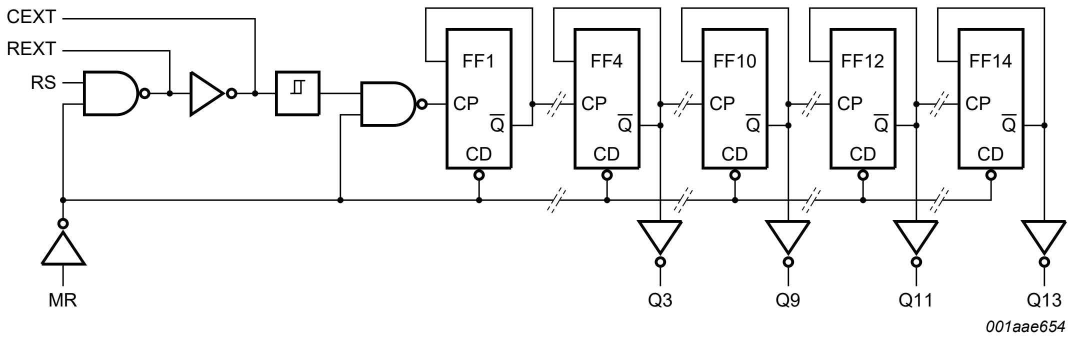


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning

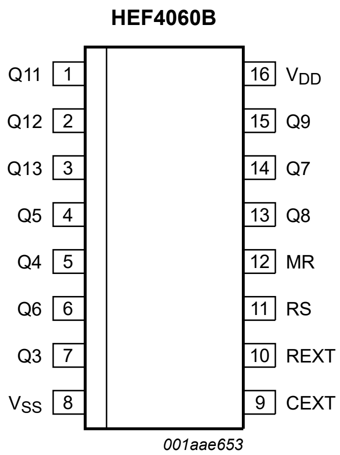


Fig. 3. Pin configuration SOT109-1 (SO16)

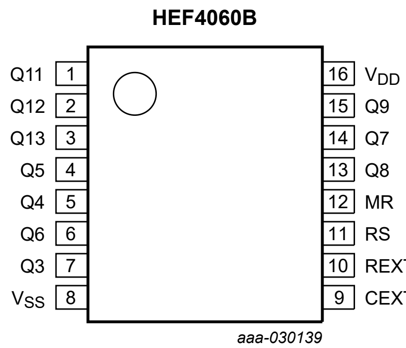


Fig. 4. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
V_{SS}	8	ground supply voltage
CEXT	9	external capacitor connection
REXT	10	oscillator pin
RS	11	clock input/oscillator pin
MR	12	master reset
V_{DD}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH clock transition; ↓ HIGH-to-LOW clock transition.

Input		Output
RS	**MR**	**Q3 to Q9 and Q11 to Q13**
↑	L	no change
↓	L	count
X	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} -40 °C to +85 °C [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	input MR				
		V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C; V_{SS} = 0 V; C_L = 50 pF; $t_r = t_f \leq 20$ ns; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{pd}	propagation delay	RS → Q3; see Fig. 5	5 V [2]	183 ns + (0.55 ns/pF) C_L	-	210	420	ns
			10 V	69 ns + (0.23 ns/pF) C_L	-	80	160	ns
			15 V	42 ns + (0.16 ns/pF) C_L	-	50	100	ns
		Qn → Qn + 1; see Fig. 5	5 V	-	-	25	50	ns
			10 V	-	-	10	20	ns
			15 V	-	-	6	12	ns
		MR → Qn; HIGH to LOW see Fig. 5	5 V	73 ns + (0.55 ns/pF) C_L	-	100	200	ns
			10 V	29 ns + (0.23 ns/pF) C_L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF) C_L	-	30	60	ns
t_t	transition time	see Fig. 5	5 V [3]	10 ns + (1.00 ns/pF) C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF) C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) C_L	-	20	40	ns
t_W	pulse width	minimum width; RS HIGH; see Fig. 5	5 V		120	60	-	ns
			10 V		50	25	-	ns
			15 V		30	15	-	ns
		minimum width; MR HIGH; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t_{rec}	recovery time	input MR; see Fig. 5	5 V		160	80	-	ns
			10 V		80	40	-	ns
			15 V		60	30	-	ns
f_{max}	maximum frequency	input RS; see Fig. 5	5 V		4	8	-	MHz
			10 V		10	20	-	MHz
			15 V		15	30	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_t is the same as t_{THL} and t_{TLH}.

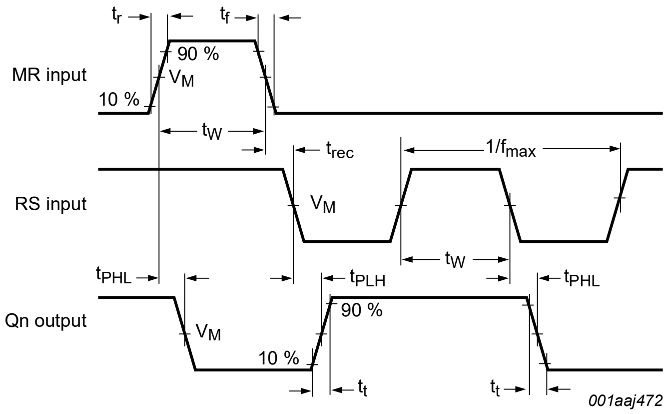
Table 8. Power dissipation

Dynamic power dissipation P_D and total power dissipation P_{tot} can be calculated from the formulas shown. T_{amb} = 25 °C.

Symbol	Parameter	Conditions	V_{DD}	Typical formula for P_D and P_{tot} (μW)[1]
P_D	dynamic power dissipation	per device	5 V	$P_D = 700 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$
			10 V	$P_D = 3300 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$
			15 V	$P_D = 8900 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$
P_{tot}	total power dissipation	when using the on-chip oscillator	5 V	$P_{tot} = 700 \times f_{osc} + \sum(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 690 \times V_{DD}$
			10 V	$P_{tot} = 3300 \times f_{osc} + \sum(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 6900 \times V_{DD}$
			15 V	$P_{tot} = 8900 \times f_{osc} + \sum(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 22000 \times V_{DD}$

[1] Where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{DD} = supply voltage in V;
$\sum(f_o \times C_L)$ = sum of the outputs;
C_t = timing capacitance (pF);
f_{osc} = oscillator frequency (MHz).

10.1. Waveforms and test circuit

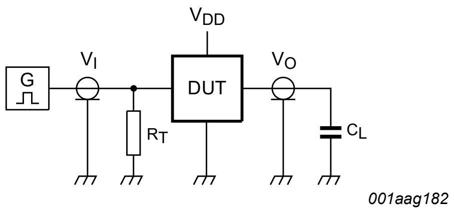


Measurement points are given in Table 9.

Fig. 5. Waveforms showing propagation delays for MR to Qn and $\overline{CP}$ to Q0, minimum MR, and $\overline{CP}$ pulse widths

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

C_L = load capacitance including jig and probe capacitance;

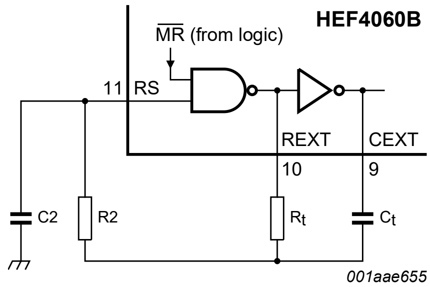
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

Table 10. Measurement point and test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. RC oscillator



Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.3 \times R_t \times C_t}$

Fig. 7. External component connection for RC oscillator

11.1. Timing component limitations

The oscillator frequency is mainly determined by R_t x C_t, provided R_t << R2 and R2 x C2 << R_t x C_t. The influence of the forward voltage across the input protection diodes on the frequency is minimized by R2. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS (Local Oxidation Complementary Metal-Oxide Semiconductor) 'ON' resistance in series with it, which typically is 500 Ω at V_{DD} = 5 V, 300 Ω at V_{DD} = 10 V and 200 Ω at V_{DD} = 15 V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

- C_t ≥ 100 pF, up to any practical value,
- 10 kΩ ≤ R_t ≤ 1 MΩ.

11.2. Typical crystal oscillator circuit

In Fig. 8, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

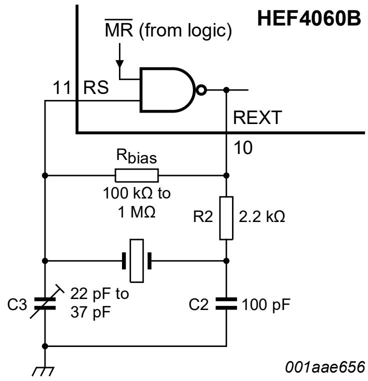
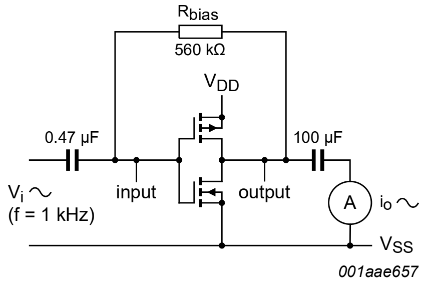
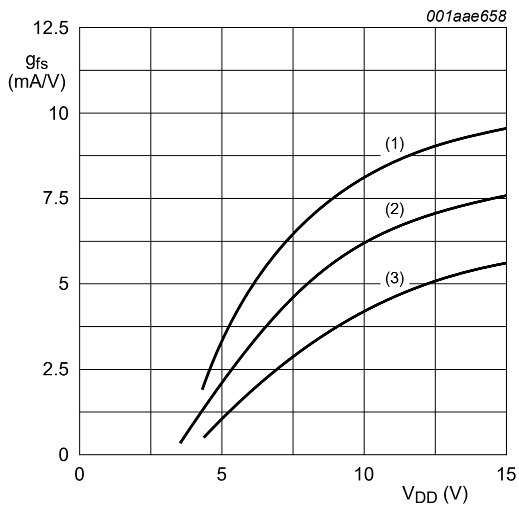


Fig. 8. External component connection for crystal oscillator



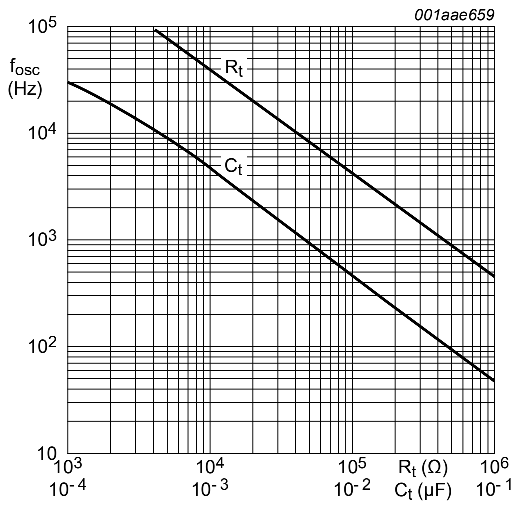
$g_{fs} = di_o/dv_i$ at v_o is constant (see also Fig. 10);
MR = LOW.

Fig. 9. Test setup for measuring forward transconductance (g_{fs})



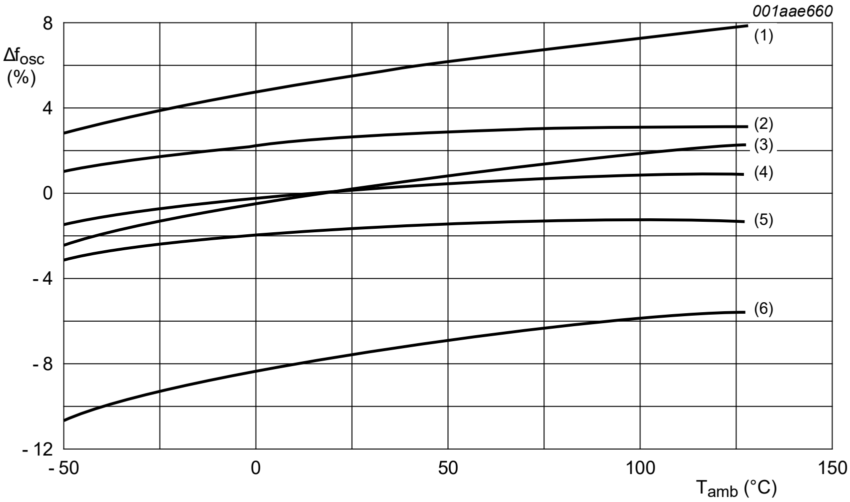
T_{amb} = 25 °C.
(1) Average + 2 σ.
(2) Average.
(3) Average - 2 σ.
Where ' σ' is the observed standard deviation.

Fig. 10. Typical forward transconductance g_{fs} as a function of the supply voltage



C_t curve at R_t = 100 kΩ; R2 = 470 kΩ.
R_t curve at C_t = 1 nF; R2 = 5 R_t.
V_{DD} = 5 V to 15 V; T_{amb} = 25 °C.

Fig. 11. RC oscillator frequency as a function of R_t and C_t



Lines (1) and (2): V_{DD} = 15 V.

Lines (3) and (4): V_{DD} = 10 V.

Lines (5) and (6): V_{DD} = 5 V.

Lines (1), (3), (6): R_t = 100 kΩ; C_t = 1 nF; R2 = 0 Ω.

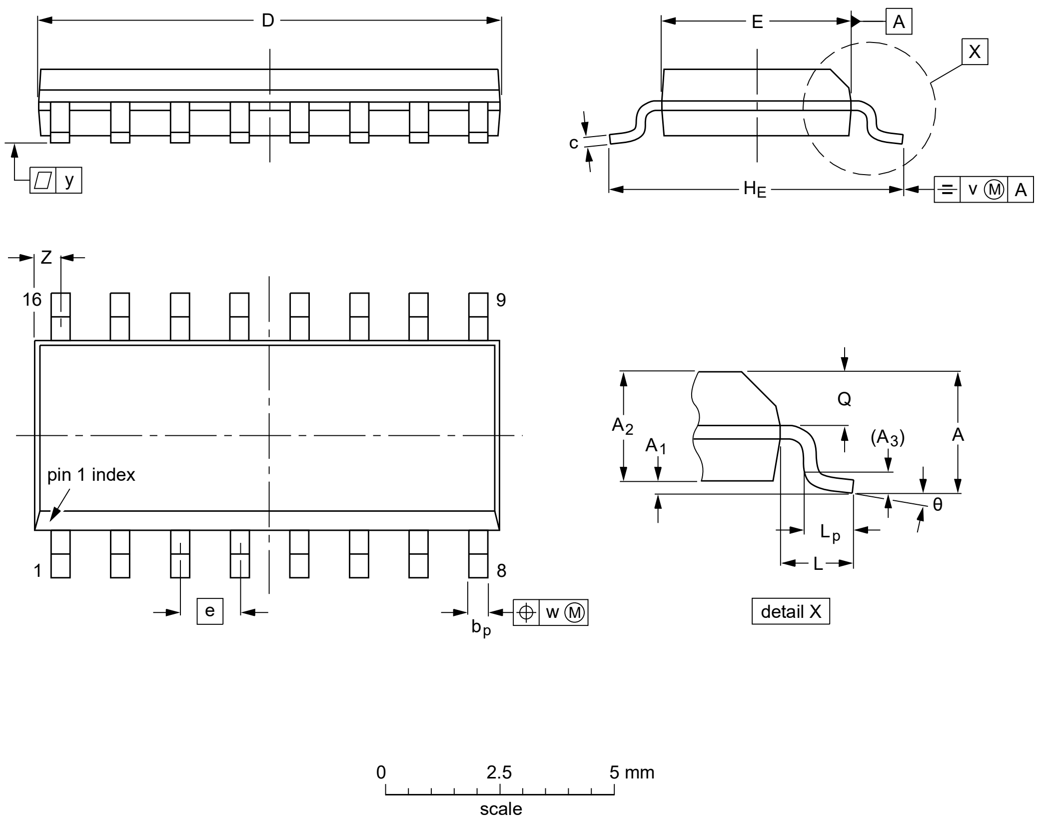
Lines (2), (4), (5): R_t = 100 kΩ; C_t = 1 nF; R2 = 300 kΩ.

Referenced at: f_{osc} at T_{amb} = 25 °C and V_{DD} = 10 V.

Fig. 12. Oscillator frequency deviation (Δf_{osc}) as a function of ambient temperature

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

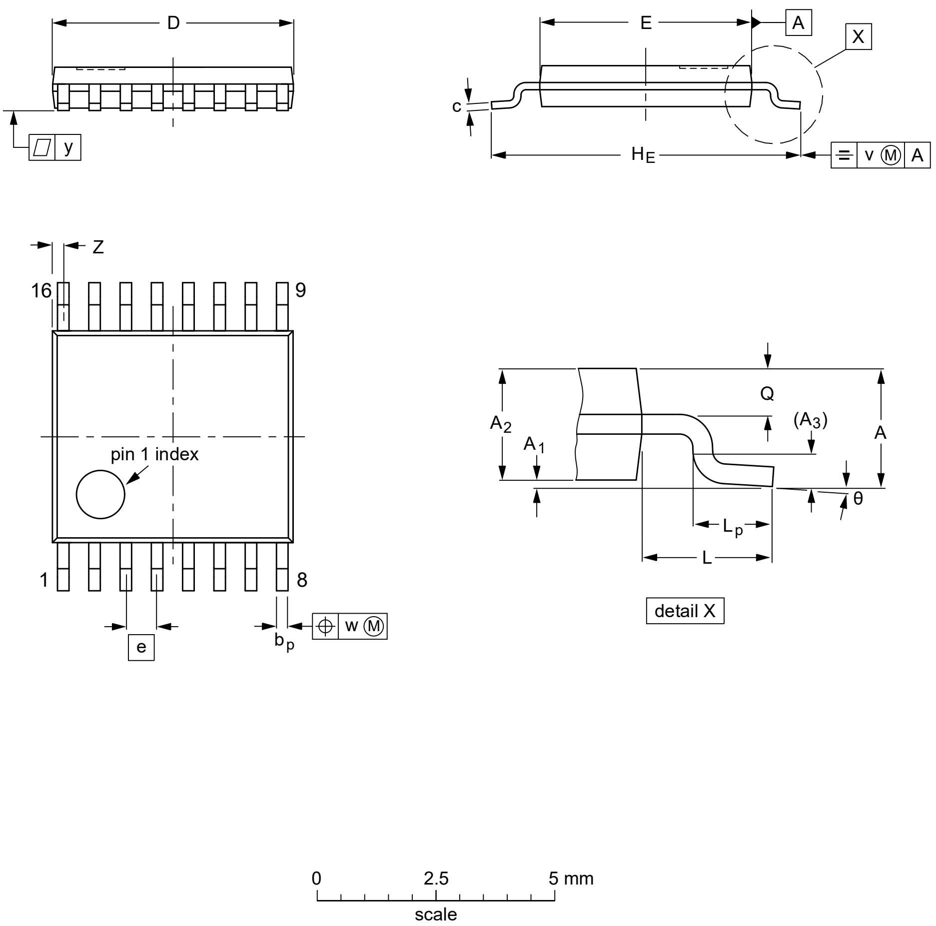
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(2)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 14. Package outline SOT403-1 (TSSOP16)

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4060B v.9	20190708	Product data sheet	-	HEF4060B v.8
Modifications:	• Type number HEF4060BTT (SOT403-1/TSSOP16) added.			
HEF4060B v.8	20160325	Product data sheet	-	HEF4060B v.7
Modifications:	• Type number HEF4060BP (SOT38-4) removed.			
HEF4060B v.7	20111116	Product data sheet	-	HEF4060B v.6
Modifications:	• Legal pages updated. • Changes in "General description" and "Features and benefits". • Section "Applications" removed.			
HEF4060B v.6	20110511	Product data sheet	-	HEF4060B v.5
HEF4060B v.5	20091127	Product data sheet	-	HEF4060B v.4
HEF4060B v.4	20090817	Product data sheet	-	HEF4060B_CNV v.3
HEF4060B_CNV v.3	19950101	Product specification	-	HEF4060B_CNV v.2
HEF4060B_CNV v.2	19950101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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