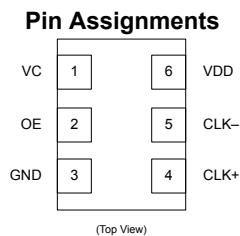
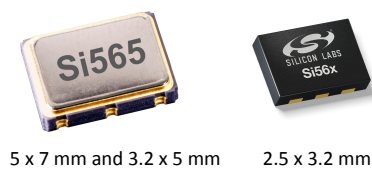


# Ultra Series™ Crystal Oscillator (VCXO) Si565 Data Sheet

## Ultra Low Jitter Any-Frequency VCXO (100 fs), 0.2 to 3000 MHz

The Si565 Ultra Series™ voltage-controlled crystal oscillator utilizes Silicon Laboratories' advanced 4<sup>th</sup> generation DSPLL<sup>®</sup> technology to provide an ultra-low jitter, low phase noise clock at any output frequency. The device is factory-programmed to any frequency from 0.2 to 3000 MHz with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. On-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in industry-standard footprints, the Si565 has a dramatically simplified supply chain that enables Silicon Labs to ship custom frequency samples 1-2 weeks after receipt of order. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si565 uses one simple crystal and a DSPLL IC-based approach to provide the desired output frequency. The Si565 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location/polarity. Specific configurations are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators.



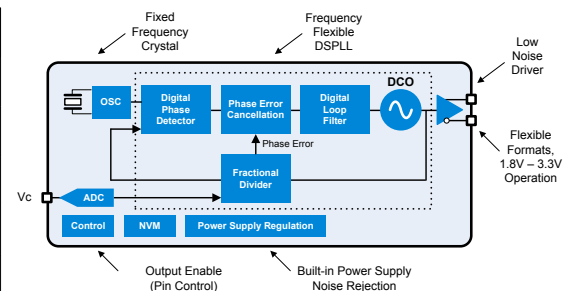
Pin #	Descriptions
1	VC = Voltage Control Pin
2	OE = Output enable
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output. Not used for CMOS.
6	VDD = Power supply

### KEY FEATURES

- Available with any frequency from 200 kHz to 3000 MHz
- Ultra low jitter: 100 fs RMS typical (12 kHz – 20 MHz)
- Excellent PSNR and supply noise immunity: –80 dBc Typ
- 3.3 V, 2.5 V and 1.8 V V<sub>DD</sub> supply operation from the same part number
- LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- 2.5x3.2, 3.2x5, 5x7 mm package options
- Samples available with 1-2 week lead times

### APPLICATIONS

- 100G/200G/400G OTN, coherent optics
- 10G/25G/40G/100G Ethernet
- 56G/112G PAM4 clocking
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Servers, switches, storage, NICs, search acceleration
- Test and measurement
- FPGA/ASIC clocking



## 1. Ordering Guide

The Si565 VCXO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to [www.silabs.com/oscillators](http://www.silabs.com/oscillators) to access this tool and for further ordering instructions.

VCXO Series	Description	Code	OE Pin	OE Polarity	Package	Temperature Grade
565	Single Frequency VCXO	A	Pin 2	Active High	A 5x7 mm	G -40 to 85 °C
		B	Pin 2	Active Low	B 3.2x5 mm	
					C 2.5x3.2 mm	

Signal Format	VDD Range	Order Option
LVPECL	2.5, 3.3 V	A
LVDS	1.8, 2.5, 3.3 V	B
CMOS	1.8, 2.5, 3.3 V	C
CML	1.8, 2.5, 3.3 V	D
HCSL	1.8, 2.5, 3.3 V	E
Dual CMOS (In-Phase)	1.8, 2.5, 3.3 V	F
Dual CMOS (Complementary)	1.8, 2.5, 3.3 V	G
Custom <sup>1</sup>	1.8, 2.5, 3.3 V	X

Temperature Stability = ± 20 ppm				
	Vc Tuning Slope Kv [ppm/V]	Min APR [± ppm] at VDD <sup>3</sup>		
		3.3V	2.5V	1.8V
A	60	20	--	--
B	75	40	20	--
C	105	70	40	20
D	150	115	75	45
E	180	145	100	65
F	225	190	135	85

Code	Reel
R	Tape and Reel
<Blank>	Coil Tape

Frequency Code <sup>2</sup>	Description
Mxxxxxx	F <sub>CLK</sub> < 1 MHz
xMxxxxx	1 MHz ≤ F <sub>CLK</sub> < 10 MHz
xxMxxxx	10 MHz ≤ F <sub>CLK</sub> < 100 MHz
xxxMxxx	100 MHz ≤ F <sub>CLK</sub> < 1000 MHz
xxxxMxx	1000 MHz ≤ F <sub>CLK</sub> < 3000 MHz
xxxxxx	Custom code if F <sub>CLK</sub> > 6 digits

565 A A A - - - - - A B G R

Device Revision

### Notes:

- Contact Silicon Labs for non-standard configurations.
- Create custom part numbers at [www.silabs.com/oscillators](http://www.silabs.com/oscillators).
- Min Absolute Pull Range (APR) includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
  - For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher Kv values to account for their higher temperature dependence, the Si56x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs.
  - APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±20 ppm is able to lock to a clock with a ±20 ppm stability over 20 years over all operating conditions.
  - APR (±) = (0.5 x VDD x tuning slope) - (initial accuracy + temp stability + load pulling + VDD variation + aging).
  - Minimum APR values noted above include absolute worst case values for all parameters.
  - See application note, "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)" for more information.

### 1.1 Technical Support

Frequently Asked Questions (FAQ)	<a href="http://www.silabs.com/Si565-FAQ">www.silabs.com/Si565-FAQ</a>
Oscillator Phase Noise Lookup Utility	<a href="http://www.silabs.com/oscillator-phase-noise-lookup">www.silabs.com/oscillator-phase-noise-lookup</a>
Quality and Reliability	<a href="http://www.silabs.com/quality">www.silabs.com/quality</a>
Development Kits	<a href="http://www.silabs.com/oscillator-tools">www.silabs.com/oscillator-tools</a>

## 2. Electrical Specifications

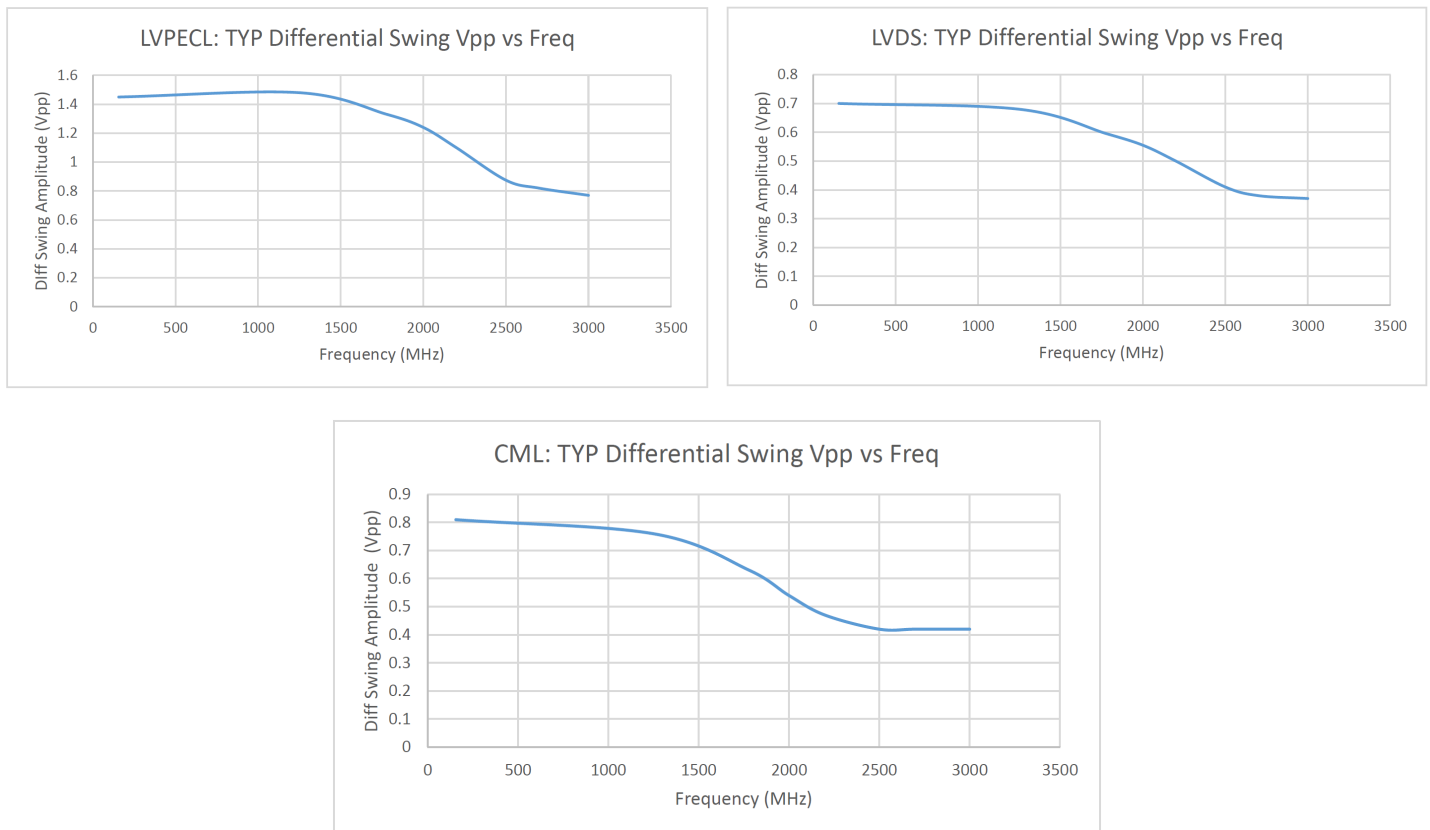
**Table 2.1. Electrical Specifications**
 $V_{DD} = 1.8\text{ V}, 2.5\text{ or }3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ 

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	$T_A$		-40	—	85	$^\circ\text{C}$
Frequency Range	$F_{CLK}$	LVPECL, LVDS, CML	0.2	—	3000	MHz
		HCSL	0.2	—	400	MHz
		CMOS, Dual CMOS	0.2	—	250	MHz
Supply Voltage	$V_{DD}$	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	$I_{DD}$	LVPECL (output enabled)	—	120	170	mA
		LVDS/CML (output enabled)	—	100	140	mA
		HCSL (output enabled)	—	95	140	mA
		CMOS (output enabled)	—	95	145	mA
		Dual CMOS (output enabled)	—	105	155	mA
		Tristate Hi-Z (output disabled)	—	83	—	mA
Temperature Stability <sup>1</sup>		-40 to 85 $^\circ\text{C}$	-20	—	20	ppm
Rise/Fall Time (20% to 80% $V_{PP}$ )	$T_R/T_F$	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS ( $C_L = 5\text{ pF}$ )	—	0.5	1.5	ns
		HCSL, $F_{CLK} > 50\text{ MHz}$	—	—	550	ps
Duty Cycle	$D_C$	All formats	45	—	55	%
Output Enable (OE) <sup>2</sup>	$V_{IH}$		$0.7 \times V_{DD}$	—	—	V
	$V_{IL}$		—	—	$0.3 \times V_{DD}$	V
	$T_D$	Output Disable Time, $F_{CLK} > 10\text{ MHz}$	—	—	3	$\mu\text{s}$
	$T_E$	Output Enable Time, $F_{CLK} > 10\text{ MHz}$	—	—	20	$\mu\text{s}$
Powerup Time	$t_{OSC}$	Time from $0.9 \times V_{DD}$ until output frequency ( $F_{CLK}$ ) within spec	—	—	10	ms
Powerup VDD Ramp Rate	$V_{RAMP}$	Fastest $V_{DD}$ ramp rate allowed on startup	—	—	9	V/ms
LVPECL Output Option <sup>3</sup>	$V_{OC}$	Mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	$V_O$	Swing (diff, $F_{CLK} \leq 1.5\text{ GHz}$ )	1.1	—	1.9	$V_{PP}$
		Swing (diff, $F_{CLK} > 1.5\text{ GHz}$ ) <sup>6</sup>	0.55	—	1.7	$V_{PP}$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
LVDS Output Option <sup>4</sup>	V <sub>OC</sub>	Mid-level (2.5 V, 3.3 V V <sub>DD</sub> )	1.125	1.20	1.275	V
		Mid-level (1.8 V V <sub>DD</sub> )	0.8	0.9	1.0	V
	V <sub>O</sub>	Swing (diff, F <sub>CLK</sub> ≤ 1.4 GHz)	0.6	0.7	0.9	V <sub>PP</sub>
		Swing (diff, F <sub>CLK</sub> > 1.4 GHz) <sup>6</sup>	0.25	0.5	0.8	V <sub>PP</sub>
HCSL Output Option <sup>5</sup>	V <sub>OH</sub>	Output voltage high	660	800	850	mV
	V <sub>OL</sub>	Output voltage low	-150	0	150	mV
	V <sub>C</sub>	Crossing voltage	250	410	550	mV
CML Output Option (AC-Coupled)	V <sub>O</sub>	Swing (diff, F <sub>CLK</sub> ≤ 1.5 GHz)	0.6	0.8	1.0	V <sub>PP</sub>
		Swing (diff, F <sub>CLK</sub> > 1.5 GHz) <sup>6</sup>	0.3	0.55	0.9	V <sub>PP</sub>
CMOS Output Option	V <sub>OH</sub>	I <sub>OH</sub> = 8/6/4 mA for 3.3/2.5/1.8 V V <sub>DD</sub>	0.85 × V <sub>DD</sub>	—	—	V
	V <sub>OL</sub>	I <sub>OL</sub> = 8/6/4 mA for 3.3/2.5/1.8 V V <sub>DD</sub>	—	—	0.15 × V <sub>DD</sub>	V

**Notes:**

1. Min APR includes temperature stability, initial accuracy, load pulling, V<sub>DD</sub> variation, and aging for 20 yrs at 70 °C.
2. OE includes a 50 kΩ pull-up to V<sub>DD</sub> for OE active high, or includes a 50 kΩ pull-down to GND for OE active low.
3. R<sub>term</sub> = 50 Ω to V<sub>DD</sub> - 2.0 V (see Figure 4.1).
4. R<sub>term</sub> = 100 Ω (differential) (see Figure 4.2).
5. R<sub>term</sub> = 50 Ω to GND (see Figure 4.2).
6. Refer to the figure below for Typical Clock Output Swing Amplitudes vs Frequency.

**Figure 2.1. Typical Clock Output Swing Amplitudes vs. Frequency**

**Table 2.2. V<sub>C</sub> Control Voltage Input**V<sub>DD</sub> = 1.8, 2.5 or 3.3 V ± 5%, T<sub>A</sub> = -40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Control Voltage Range	V <sub>C</sub>		0.1 x VDD	VDD/2	0.9 x VDD	V
Control Voltage Tuning Slope (V <sub>c</sub> = 10% VDD to 90% VDD)	Kv	Positive slope, ordering option	60, 75, 105, 150, 180, 225			ppm/V
Kv Variation	Kv_var		—	—	±10	%
Control Voltage Linearity	LVC	Best Straight Line fit	-1.5	±0.5	+1.5	%
Modulation Bandwidth	BW		—	10	—	kHz
Vc Input Impedance	ZVC		500	—	—	kΩ

**Table 2.3. Clock Output Phase Jitter and PSNR**V<sub>DD</sub> = 1.8 V, 2.5 or 3.3 V ± 5%, T<sub>A</sub> = -40 to 85 °C

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> All Differential Formats, F <sub>CLK</sub> ≥ 200 MHz	φ <sub>J</sub>	Kv = 60 ppm/V	—	100	150	fs
		Kv = 75 ppm/V	—	103	—	fs
		Kv = 105 ppm/V	—	110	—	fs
		Kv = 150 ppm/V	—	123	—	fs
		Kv = 180 ppm/V	—	132	—	fs
		Kv = 225 ppm/V	—	150	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> All Diff Formats, 100 MHz ≤ F <sub>CLK</sub> < 200 MHz	φ <sub>J</sub>	Kv = 60 ppm/V	—	115	180	fs
		Kv = 75 ppm/V	—	118	—	fs
		Kv = 105 ppm/V	—	125	—	fs
		Kv = 150 ppm/V	—	138	—	fs
		Kv = 180 ppm/V	—	147	—	fs
		Kv = 225 ppm/V	—	165	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> LVDS, F <sub>CLK</sub> = 156.25 MHz	φ <sub>J</sub>	Kv = 60 ppm/V	—	110	130	fs
		Kv = 75 ppm/V	—	113	—	fs
		Kv = 105 ppm/V	—	120	—	fs
		Kv = 150 ppm/V	—	133	—	fs
		Kv = 180 ppm/V	—	142	—	fs
		Kv = 225 ppm/V	—	160	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> CMOS / Dual CMOS Formats	φ <sub>J</sub>	10 MHz ≤ F <sub>CLK</sub> < 250 MHz	—	200	—	fs

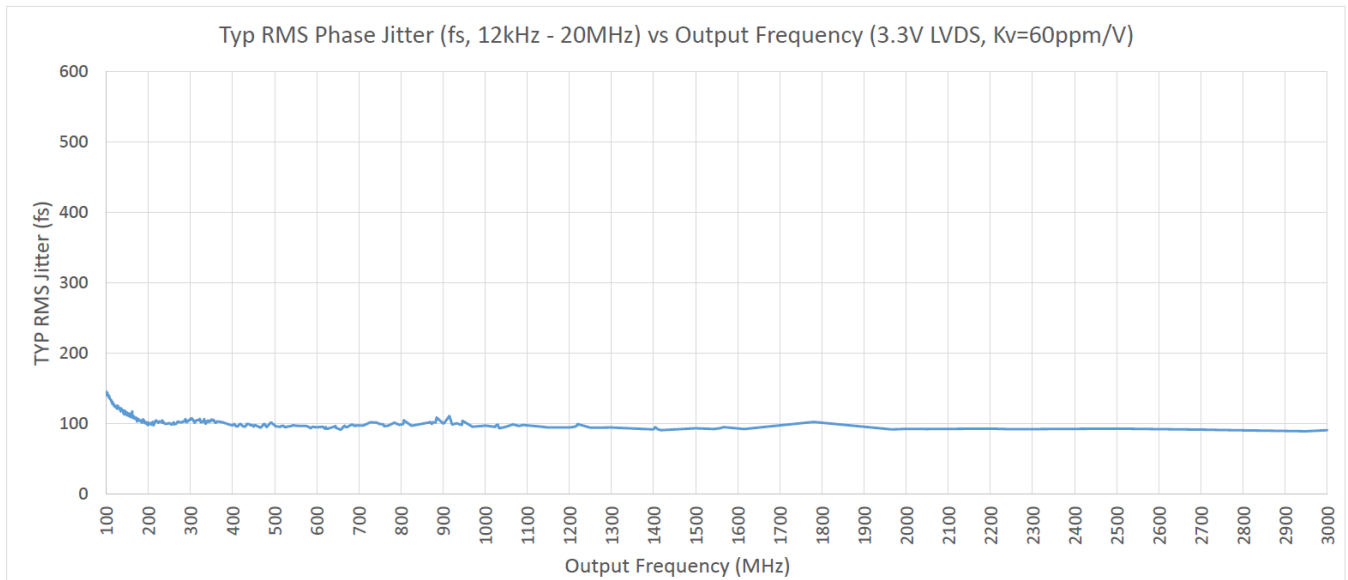
Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output	PSNR	100 kHz sine wave		-83		dBc
		200 kHz sine wave		-83		
		500 kHz sine wave		-82		
		1 MHz sine wave		-85		

**Note:**

1. Guaranteed by characterization. Jitter inclusive of any spurs.

**Table 2.4. 3.2 x 5 mm Clock Output Phase Noise (Typical)**

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	-73	-71	-60	dBc/Hz
1 kHz	-102	-102	-93	
10 kHz	-130	-128	-118	
100 kHz	-141	-139	-129	
1 MHz	-150	-148	-138	
10 MHz	-159	-160	-153	
20 MHz	-160	-162	-154	
Offset Frequency (f)	156.25 MHz LVPECL	200 MHz LVPECL	644.53125 MHz LVPECL	Unit
100 Hz	-72	-71	-60	dBc/Hz
1 kHz	-103	-101	-92	
10 kHz	-130	-127	-117	
100 kHz	-142	-139	-129	
1 MHz	-150	-148	-138	
10 MHz	-160	-162	-154	
20 MHz	-161	-162	-156	



**Figure 2.2. Phase Jitter vs. Output Frequency**

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at [www.silabs.com/oscillators](http://www.silabs.com/oscillators).

**Table 2.5. Environmental Compliance and Package Information**

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL): 3.2 x 5, 5 x 7 packages	1
Moisture Sensitivity Level (MSL): 2.5 x 3.2 package	2
Contact Pads: 3.2x5, 5x7 packages	Au/Ni (0.3 - 1.0 $\mu\text{m}$ / 1.27 - 8.89 $\mu\text{m}$ )
Contact Pads: 2.5x3.2 packages	Au/Pd/Ni (0.03 - 0.12 $\mu\text{m}$ / 0.1 - 0.2 $\mu\text{m}$ / 3.0 - 8.0 $\mu\text{m}$ )
<b>Note:</b>	
1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: <a href="http://www.silabs.com/sup-port/quality/Pages/RoHSInformation.aspx">www.silabs.com/sup-port/quality/Pages/RoHSInformation.aspx</a> .	

**Table 2.6. Thermal Conditions<sup>1</sup>**

Max Junction Temperature = 125° C

Package	Parameter	Symbol	Test Condition	Value	Unit
2.5 x 3.2 mm 6-pin DFN <sup>2</sup>	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	72	°C/W
	Thermal Parameter Junction to Board	$\Psi_{JB}$	Still Air, 85 °C	38	°C/W
	Thermal Parameter Junction to Top Center	$\Psi_{JT}$	Still Air, 85 °C	15	°C/W
3.2 x 5 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	55	°C/W
	Thermal Parameter Junction to Board	$\Psi_{JB}$	Still Air, 85 °C	20	°C/W
	Thermal Parameter Junction to Top Center	$\Psi_{JT}$	Still Air, 85 °C	20	°C/W
5 x 7 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	53	°C/W
	Thermal Parameter Junction to Board	$\Psi_{JB}$	Still Air, 85 °C	26	°C/W
	Thermal Parameter Junction to Top Center	$\Psi_{JT}$	Still Air, 85 °C	26	°C/W
<b>Note:</b>					
1. Based on PCB Dimensions: 4.5" x 7", PCB Thickness: 1.6 mm, Number of Cu Layers: 4.					
2. For best 2.5x3.2mm thermal performance, use 2 GND vias as shown in the <a href="#">Si5xxUC-EVB</a> eval board layout					



**Table 2.7. Absolute Maximum Ratings<sup>1</sup>**

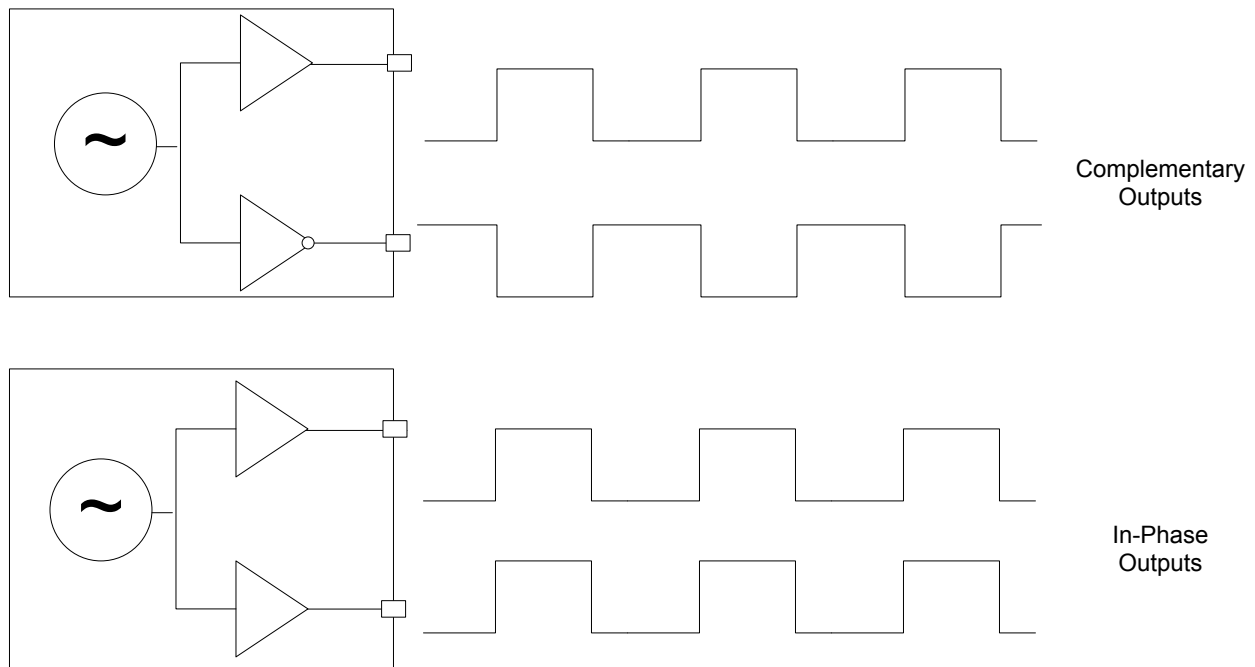
Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	$T_{AMAX}$	95	°C
Storage Temperature	$T_S$	-55 to 125	°C
Supply Voltage	$V_{DD}$	-0.5 to 3.8	°C
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.3$	V
ESD HBM (JESD22-A114)	HBM	2.0	kV
Solder Temperature <sup>2</sup>	$T_{PEAK}$	260	°C
Solder Time at $T_{PEAK}$ <sup>2</sup>	$T_P$	20–40	sec

**Notes:**

- Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020.

### 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple VCXOs with a single Si565 device.



**Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs**

### 4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

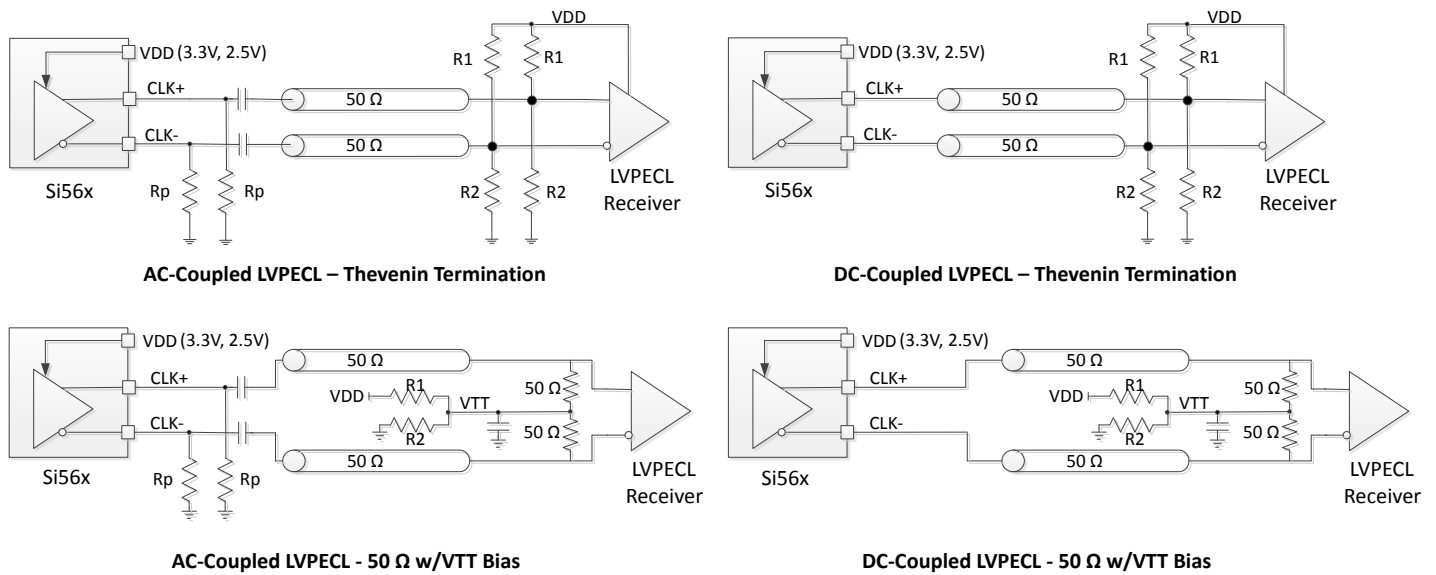


Figure 4.1. LVPECL Output Terminations

AC-Coupled LVPECL Termination Resistor Values				DC-Coupled LVPECL Termination Resistor Values		
VDD	R1	R2	Rp	VDD	R1	R2
3.3 V	127 Ω	82.5 Ω	130 Ω	3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω	90 Ω	2.5 V	250 Ω	62.5 Ω



## 5. Package Outline

### 5.1 Package Outline (5x7 mm)

The figure below illustrates the package details for the 5x7 mm Si565. The table below lists the values for the dimensions shown in the illustration.

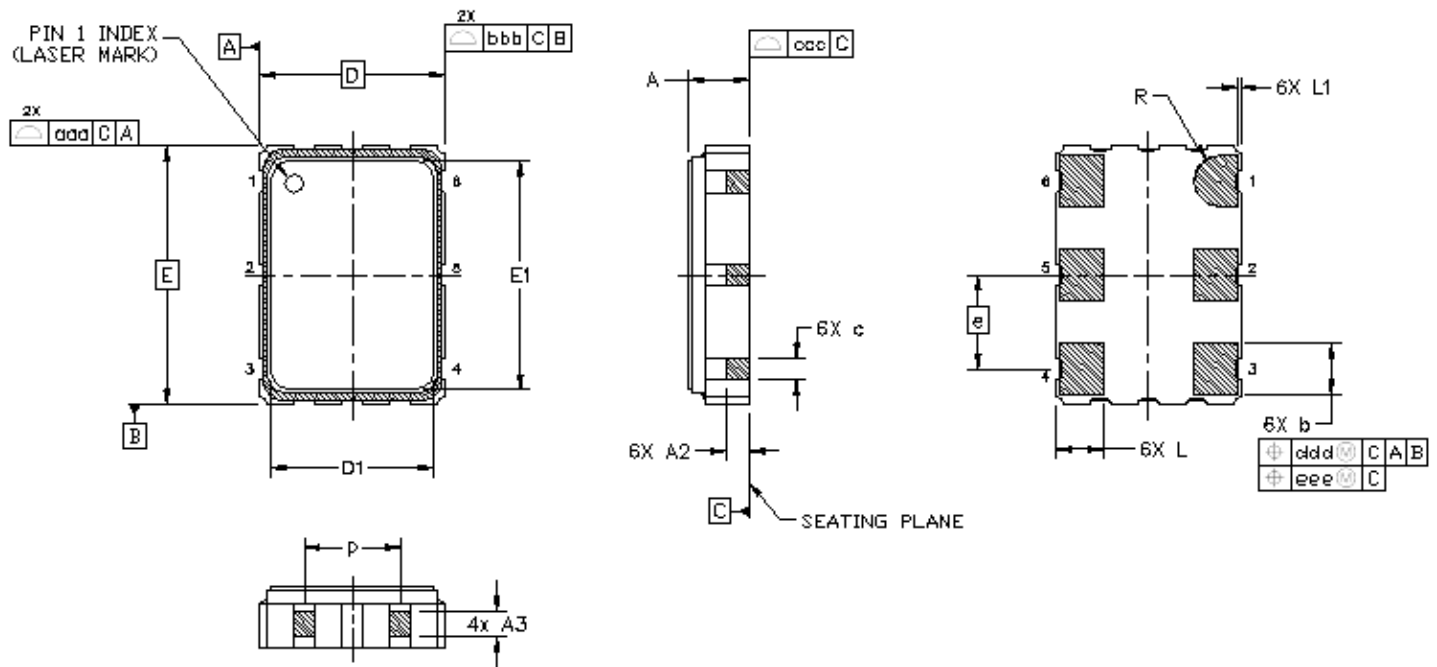


Figure 5.1. Si565 (5x7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

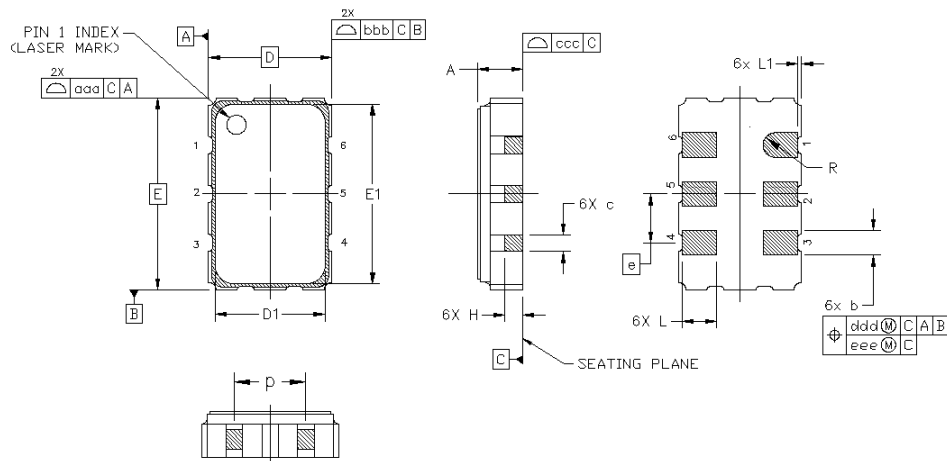
Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.13	1.28	1.43	L	1.17	1.27	1.37
A2	0.50	0.55	0.60	L1	0.05	0.10	0.15
A3	0.50	0.55	0.60	p	1.70	—	1.90
b	1.30	1.40	1.50	R	0.70 REF		
c	0.50	0.60	0.70	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.30	4.40	4.50	ccc	0.08		
e	2.54 BSC			ddd	0.10		
E	7.00 BSC			eee	0.05		
E1	6.10	6.20	6.30				

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si565. The table below lists the values for the dimensions shown in the illustration.



**Figure 5.2. Si565 (3.2×5 mm) Outline Diagram**

**Table 5.2. Package Diagram Dimensions (mm)**

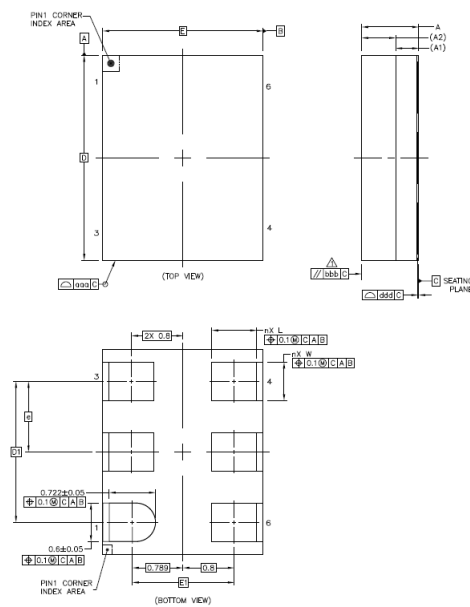
Dimension	Min	Nom	Max
A	1.06	1.17	1.33
b	0.54	0.64	0.74
c	0.35	0.45	0.55
D	3.20 BSC		
D1	2.55	2.60	2.65
e	1.27 BSC		
E	5.00 BSC		
E1	4.35	4.40	4.45
H	0.45	0.55	0.65
L	0.80	0.90	1.00
L1	0.05	0.10	0.15
p	1.36	1.46	1.56
R	0.32 REF		
aaa	0.15		
bbb	0.15		
ccc	0.08		
ddd	0.10		
eee	0.05		

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

### 5.3 Package Outline (2.5x3.2 mm)

The figure below illustrates the package details for the 2.5x3.2 mm Si565. The table below lists the values for the dimensions shown in the illustration.



**Figure 5.3. Si565 (2.5x3.2 mm) Outline Diagram**

**Table 5.3. Package Diagram Dimensions (mm)**

Dimension	Min	Nom	Max
A	0.90	0.95	1.00
A1		0.36 REF	
A2		0.53 REF	
W	0.55	0.60	0.65
D		3.2 BSC	
E		2.5 BSC	
e		1.10 BSC	
L	0.65	0.70	0.75
n		5	
D1		2.2 BSC	
E1		1.589 BSC	
aaa		0.10	
bbb		0.10	
ddd		0.08	

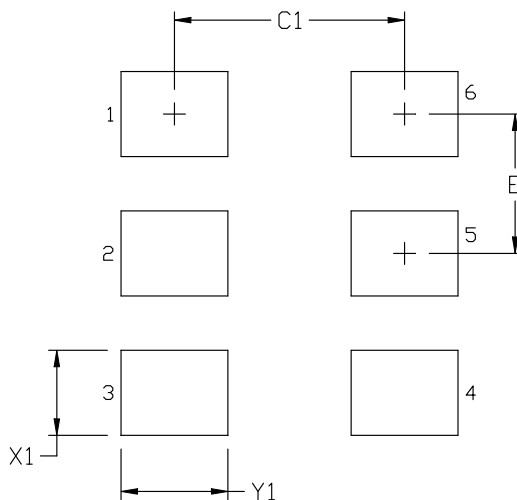
**Notes:**

1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 6. PCB Land Pattern

### 6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si565. The table below lists the values for the dimensions shown in the illustration.



**Figure 6.1. Si565 (5×7 mm) PCB Land Pattern**

**Table 6.1. PCB Land Pattern Dimensions (mm)**

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

#### Notes:

##### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

##### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

##### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

##### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



## 6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si565. The table below lists the values for the dimensions shown in the illustration.

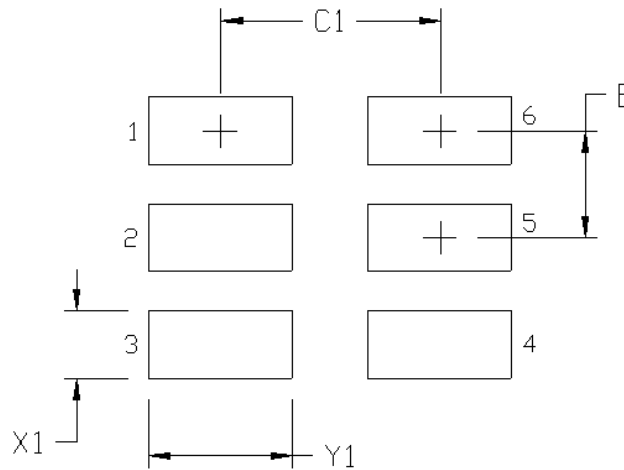


Figure 6.2. Si565 (3.2×5 mm) PCB Land Pattern

Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

### Notes:

#### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

#### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

#### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.3 PCB Land Pattern (2.5×3.2 mm)

The figure below illustrates the 2.5×3.2 mm PCB land pattern for the Si565. The table below lists the values for the dimensions shown in the illustration.

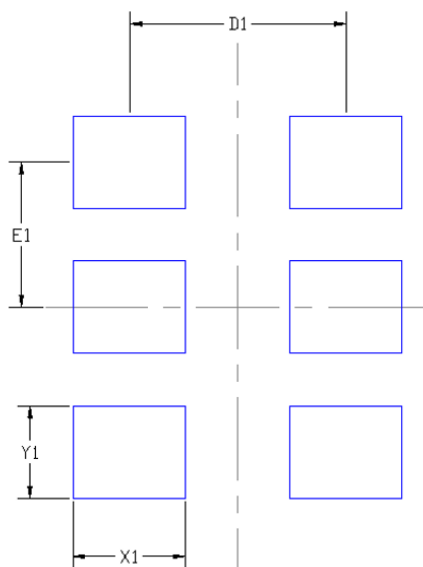


Figure 6.3. Si565 (2.5×3.2 mm) PCB Land Pattern

Table 6.3. PCB Land Pattern Dimensions (mm)

Dimension	Description	Value (mm)
X1	Width - leads on long sides	0.85
Y1	Height - leads on long sides	0.7
D1	Pitch in X directions of XLY1 leads	1.639
E1	Lead pitch XLY1 leads	1.10

**Notes:** The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

#### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

#### Stencil Design

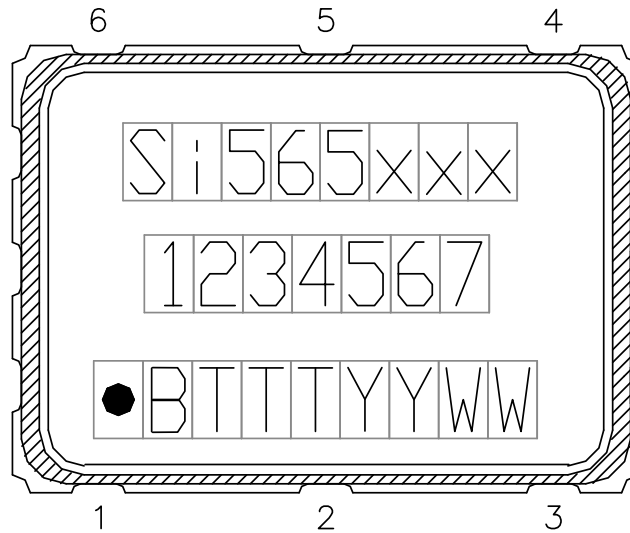
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

#### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. Top Marking (5x7 and 3.2x5 Packages)

The figure below illustrates the mark specification for the Si565 5x7 and 3.2x5 package sizes. The table below lists the line information.



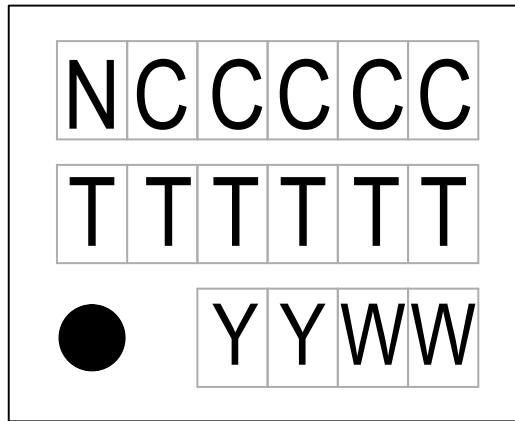
**Figure 7.1. Mark Specification**

**Table 7.1. Si565 Top Mark Description**

Line	Position	Description
1	1–8	"Si565", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si565AAA)
2	1–7	Frequency Code (e.g. 100M000 or 6-digit custom code as described in the Ordering Guide)
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (B)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

## 8. Top Marking (2.5x3.2 Package)

The figure below illustrates the mark specification for the Si565 2.5x3.2 package sizes. The table below lists the line information.



**Figure 8.1. Mark Specification**

**Table 8.1. Si565 Top Mark Description**

Line	Position	Description
1	1–6	N = Si565, CCCCC = Custom Mark Code
2	<b>Trace Code</b>	
	1–6	Six-digit trace code per assembly release instructions
3	Position 1	Pin 1 orientation mark (dot)
	Position 2–3	Year (last two digits of the year), to be assigned by assembly site (exp: 2017 = 17)
	Position 4–5	Calendar Work Week number (1–53), to be assigned by assembly site

## 9. Revision History

### Revision 1.2

September, 2020

- Added 2.5 x 3.2 mm package option.
- Updated Table 2.2, Powerup VDD Ramp Rate and LVDS Swing.

### Revision 1.0

June, 2018

- Initial draft



# SKYWORKS®

## ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

[www.skyworksinc.com/CBPro](http://www.skyworksinc.com/CBPro)



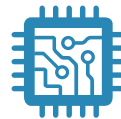
**Portfolio**

[www.skyworksinc.com/ia/timing](http://www.skyworksinc.com/ia/timing)



**SW/HW**

[www.skyworksinc.com/CBPro](http://www.skyworksinc.com/CBPro)



**Quality**

[www.skyworksinc.com/quality](http://www.skyworksinc.com/quality)



**Support & Resources**

[www.skyworksinc.com/support](http://www.skyworksinc.com/support)

### Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, Clockbuilder®, DSPLL®, ISOModem®, ProSLIC®, and SiPHY® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at [www.skyworksinc.com](http://www.skyworksinc.com), are incorporated by reference.

Skyworks Solutions, Inc. | Nasdaq: SWKS | [sales@skyworksinc.com](mailto:sales@skyworksinc.com) | [www.skyworksinc.com](http://www.skyworksinc.com)

USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540 |    