Freescale Semiconductor
Technical Data

Document Number: MMRF1024HS
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√RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 50 W asymmetrical Doherty RF power LDMOS transistor is optimized for instantaneous signal bandwidth capabilities covering the frequency range of 2496 to 2690 MHz. This part is ideally suited for commercial and defense communications and electronic warfare applications, such as an IED jammer.

2600 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.4 Vdc, P_{out} = 50 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

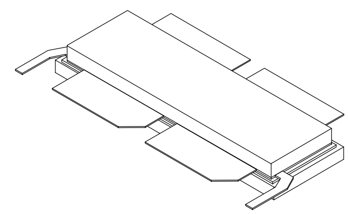
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	14.1	44.6	8.1	–31.5
2590 MHz	14.4	44.9	8.1	–33.8
2690 MHz	14.2	44.2	7.9	–37.6

Features

- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

MMRF1024HS

2496–2690 MHz, 50 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-1230S-4L2L

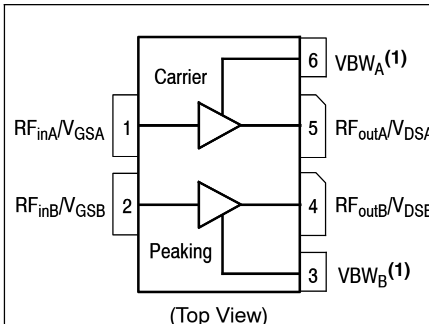


Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	294 1.7	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 50 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.4 Vdc, 2590 MHz	$R_{\theta JC}$	0.42	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	B, passes 250 V
Charge Device Model (per JESD22-C101)	IV, passes 1200 V

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (3)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (Carrier) (3)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 700 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 6 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics - Side B (Peaking) (3)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 6 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
3. Each side of device measure separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.4 Vdc, P_{out} = 50 W Avg., f = 2496 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	13.0	14.1	16.0	dB
Drain Efficiency	η_D	41.0	44.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.4	8.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	–31.5	–29.0	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 700 mA, f = 2590 MHz					
VSWR 10:1 at 32 Vdc, 335 W[3] CW Output Power (2 dB Input Overdrive from 230 W CW Rated Power)	No Device Degradation				
Typical Performance [2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.4 Vdc, 2496–2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	230	—	W
P_{out} @ 3 dB Compression Point [4]	P3dB	—	320	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range)	Φ	—	–22	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	110	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 50 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.002	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) [3]	ΔP1dB	—	0.006	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
MMRF1024HSR5	R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

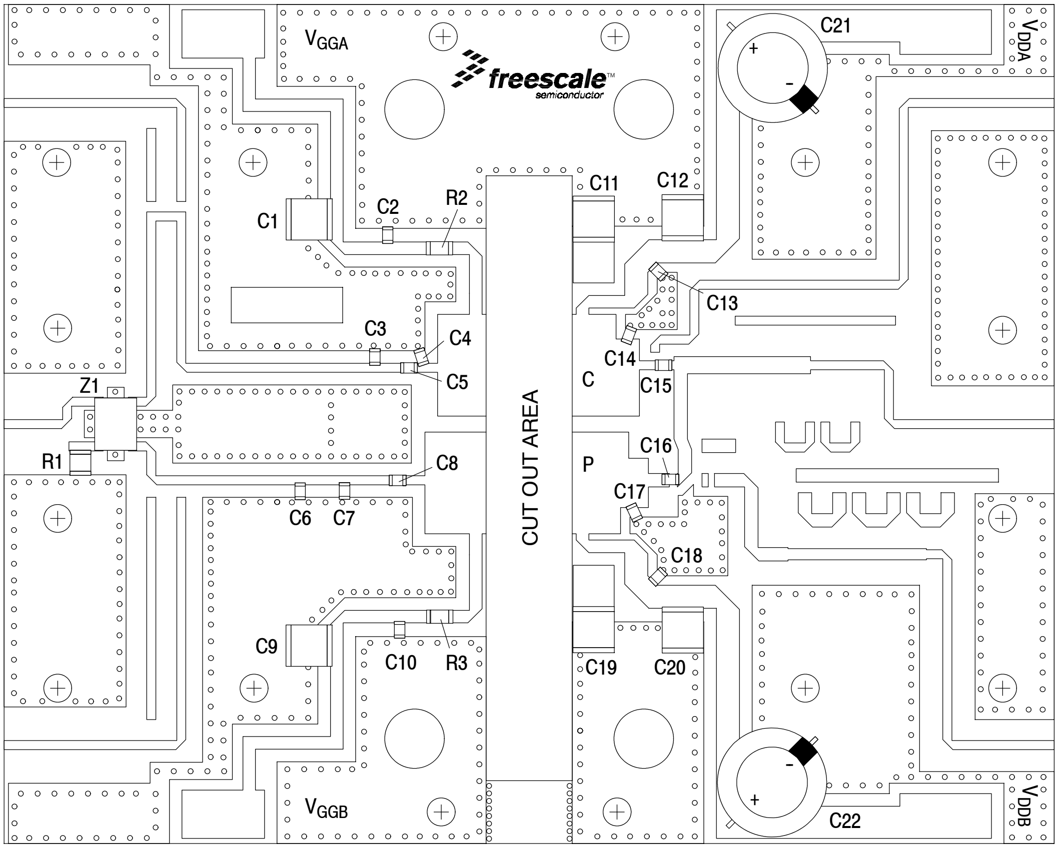


Figure 2. MMRF1024HS Test Circuit Component Layout

Table 6. MMRF1024HS Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C11, C12, C19, C20	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C5, C8, C10, C13, C18	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C3, C4	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C6, C7	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C14	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
C15	2.0 pF Chip Capacitor	ATC600F2R0BT250XT	ATC
C16	10 pF Chip Capacitor	ATC600F100JT250XT	ATC
C17	0.9 pF Chip Capacitor	ATC600F0R9BT250XT	ATC
C21, C22	220 μF Electrolytic Capacitors	227CKS050M	Illinois Capacitor
R1	50 Ω, 4 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	2.0 Ω, 1/4 W Chip Resistors	CRCW12062R00JNEA	Vishay
Z1	2300–2700 MHz Band, 5 dB Directional Coupler	X3C25P1-05S	Anaren
PCB	Rogers RO4305B, 0.020″, $\varepsilon_r = 3.66$	—	MTL

TYPICAL CHARACTERISTICS

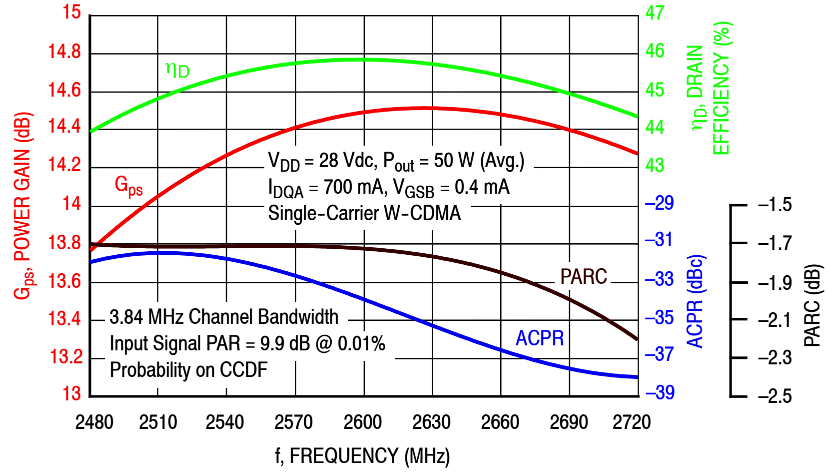


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

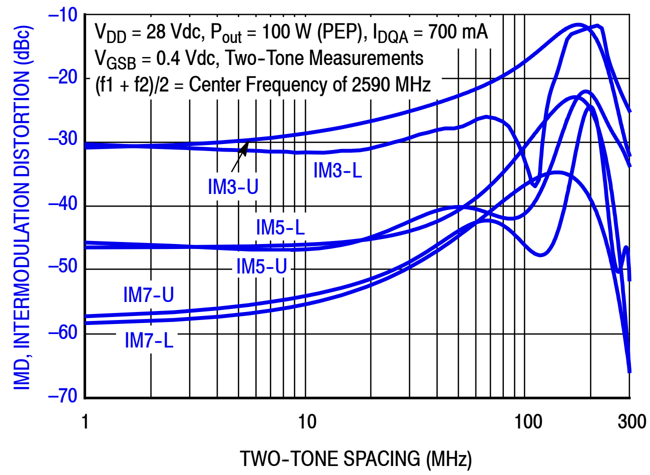


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

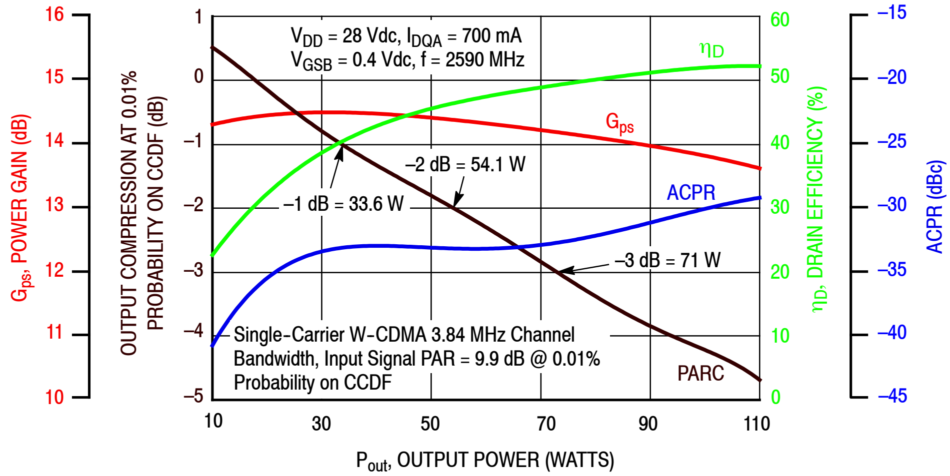


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

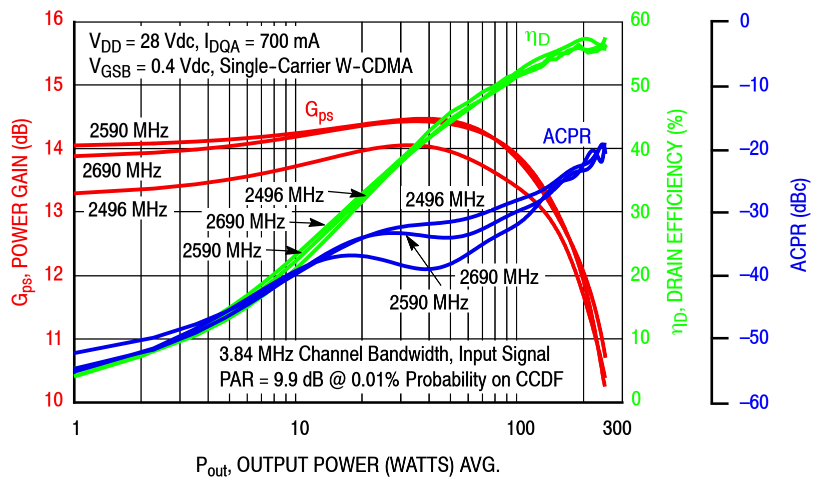


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

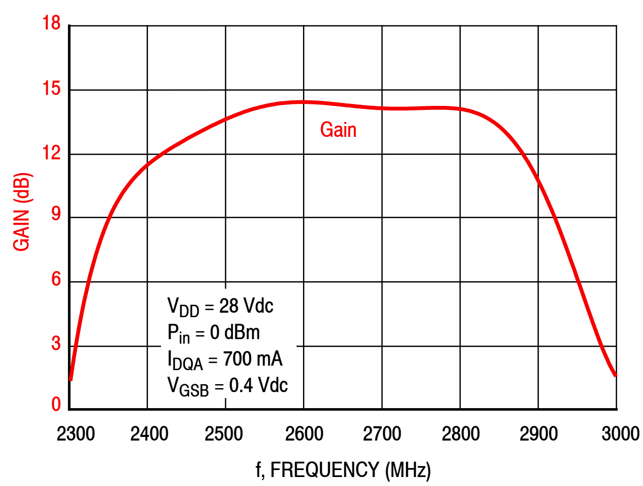


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 689 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.07 - j10.7	4.00 + j9.61	2.03 - j4.57	17.4	51.8	151	54.1	-13
2590	7.57 - j11.9	6.72 + j10.7	2.00 - j4.75	17.6	51.7	147	53.2	-12
2690	15.7 - j9.50	12.9 + j8.73	2.00 - j5.11	17.6	51.6	143	52.4	-13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.07 - j10.7	3.92 + j10.2	1.92 - j4.78	15.2	52.5	179	54.9	-17
2590	7.57 - j11.9	7.03 + j11.7	1.91 - j4.97	15.3	52.4	174	53.6	-17
2690	15.7 - j9.50	14.9 + j9.37	1.92 - j5.34	15.3	52.3	170	52.4	-17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

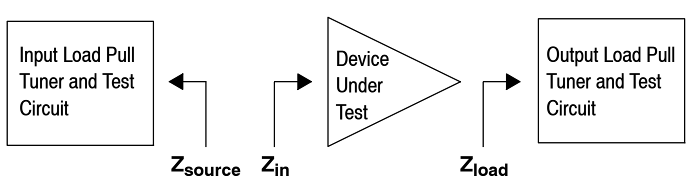
V_{DD} = 28 Vdc, I_{DQA} = 689 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.07 - j10.7	4.07 + j10.0	4.82 - j3.58	19.7	49.9	97	64.0	-19
2590	7.57 - j11.9	6.62 + j11.4	3.74 - j2.51	20.0	49.6	92	62.6	-21
2690	15.7 - j9.50	13.3 + j9.45	3.36 - j2.87	19.9	49.5	90	61.2	-20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.07 - j10.7	3.77 + j10.6	4.53 - j2.90	17.8	50.4	111	64.0	-28
2590	7.57 - j11.9	6.80 + j12.2	3.67 - j2.58	18.0	50.3	108	62.7	-29
2690	15.7 - j9.50	15.2 + j9.96	3.36 - j2.87	17.9	50.2	105	61.2	-28

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 0.4 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	3.33 - j9.36	3.00 + j9.43	2.00 - j5.09	12.1	53.2	209	54.4	-22
2590	4.98 - j10.4	5.22 + j10.6	2.11 - j5.43	12.2	53.1	203	53.8	-22
2690	10.9 - j8.12	11.3 + j9.48	2.35 - j6.10	12.1	52.9	196	52.8	-20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	3.33 - j9.36	3.14 + j9.86	1.99 - j5.35	9.9	53.9	243	54.3	-28
2590	4.98 - j10.4	5.76 + j11.2	2.11 - j5.74	10.0	53.7	236	53.0	-28
2690	10.9 - j8.12	13.0 + j9.24	2.40 - j6.29	10.0	53.5	226	52.5	-26

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

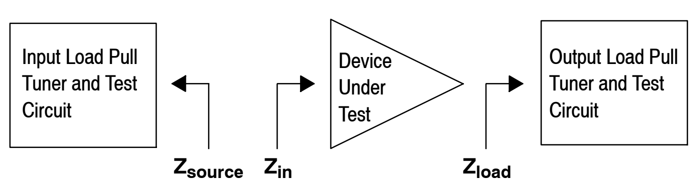
V_{DD} = 28 Vdc, V_{GSB} = 0.4 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	3.33 - j9.36	2.65 + j9.45	4.22 - j3.35	13.3	51.6	144	64.3	-30
2590	4.98 - j10.4	4.64 + j10.7	3.57 - j3.41	13.4	51.6	145	63.8	-30
2690	10.9 - j8.12	10.5 + j10.4	3.29 - j3.86	13.1	51.6	143	62.4	-27

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	3.33 - j9.36	2.81 + j9.82	3.97 - j3.62	11.2	52.3	171	64.6	-38
2590	4.98 - j10.4	5.16 + j11.3	3.50 - j3.54	11.3	52.2	167	63.7	-38
2690	10.9 - j8.12	12.3 + j10.3	3.17 - j3.92	11.1	52.1	163	61.8	-35

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

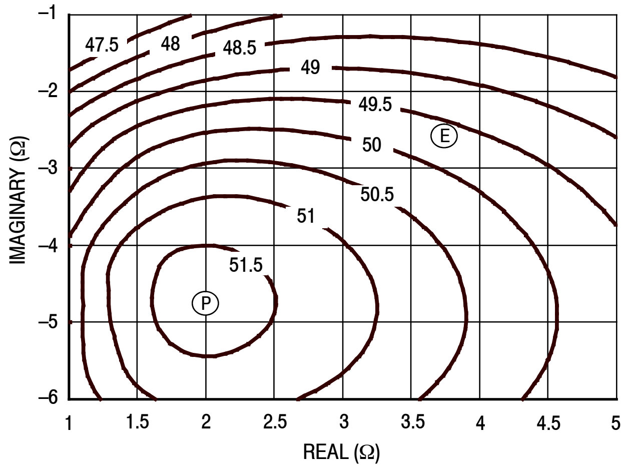


Figure 12. P1dB Load Pull Output Power Contours (dBm)

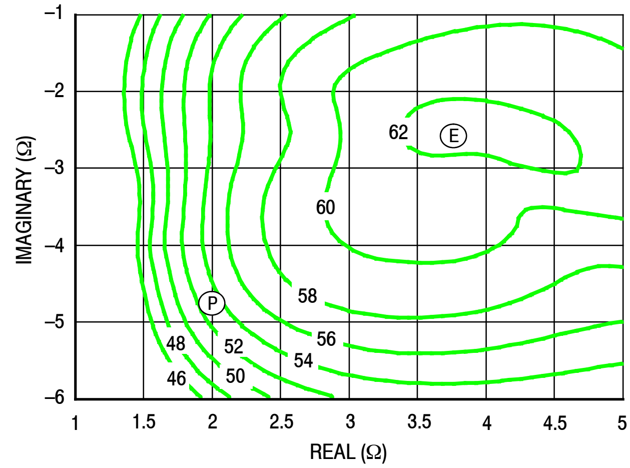


Figure 13. P1dB Load Pull Efficiency Contours (%)

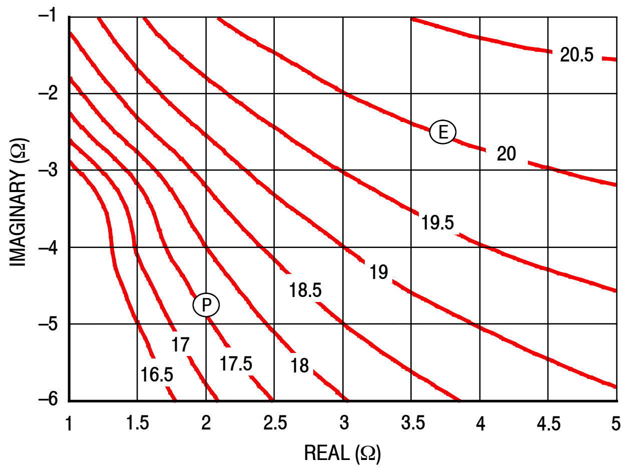


Figure 14. P1dB Load Pull Gain Contours (dB)

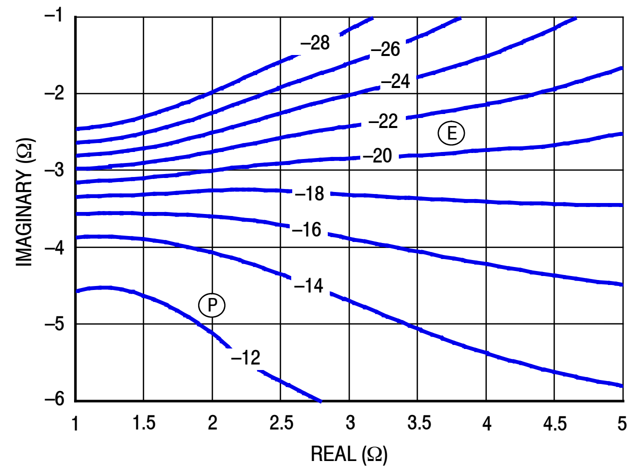


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

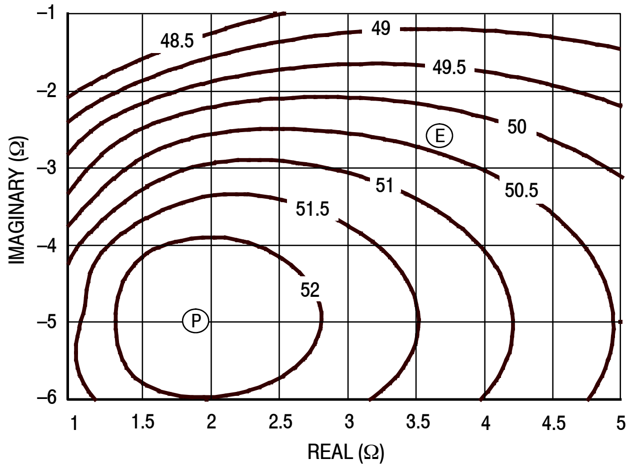


Figure 16. P3dB Load Pull Output Power Contours (dBm)

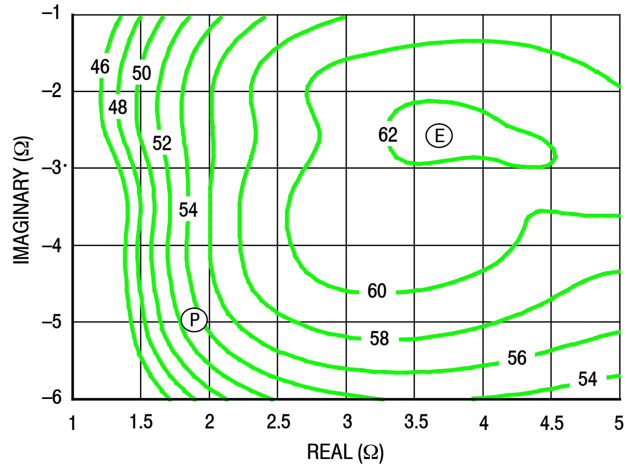


Figure 17. P3dB Load Pull Efficiency Contours (%)

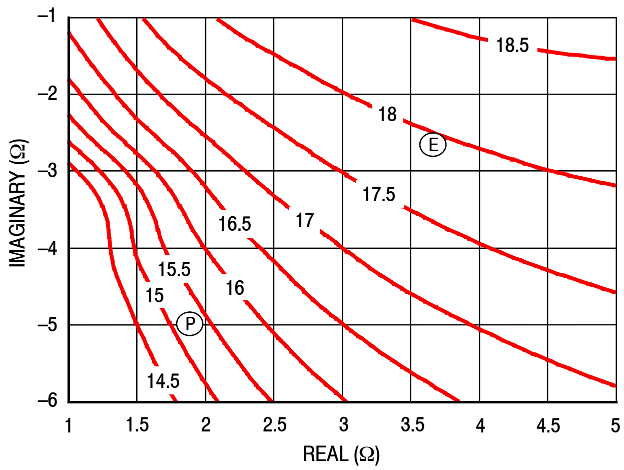


Figure 18. P3dB Load Pull Gain Contours (dB)

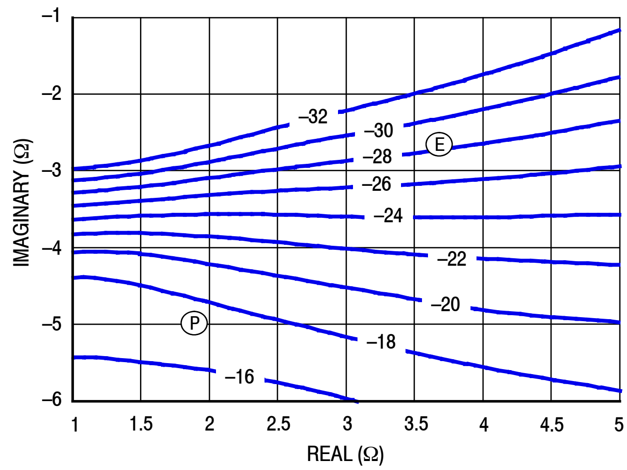


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

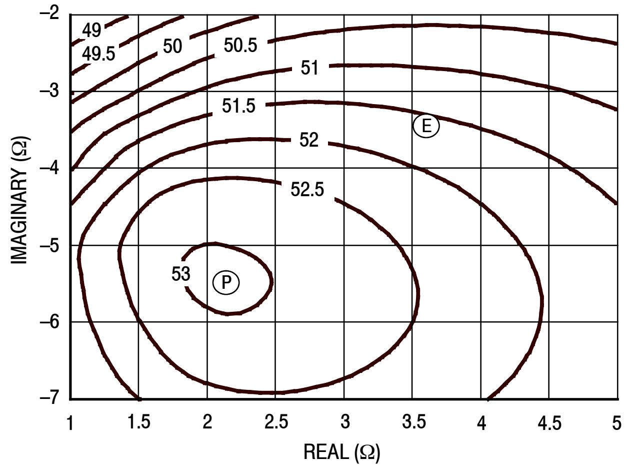


Figure 20. P1dB Load Pull Output Power Contours (dBm)

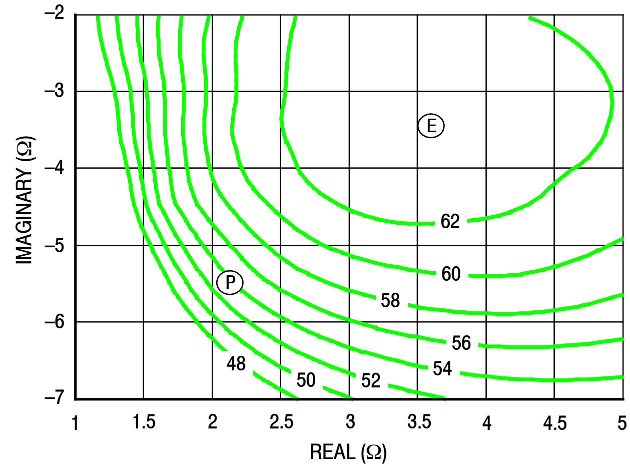


Figure 21. P1dB Load Pull Efficiency Contours (%)

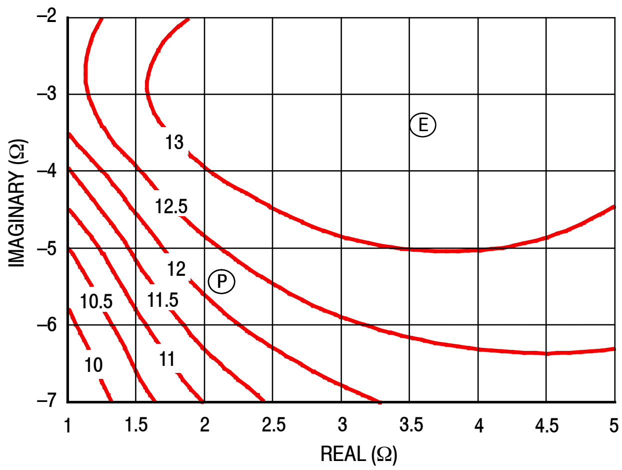


Figure 22. P1dB Load Pull Gain Contours (dB)

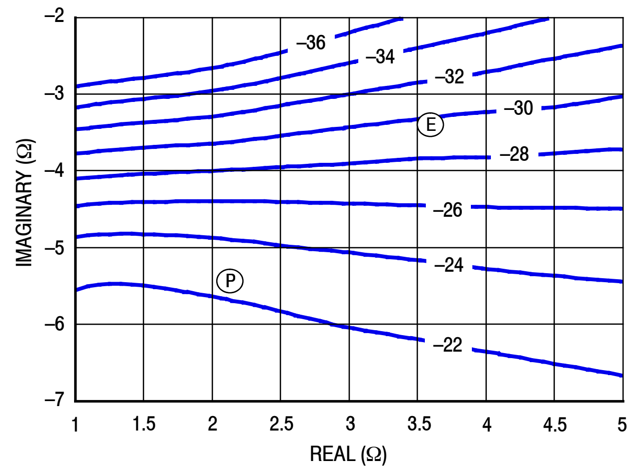


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

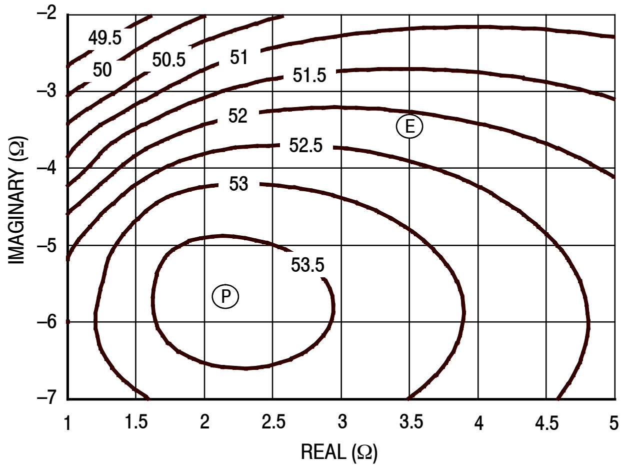


Figure 24. P3dB Load Pull Output Power Contours (dBm)

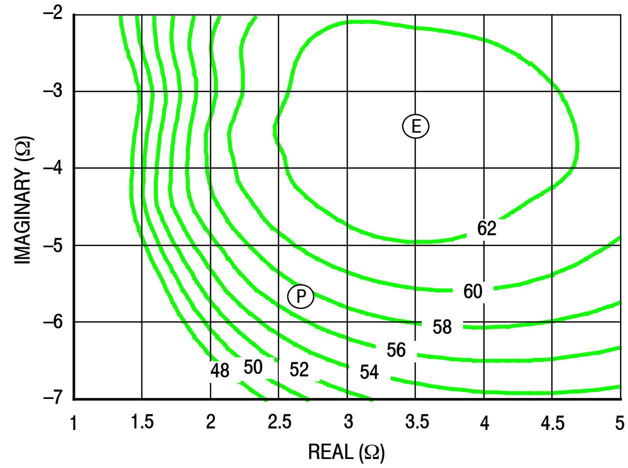


Figure 25. P3dB Load Pull Efficiency Contours (%)

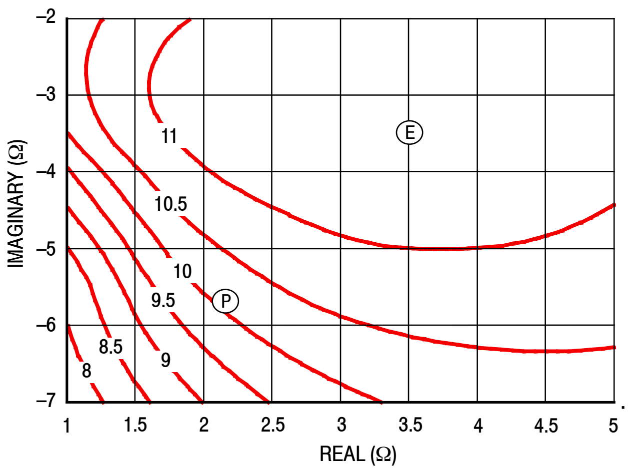


Figure 26. P3dB Load Pull Gain Contours (dB)

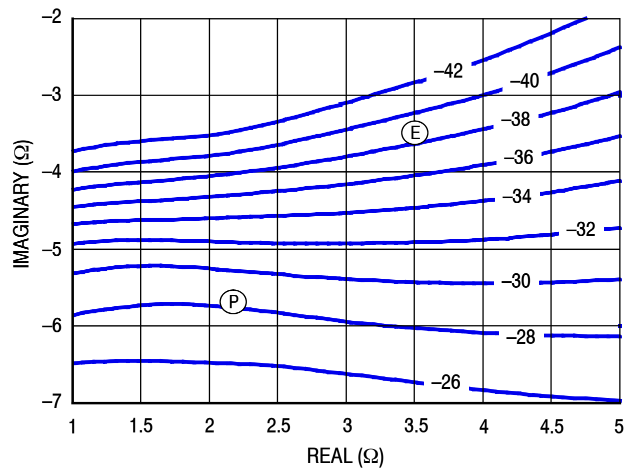


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

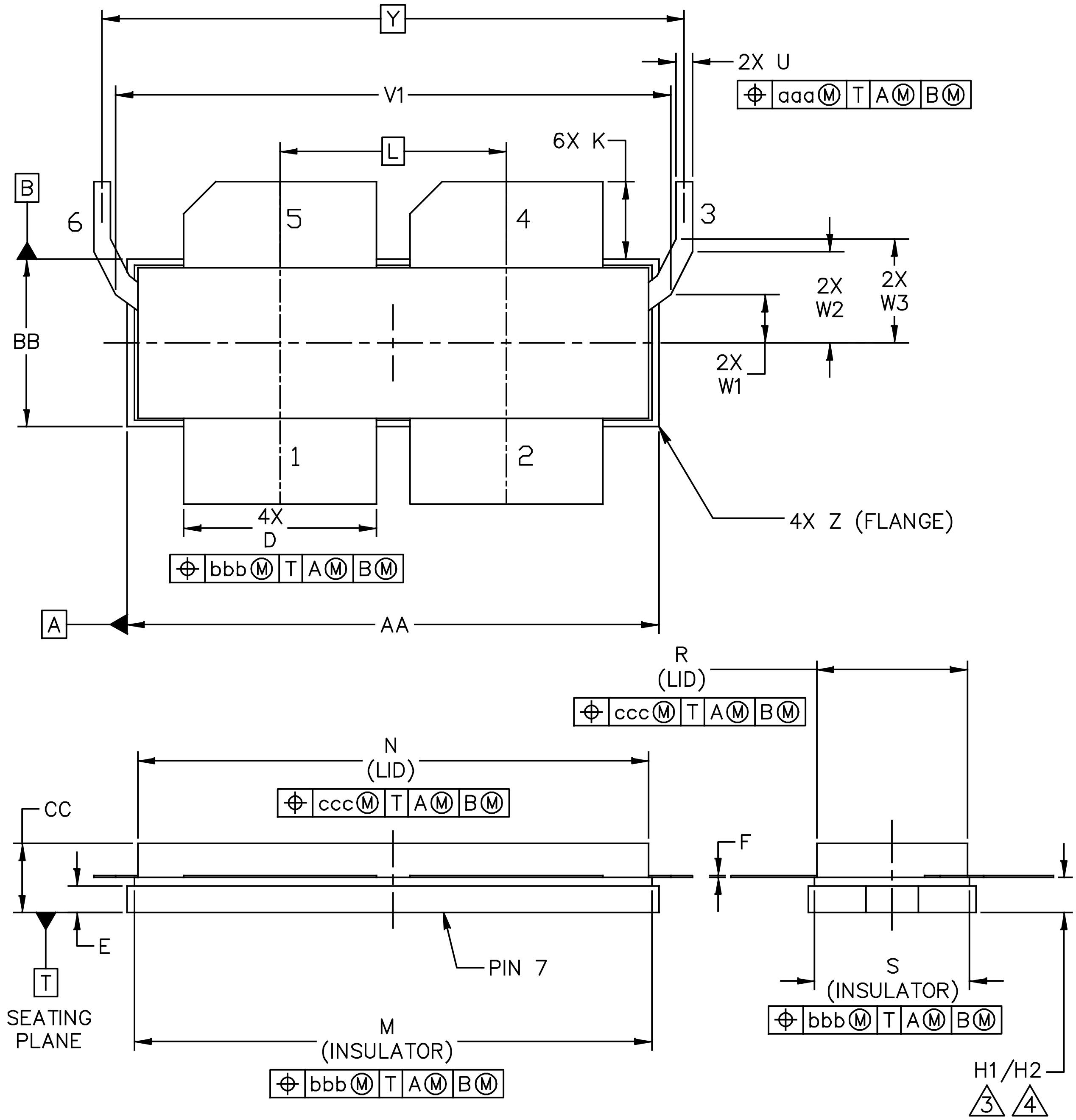
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

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PRODUCT DOCUMENTATION

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2016	• Initial Release of Data Sheet

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