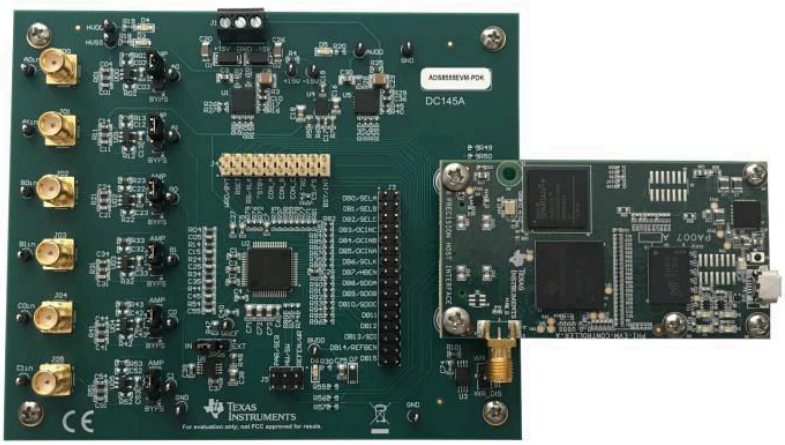
User's Guide

ADS8555EVM-PDK Evaluation Module

ABSTRACT



This user's guide describes the operation and use of the ADS8555 evaluation module (EVM). The ADS8555 is a 6-channel, simultaneous sampling, 16-bit successive approximation (SAR) analog-to-digital converter (ADC). Each input channel on the device can support true bipolar input ranges up to ±12 V. The device includes a programmable, internally buffered voltage reverence. The ADC includes a serial programming interface (SPI) interface and a parallel interface (word and byte mode) for data communication. Device configuration is achieved through simple static digital input pins (hardware mode) or through communications to the SPI interface (control register configuration in software mode). This user's guide covers the circuit description, schematic diagram, and bill of materials for the ADS8555 circuit board. This EVM hardware and software can also be used to support the ADS8556, ADS8557, and ADS8558 devices from this family. Other devices can be tested by desoldering the ADC and reprogramming the EVM (see Section 6.3). Detailed instructions for using other family members are provided later in this document.

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1 ADS8555EVM-PDK Overview

This document describes how to connect the EVM to your computer and test equipment to evaluate device performance and understand device features. The document also describes how to install and use the associated evaluation module software.

1.1 ADS8555EVM-PDK Features

Figure 1-1 shows the proper component connection for the ADS8555EVM. The ADS8555 evaluation module kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8555 ADC.
- Digital and analog interface power with universal serial bus (USB) power. External power is required for the high-voltage ±15-V supply.
- Easy-to-use evaluation software for the 64-bit Microsoft® Windows®7, Windows® 8, and Windows® 10 operating systems.
- Precision host interface (PHI) controller translates the USB (2.0) or higher to parallel or serial digital communications.

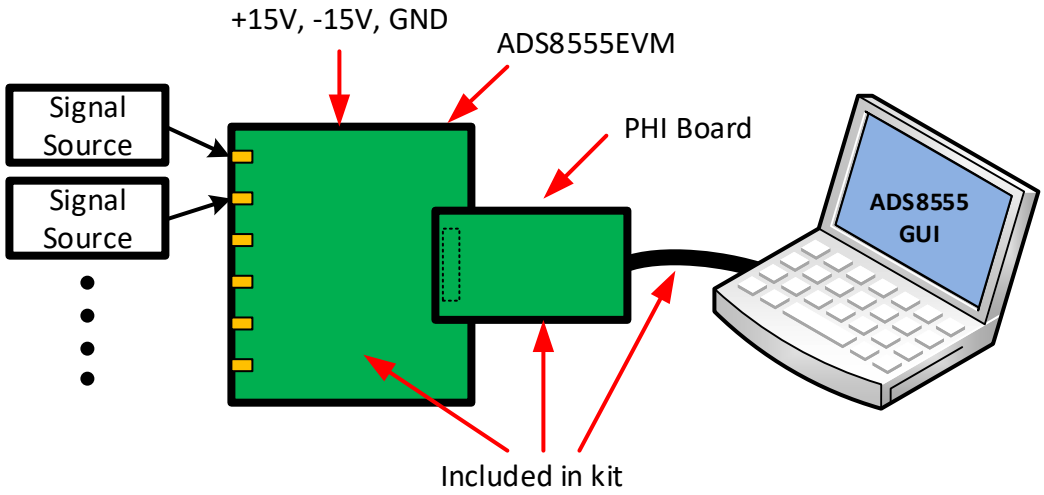

Figure 1-1. System Connection for Evaluation

1.2 ADS8555EVM Features

- Six input channels connected to external single-ended signals that are source applied to subminiature version A (SMA) connectors or headers.
- Serial and parallel interface connects to the PHI controller via a 60-pin connector (J2).
- High-voltage power supplies (HVDD and HVSS) are not included. Connect common lab supplies via screw terminal J1.
- Analog low-voltage supplies (AVDD = 5 V) are generated using an external 15-V supply and a low-dropout regulator (LDO). HVDD (12-V supply) is also generated using the 15-V supply and an LDO. HVSS (–12-V supply) is generated using the –15-V supply and an LDO.
- Digital low-voltage supply (DVDD = 3.3 V) is generated using USB power from the PHI controller.
- Integrated or external voltage reference options are available.

2 EVM Analog Interface

The ADS8555EVM is an evaluation module built using a two-board modular EVM system. One board is a digital controller (PHI), and the other board contains the ADC and associated analog circuitry. Both boards and the associated cables form the ADS8555EVM-PDK.

2.1 ADC Supply, Input, Voltage Reference, and Digital Connections

Figure 2-1 shows the decoupling on AVDD, BVDD, HVDD, and HVSS and the voltage reference. The decoupling capacitors match the recommendations in the ADS8555 data sheet. The layout (see Figure 7-1) uses the shortest possible connections to the decoupling capacitors and connects the ground end to the GND plane using vias. The ADS8555 can use an external or internal voltage reference. This reference can be selected by changing the position of JP06 to *INT* for internal or *EXT* for external. Figure 2-1 also shows the analog input signal and digital signal connections.

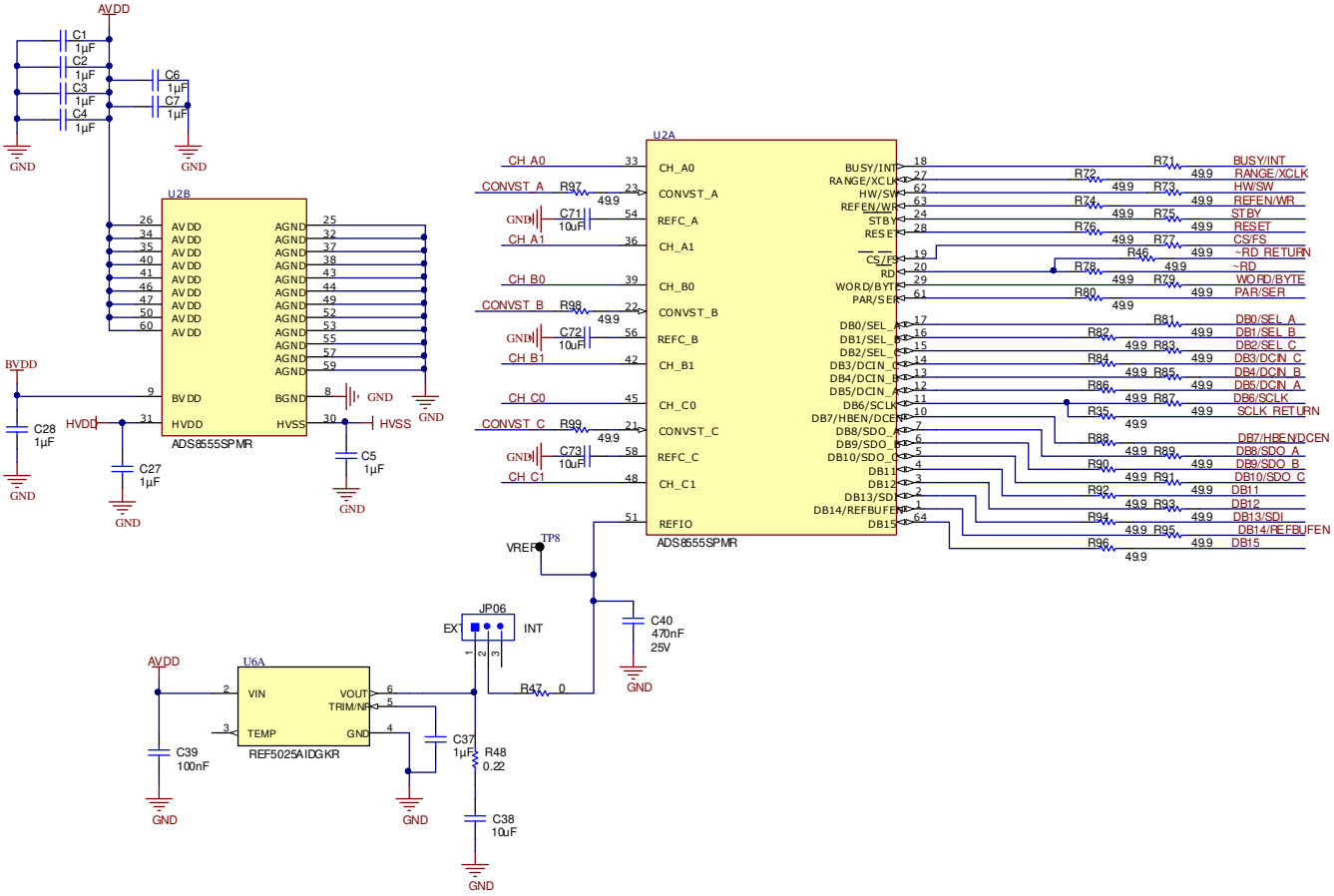

Figure 2-1. ADC Signal and Supply Connection

2.2 ADC Amplifier Drive

Figure 2-2 shows the op amp configuration for each ADC drive input. The default configuration is a noninverting buffer configuration. The gain of this circuit can be adjusted by changing R03 and R02 as needed. C02 can be used to limit the amplifier bandwidth or compensate the amplifier. R01 and C01 can also be used to create a low-pass filter. Jumper JP00 can be used to completely bypass the amplifier. This diagram only shows one channel, but this circuit is repeated six times. For other channels, see Figure 7-2.

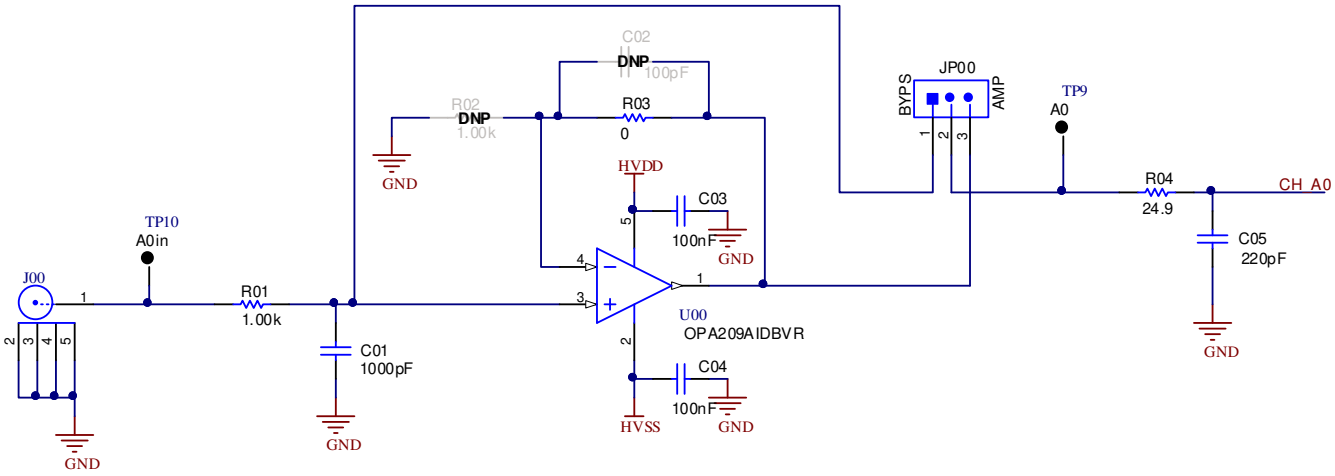

Figure 2-2. Amplifier Drive Circuit

3 Digital Interface

As noted in Section 1.1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8555 ADC (over SPI or parallel) and the EEPROM (over I^2C). The electrically erasable programmable read-only memory (EEPROM) comes preprogrammed with the information required to configure and initialize the ADS8555 platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 Parallel Interface

The parallel interface signals are generated on the PHI controller and are connected through J2. Each of these signals has a 47-Ω resistor between the device and the controller to slow down the signal edges in order to minimize signal overshoot. The digital signals can be monitored on the J3, J4, and J5 test headers.

3.2 Serial Interface (SPI)

The ADS8555 ADC uses SPI serial communication in mode 1 (CPOL = 0 and CPHA= 1). Because the serial clock (SCLK) frequency can be as fast as 36 MHz, the ADS8555EVM offers 47-Ω resistors between the controller and device to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

3.3 I^2C Bus and EEPROM

The circuit shown in Figure 3-1 is used with the EVM controller (PHI) for EVM identification. This circuit is not required by the ADS8555 for operation. The switch (S1) is write protected and does not need to be changed for EVM operation.

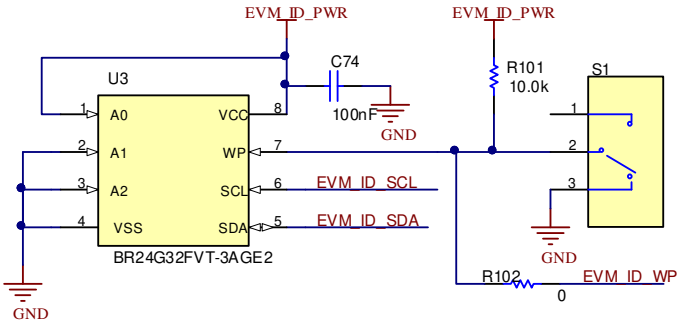

Figure 3-1. I^2C Bus and EEPROM

3.4 Connections to the PHI Connector

Connector J2 is used to connect the PHI digital controller printed circuit board (PCB) to the ADS8555EVM. This connector has all the digital signals as well as the BVDD supply. The power for the BVDD supply is from the USB connection. This connector also provides I^2C signals that are used on the EEPROM identification circuit. The digital signals can be monitored on the J3, J4, and J5 test headers. Figure 3-2 provides a schematic showing the various connections to the PHI connector.

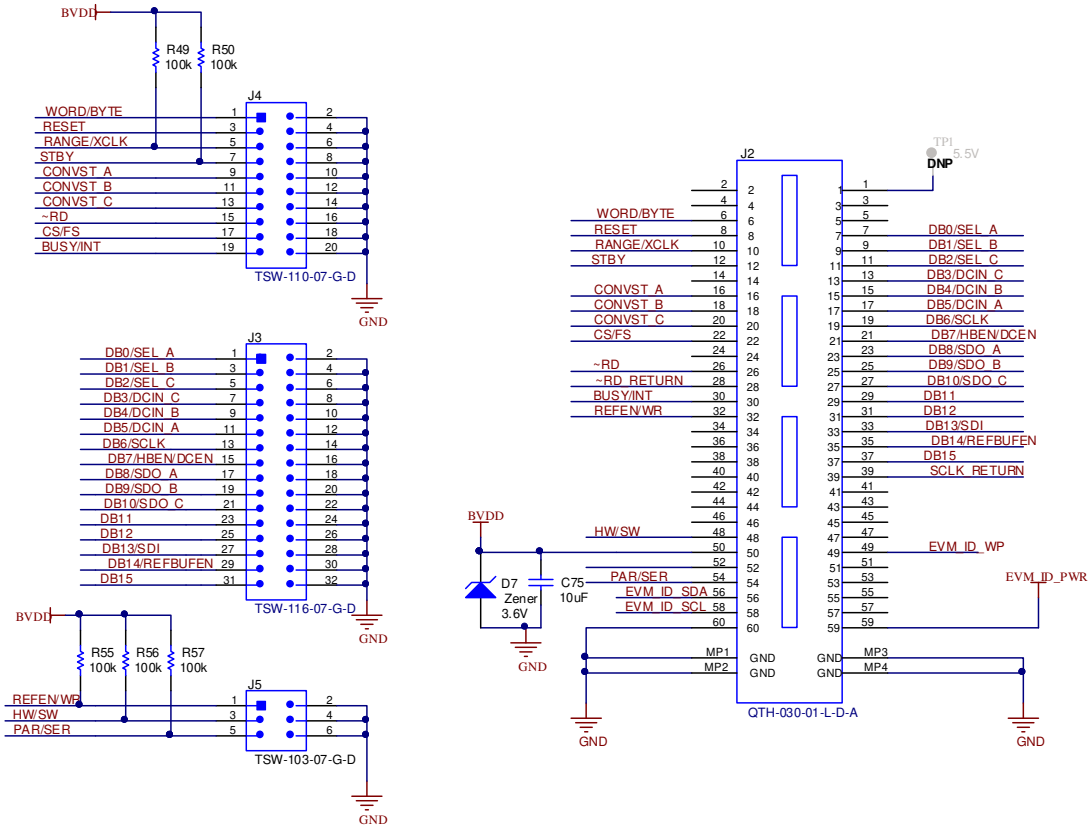

Figure 3-2. Connections to PHI Connector

4 Power Supplies

The ADS8555 device uses four power supplies: AVDD (5 V), BVDD (3.3 V), HVDD (12 V), and HVSS (–12 V). The two high-voltage power supplies require an external ±15-V supply and are connected on a screw terminal strip (J1). The ±15-V supplies are regulated from ±15 V to ±12 V for HVDD and HVSS. The digital voltage supply (BVDD), is generated with the USB power. The analog supply (AVDD) is generated using the external 15-V supply and an LDO to generate 5 V.

4.1 External Power Connections and Test Points

The screw terminal block J1 is used to connect the external high voltage supplies. These supplies are not provided in the evaluation module kit and the expectation is that a low-noise lab supply is used to provide this power (for example, Keysight™ E3632A). The high-voltage supplies have transient voltage suppressor diodes to help protect the ADC from transients. These supplies are typically connected to ±15 V. For details on operation, see the ADS8555 data sheet. Figure 4-1 also shows how each supply has a light-emitting diode (LED) monitor for quick verification that power is applied.

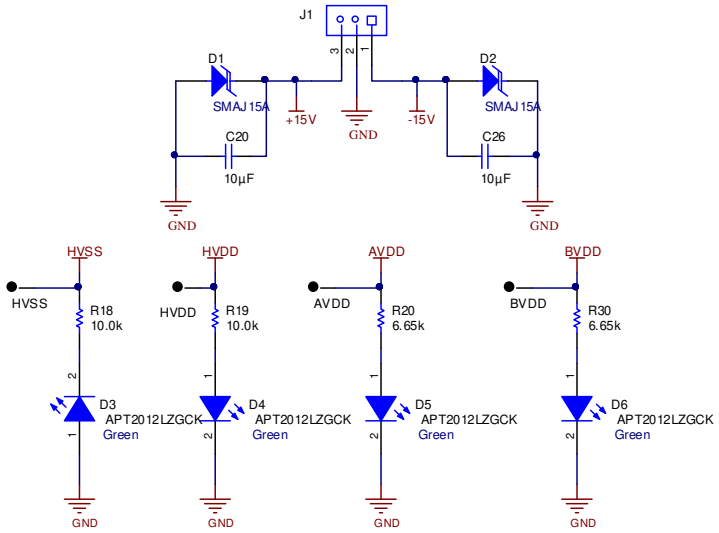

Figure 4-1. External Power Connections and Test Points

4.2 Low-Dropout Regulator (TPS7A3001 for HVSS)

As shown in Figure 4-2, the –15-V external power is connected to the TPS7A3001 LDO to generate –12 V. This LDO output can be programmed to different voltages by changing the feedback network R6 and R7. This LDO was selected for low noise and flexibility.

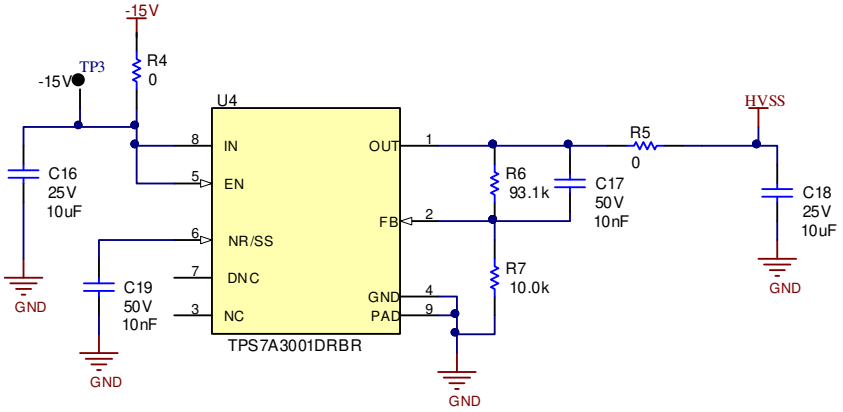

Figure 4-2. Low-Dropout Regulator (TPS7A3001 for HVSS)

4.3 Low-Dropout Regulator (TPS7A4700 for AVDD, HVDD)

The 15-V external power is connected to two LDOs (TPS7A4700RGWR). One LDO generates AVDD (5 V), and one generates HVDD (12 V). As shown in Figure 4-3, the TPS7A4700RGWR LDO output can be programmed to different voltages by installing or uninstalling the resistors connected on pins 4-12. This LDO was selected for low noise and flexibility.

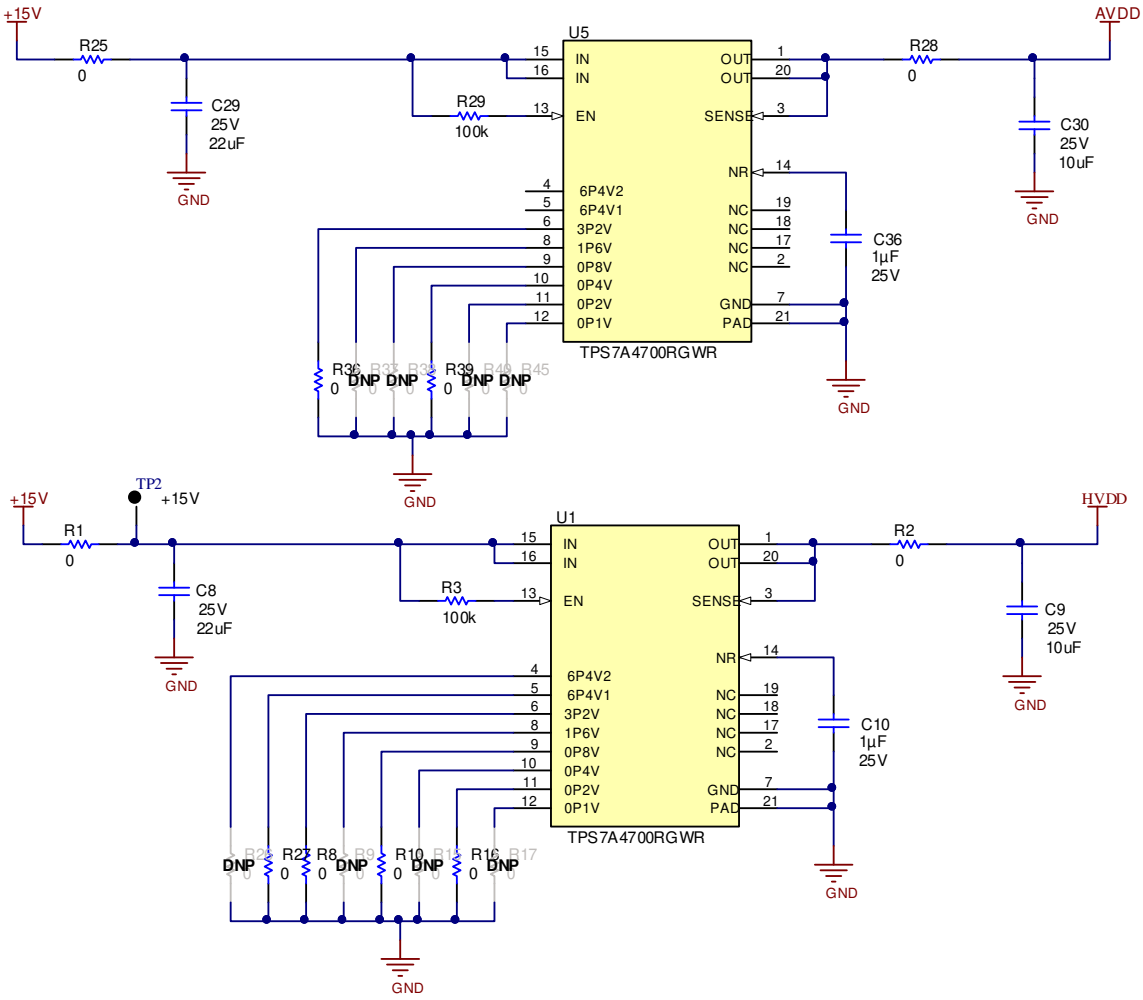

Figure 4-3. Low-Dropout Regulator (TPS7A4700 for AVDD, HVDD)

5 Installing the ADS8555EVM Software

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS8555EVM and run the GUI installer to install the EVM GUI software on your computer. Accept the license agreements and follow the on-screen instructions shown in Figure 5-1 to complete the installation.

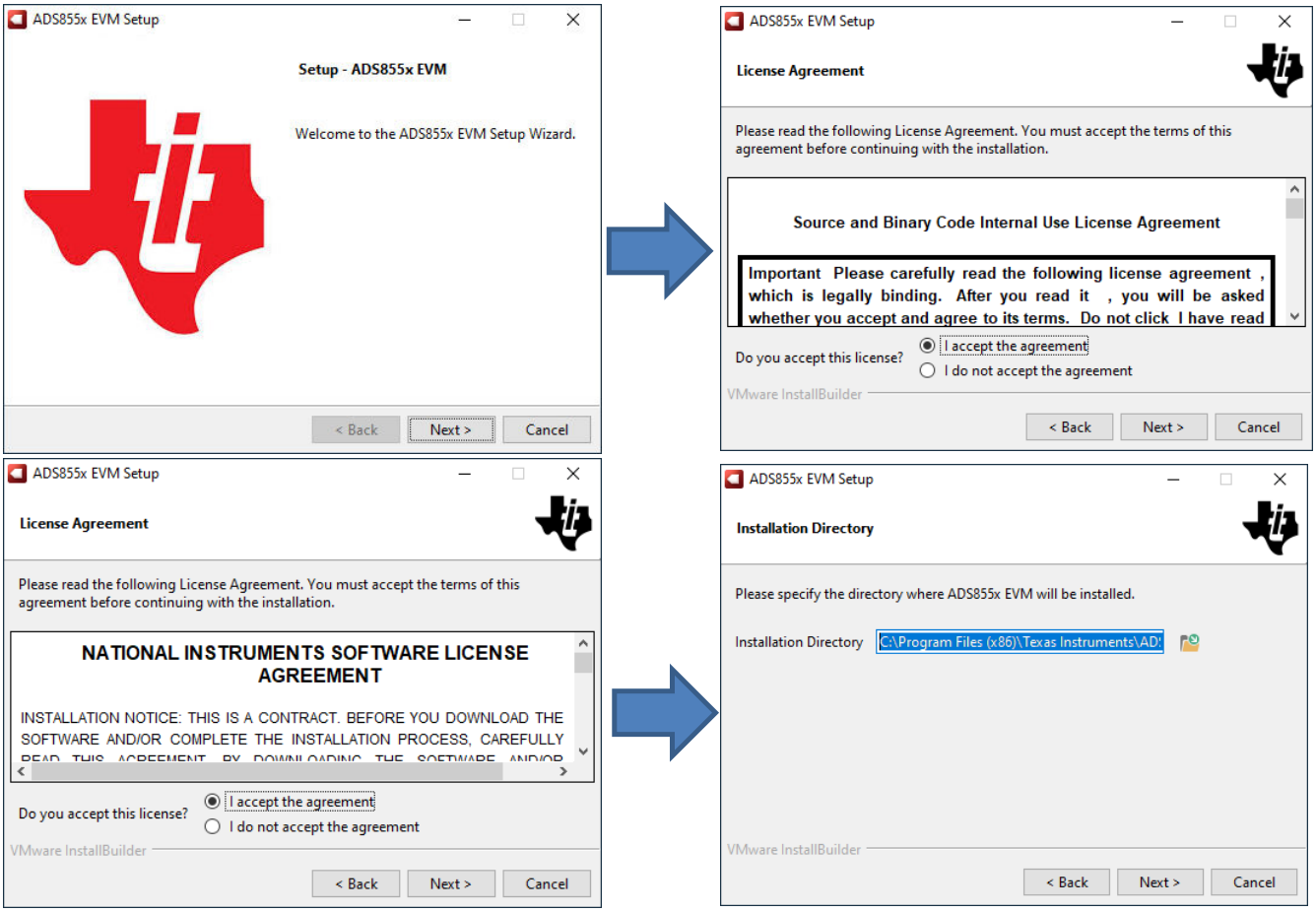

Figure 5-1. ADS8555 Software Installation Prompts

As a part of the ADS8555EVM GUI installation, a prompt with a *Device Driver Installation* (as shown in Figure 5-2) appears on the screen. Click *Next* to proceed.

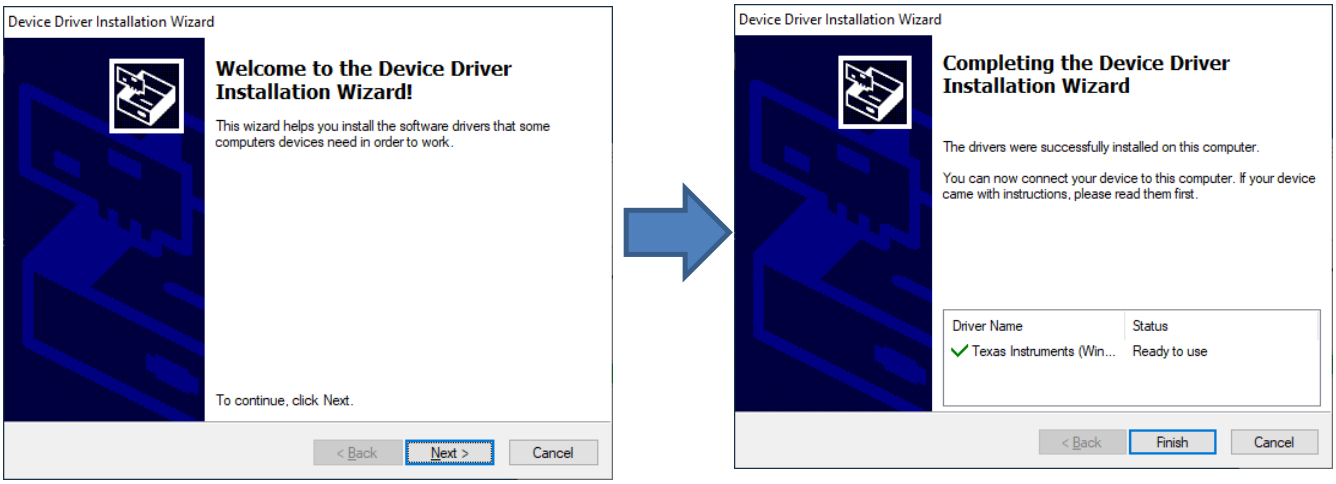

Figure 5-2. Device Driver Installation Wizard Prompts

The ADS8555EVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 5-3, if not already installed.

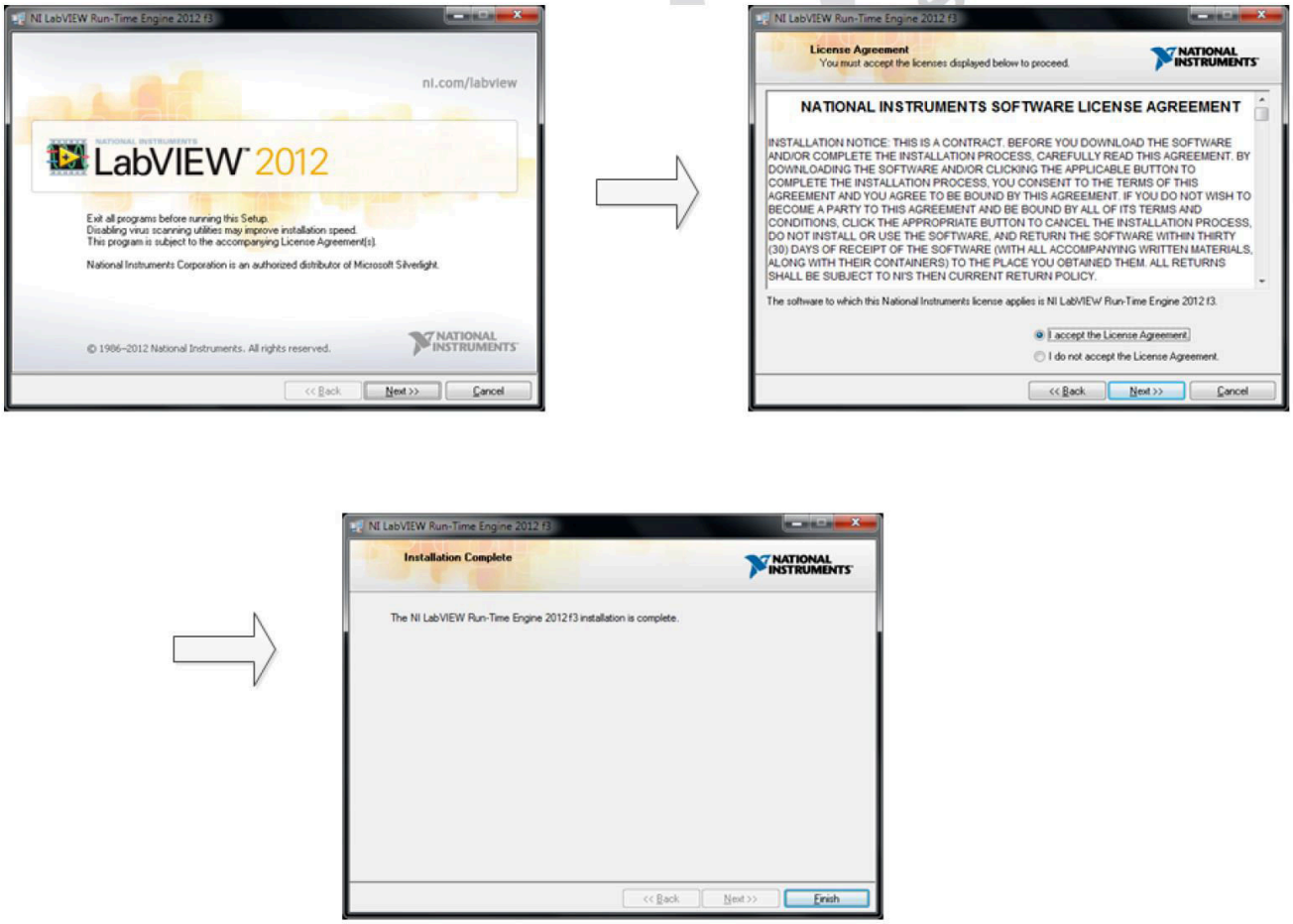

Figure 5-3. LabVIEW™ Run-Time Engine Installation

Verify that *C:\Program Files (x86)\Texas Instruments\ADS8555EVM* is as shown in Figure 5-4 after these installations.

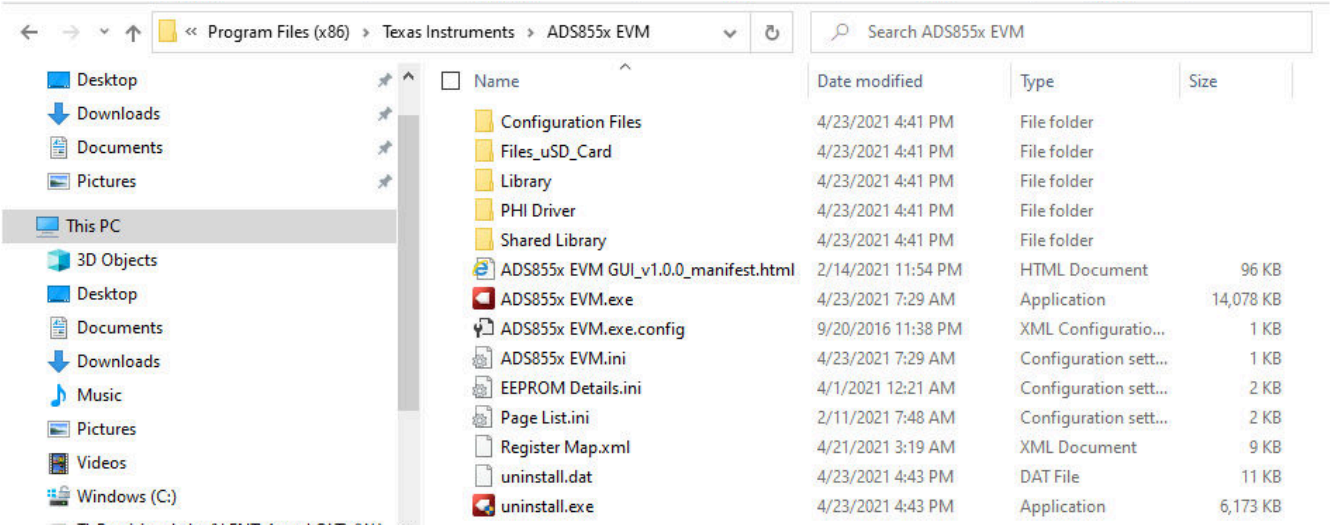

Figure 5-4. ADS8555EVM GUI Folder Post-Installation

6 ADS8555EVM Operation

This section provides step-by-step instructions for connecting the ADS8555EVM to the computer and evaluating the performance of the ADS8555.

6.1 Connecting the Hardware and Running the GUI

1. Set the jumpers according to Section 6.2.
2. Physically connect P2 of the PHI to J10 of the ADS8555EVM. Install the screws to assure a robust connection.
3. Connect the USB on the PHI to the computer first.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 6-1 shows the resulting LED indicators.
4. As shown in Figure 6-2, start the software GUI. Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This process takes a few seconds, afterwards the AVDD and DVDD power supplies turn on.
5. Connect the external ±15-V power supplies and GND to J1. This connection generates the AVDD, HVDD, and HVSS supplies (HVDD = 12 V, HVSS = –12 V, and AVDD = 5 V).
6. Connect the signal generator. The default input range is ±10 V (or 10 Vpk). A common input signal applied is a sinusoidal 1-kHz, 9.9-Vpk signal with a 0-V offset. This signal is adjusted just below the full-scale range to avoid clipping.

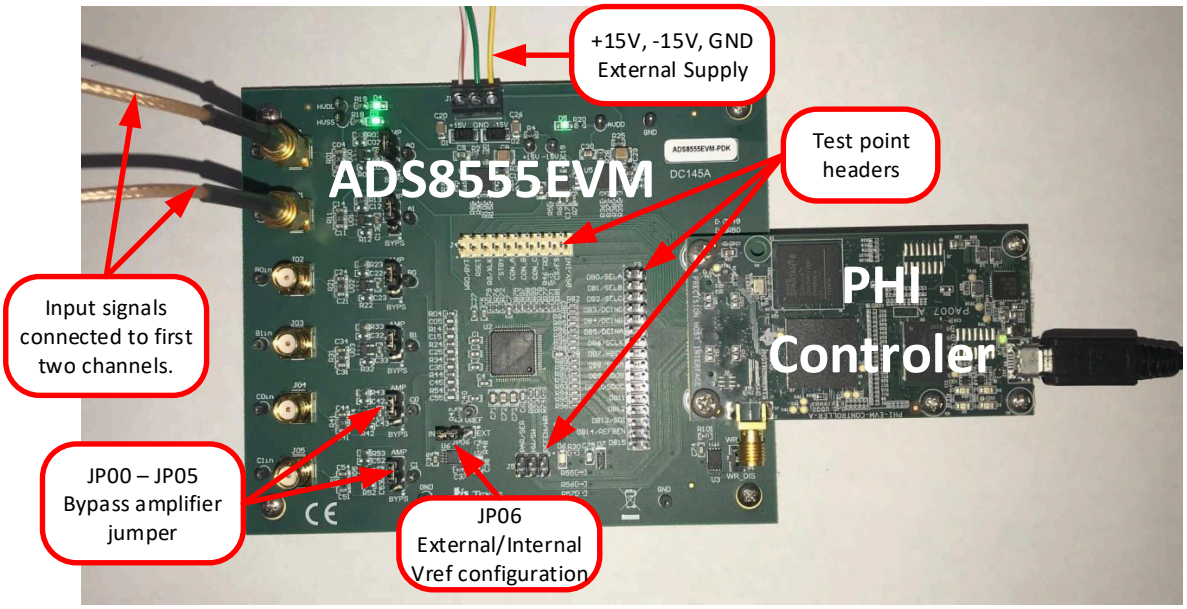

Figure 6-1. ADS8555EVM Hardware Setup and LED Indicators

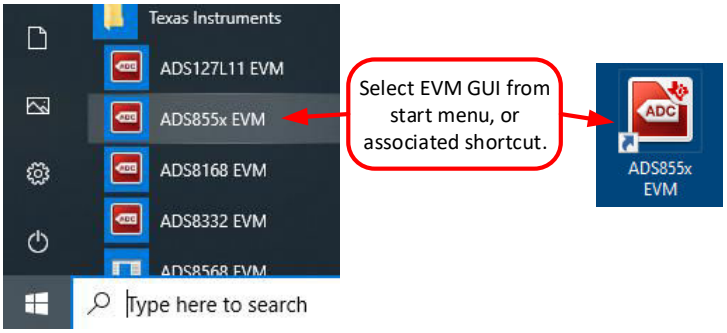

Figure 6-2. Launch the EVM GUI Software

6.2 Jumper Settings for the ADS8555EVM

The amplifiers and reference can be configured with jumpers. The amplifier jumpers (JP00–JP05) determine if the amplifier is used or if an external signal is directly connected to the ADC input. JP06 is used to select either the internal or external reference option. Make sure that the GUI configuration for the device reference matches the setting of JP06. The GUI software starts up in the *internal* reference mode, so make sure the JP06 is in the *INT* position. Table 6-1 lists the various jumper settings for the ADS8555EVM.

Table 6-1. Jumper Settings

JUMPER	SETTING	DEFAULT	FUNCTION
JP00–JP05	AMP/BYPS	AMP	These eight jumpers determine if the amplifier is used to buffer the inputs signals or if the amplifier is bypassed. Choosing AMP connects the amplifier between each SMA connector (JP00–JP05) and the ADC input. The default amplifier configuration is noninverting (gain = 1 V/V). The amplifier gain configuration can be adjusted by soldering and desoldering different resistors. Choosing the bypass configuration (BYPS) connects the SMA connectors directly to the ADC input.
JP06	INT/EXT	INT	This jumper selects either the internal or external mode on the voltage reference. Using the internal mode disconnects the external reference. Using the external mode connects the external REF5025 2.5-V reference to the ADC reference input. Make sure that the GUI settings for the voltage reference match the setting on this jumper.

6.3 Modifying Hardware and Using Software to Evaluate Other Devices in the Family

The ADS8555 is part of a family of related devices. This EVM hardware and software support the entire family because all the devices are pin-for-pin compatible. The Table 6-2 lists other compatible devices in the family. The following procedure shows how to modify the hardware and software to evaluate the other devices in this family.

1. Desolder the ADS8555 and replace this device with the device you want to evaluate.
2. Enable the EEPROM for writing. This process is done by changing switch S2 to the *WR_EN* (top) position using tweezers. Figure 6-3 details this process.
3. Connect the EVM and start the GUI as described in Figure 6-2.
4. Under the *Tools* menu in Figure 6-4, select *Load EEPROM* to load the EEPROM according to the device that is currently installed. When this procedure is successfully completed, the status bar at the top of the software updates according to the device installed on the hardware.

Table 6-2. Compatible Devices

DEVICE	RESOLUTION	PARALLEL DATA RATE	SERIAL DATA RATE	OTHER FEATURE
ADS8555	16	630	450	Does not have partial power-down mode
ADS8556	16	630	450	—
ADS8557	14	670	470	—
ADS8558	12	730	500	—

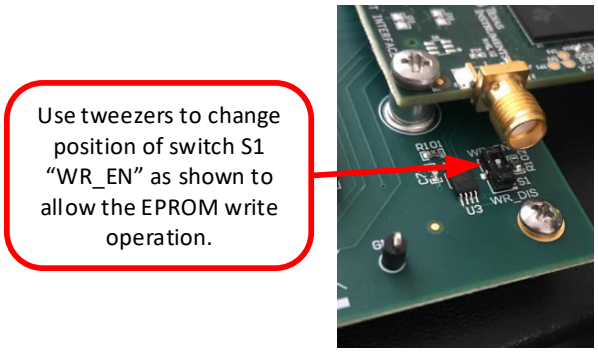

Figure 6-3. Enable EEPROM for Writing

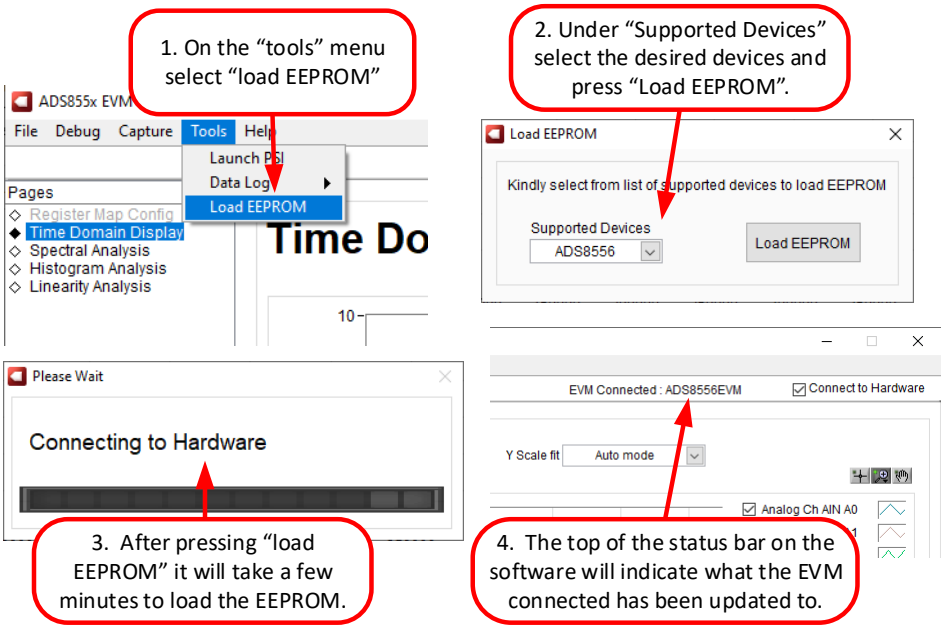

Figure 6-4. Configure EEPROM and Software for the New Device

6.4 EVM GUI Global Settings for ADC Control and Registers

Figure 6-5 shows the *Register Map* page. This page can only be accessed by selecting *Software* device mode. Editing the *CONFIG_REG* configures the different ranges and voltage references available on the ADS8555. See the ADS8555 data sheet for register field details. The left hand side of this GUI contains important configurations such as interface selection, device mode, range selection, and sampling rate. These controls are always available on the left hand side of the GUI regardless of which page is selected. Also, if *Hardware* mode is used, the hardware input select pins on the device are set according the controls on the left hand side. For example, when in hardware mode if the *Parallel Interface* is selected, than the PAR/SER pin on the device is driven low by the PHI to select parallel interface mode.

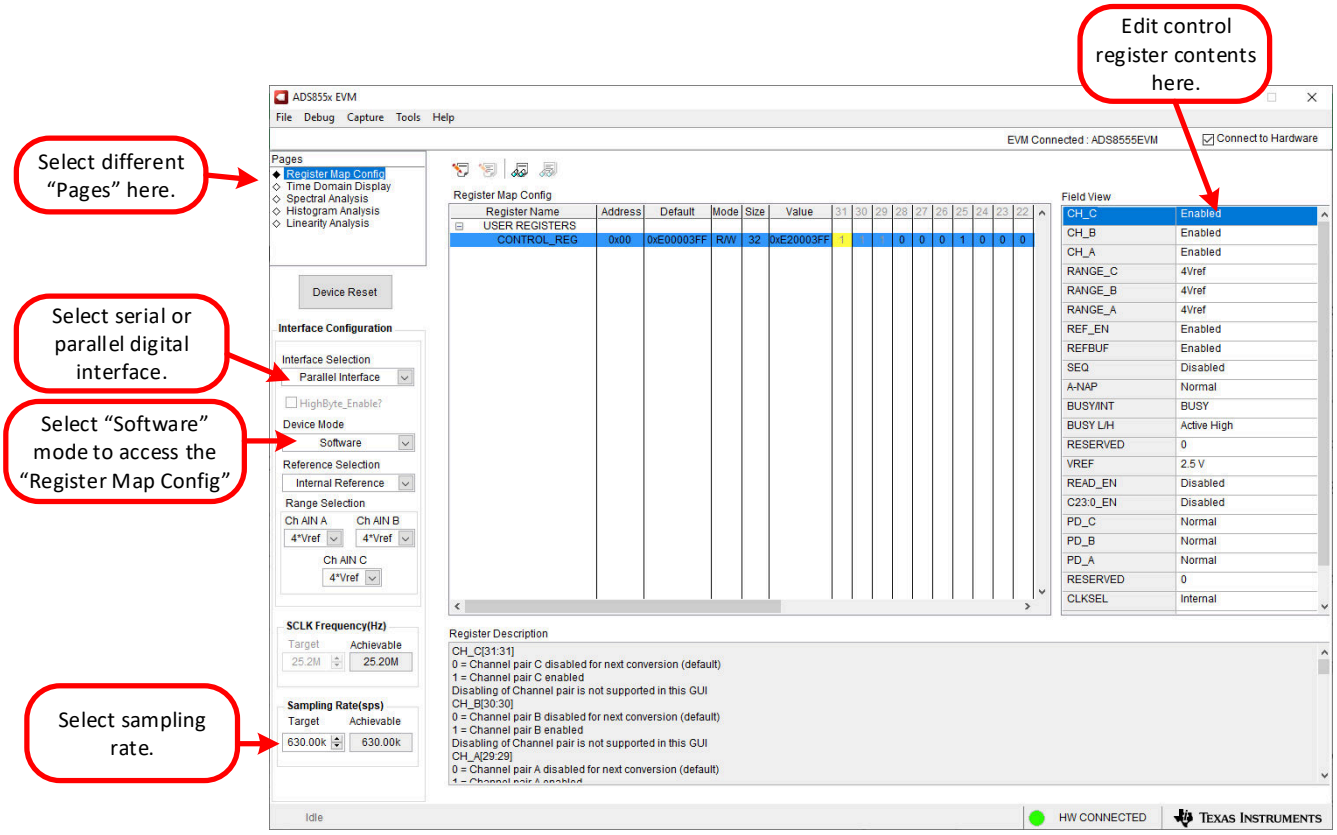

Figure 6-5. EVM GUI Global Settings for ADC Control and Registers

6.5 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS8555EVM, as per the current interface mode settings indicated in Figure 6-6 by using the *Capture* button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

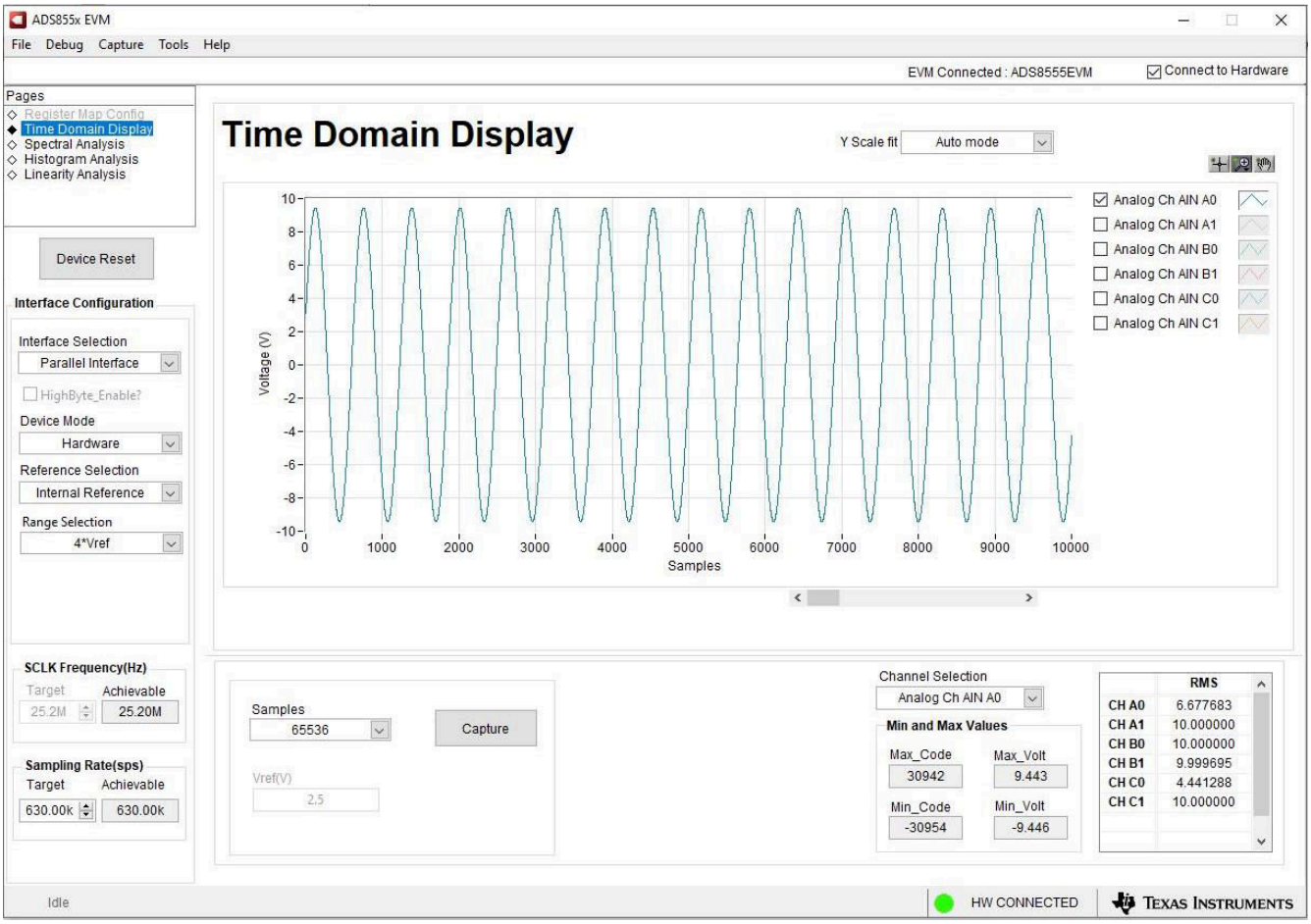

Figure 6-6. Time Domain Display

6.6 Frequency Domain Display

The spectral analysis tool, shown in Figure 6-7, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8555 ADC through single-tone sinusoidal signal fast Fourier transform (FFT) analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of noncoherent sampling (this discussion is beyond the scope of this document). The 7-term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

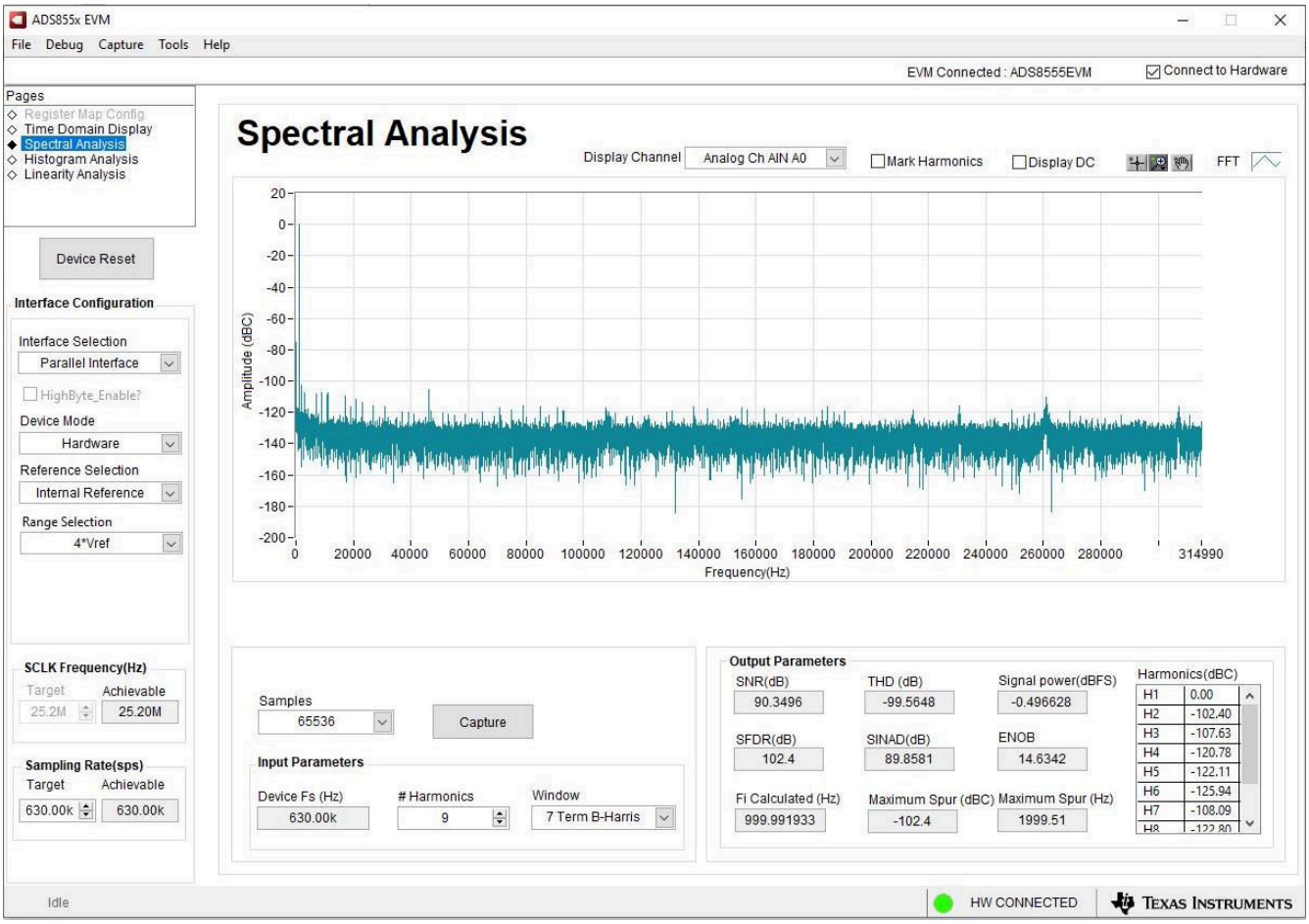

Figure 6-7. Frequency Domain Display

6.7 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. As shown in Figure 6-8, the histogram corresponding to a DC input is displayed on clicking the *Capture* button.

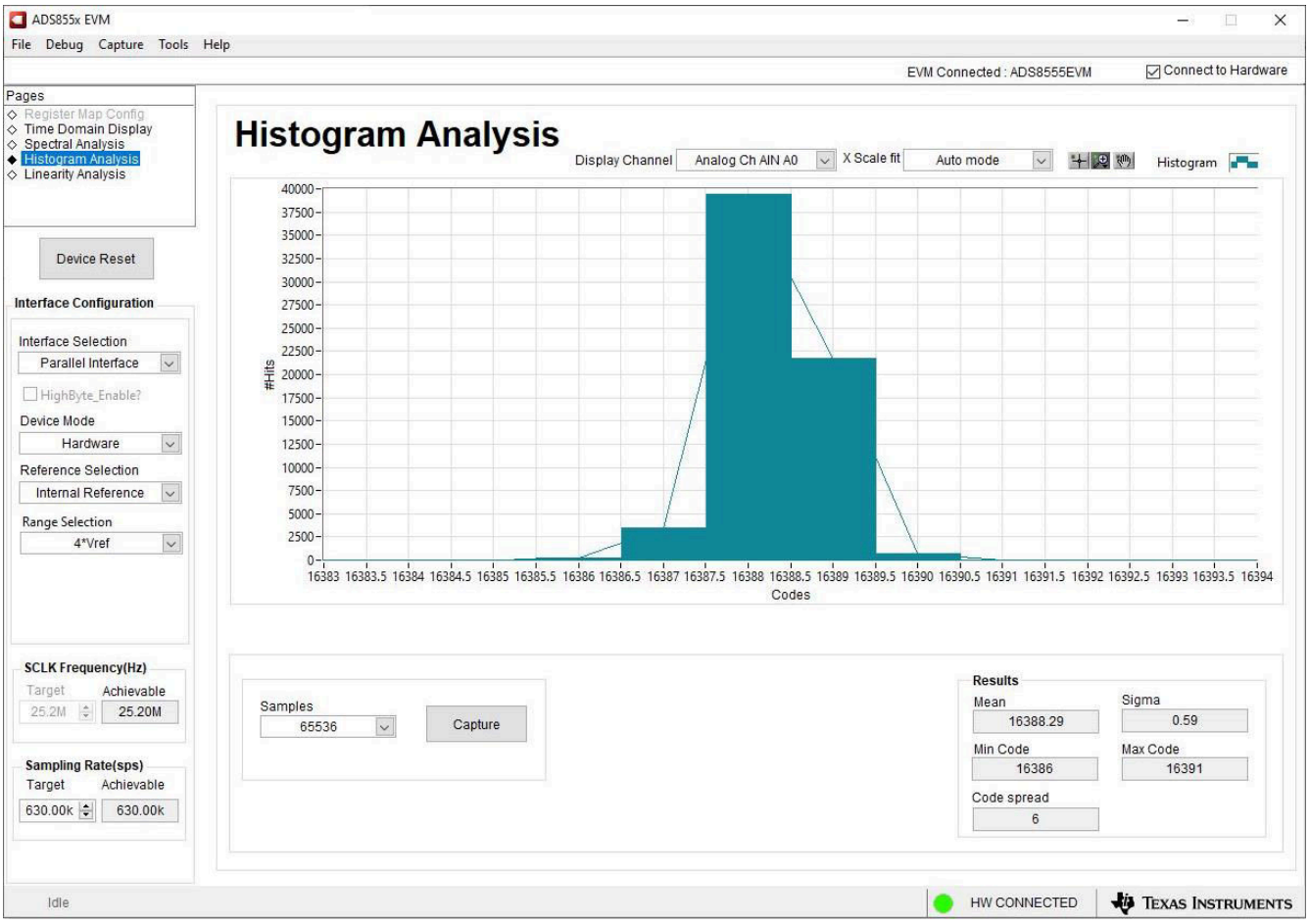

Figure 6-8. Histogram Display

7 Bill of Materials, Layout, and Schematics

This section provides a bill of materials (BOM), a PCB layout for the ADS8555EVM, and schematics for the ADS8555EVM.

7.1 Bill of Materials

Table 7-1 lists the bill of materials (BOM) for the ADS8555EVM.

Table 7-1. Bill of Materials (BOM)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB	1		Printed circuit board	ADS8555	Any
C1–C7, C10, C27, C28, C36, C37	12	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	C0603C105K3RACTU	Kemet
C01, C11, C21, C31, C41, C51	6	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0603	GRM1885C1H102JA01D	MuRata
C03, C04, C13, C14, C23, C24, C33, C34, C43, C44, C53, C54	12	0.1uF	CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	C0603C104K5RACAUTO	Kemet
C05, C15, C25, C35, C45, C55	6	220pF	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	06035A221JAT2A	AVX
C8, C29	2	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	GRM32ER71E226KE15L	MuRata
C9, C16, C18, C30, C38, C71, C72, C73, C75	9	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	CL21A106KAFN3NE	Samsung Electro-Mechanics
C17, C19	2	0.01uF	CAP, CERM, 0.01 µF, 50 V,+/- 10%, X7R, 0603	885012206089	Wurth Elektronik
C20, C26	2	10uF	CAP, CERM, 10 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206	CGA5L1X7R1H106K160AC	TDK
C39, C74	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	C0603C104K5RACTU	Kemet
C40	1	0.47uF	CAP, CERM, 0.47 uF, 25 V, +/- 10%, X7R, 0603	GRM188R71E474KA12D	MuRata
D1, D2	2	15V	Diode, TVS, Uni, 15 V, 24.4 Vc, 400 W, 16.4 A, SMA	SMAJ15A	Littelfuse
D3–D6	4	Green	LED, Green, SMD	APT2012LZGCK	Kingbright
D7	1	3.6V	Diode, Zener, 3.6 V, 500 mW, SOD-123	MMSZ4685T1G	ON Semiconductor
H1–H4	4		Hex Standoff Threaded #4-40 Aluminum 0.250" (6.35mm) 1/4"	1891	Keystone
H5–H8	4		MACHINE SCREW PAN PHILLIPS, 5/16", 4-40	PMSSS 440 0031 PH	B&F Fastener Supply
H13, H14	2		Machine Screw Pan PHILLIPS M3	RM3X4MM 2701	APM HEXSEAL
H15, H16	2		ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J00–J05	6		SMA Straight Jack, Gold, 50 Ohm, TH	901-144-8RFX	Amphenol RF
J1	1		Terminal Block, 3.5mm Pitch, 3x1, TH	ED555/3DS	On-Shore Technology
J2	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	QTH-030-01-L-D-A	Samtec
J3	1		Header, 100mil, 16x2, Gold, TH	TSW-116-07-G-D	Samtec
J4	1		Header, 100mil, 10x2, Gold, TH	TSW-110-07-G-D	Samtec
J5	1		Header, 100mil, 3x2, Gold, TH	TSW-103-07-G-D	Samtec

Table 7-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
JP00–JP06	7		Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
R1, R2, R03, R4, R5, R13, R23, R25, R28, R33, R43, R53, R102	13	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R01, R11, R21, R31, R41, R51	6	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	RT0603BRB071KL	Yageo America
R3, R29	2	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R04, R14, R24, R34, R44, R54	6	24.9	RES, 24.9, 1%, 0.1 W, 0603	RC0603FR-0724R9L	Yageo
R6	1	93.1k	RES, 93.1 k, 1%, 0.1 W, 0603	RC0603FR-0793K1L	Yageo
R7, R18, R19, R101	4	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R8, R10, R16, R27, R36, R39	6	0	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	Yageo America
R20, R30	2	6.65k	RES, 6.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04026K65FKED	Vishay-Dale
R35, R46, R71– R99	31	49.9	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040249R9FKED	Vishay-Dale
R47	1	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R48	1	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3RQFR22V	Panasonic
R49, R50, R55, R56, R57	5	100k	RES, 100 k, 1%, 0.0625 W, 0402	RC0402FR-07100KL	Yageo America
S1	1		Switch, Slide, SPDT 100mA, SMT	CAS-120TA	Copal Electronics
SH-JP00–SH-JP06	7	1x2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
TP2–TP23	22		Test Point, Miniature, Black, TH	5001	Keystone
U00–U05	6		2.2 nV/rtHz, 18 MHz, Precision, RRO, Operational Amplifier, 4.5 to 36 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br)	OPA209AIDBVR	Texas Instruments
U1, U5	2		36V, 1A, 4.17μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	TPS7A4700RGWR	Texas Instruments
U2	1		16 Bit Analog to Digital Converter 6 Input 1 SAR 64-LQFP (10x10)	ADS8555SPMR	Texas Instruments
U3	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	BR24G32FVT-3AGE2	Rohm
U4	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	TPS7A3001DRBR	Texas Instruments
U6	1		3 μVpp/V Noise, 3 ppm/°C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	REF5025AIDGKR	Texas Instruments
C02, C12, C22, C32, C42, C52	0	100pF	CAP, CERM, 100 pF, 50 V, +/-5%, C0G/NP0, 0603	885012006057	Wurth Elektronik

Table 7-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A
R02, R12, R22, R32, R42, R52	0	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	RT0603BRB071KL	Yageo America
R9, R15, R17, R26, R37, R38, R40, R45	0	0	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	Yageo America
TP1	0		Test Point, Miniature, Black, TH	5001	Keystone

7.2 Board Layout

Figure 7-1 shows the PCB layout for the ADS8555EVM.

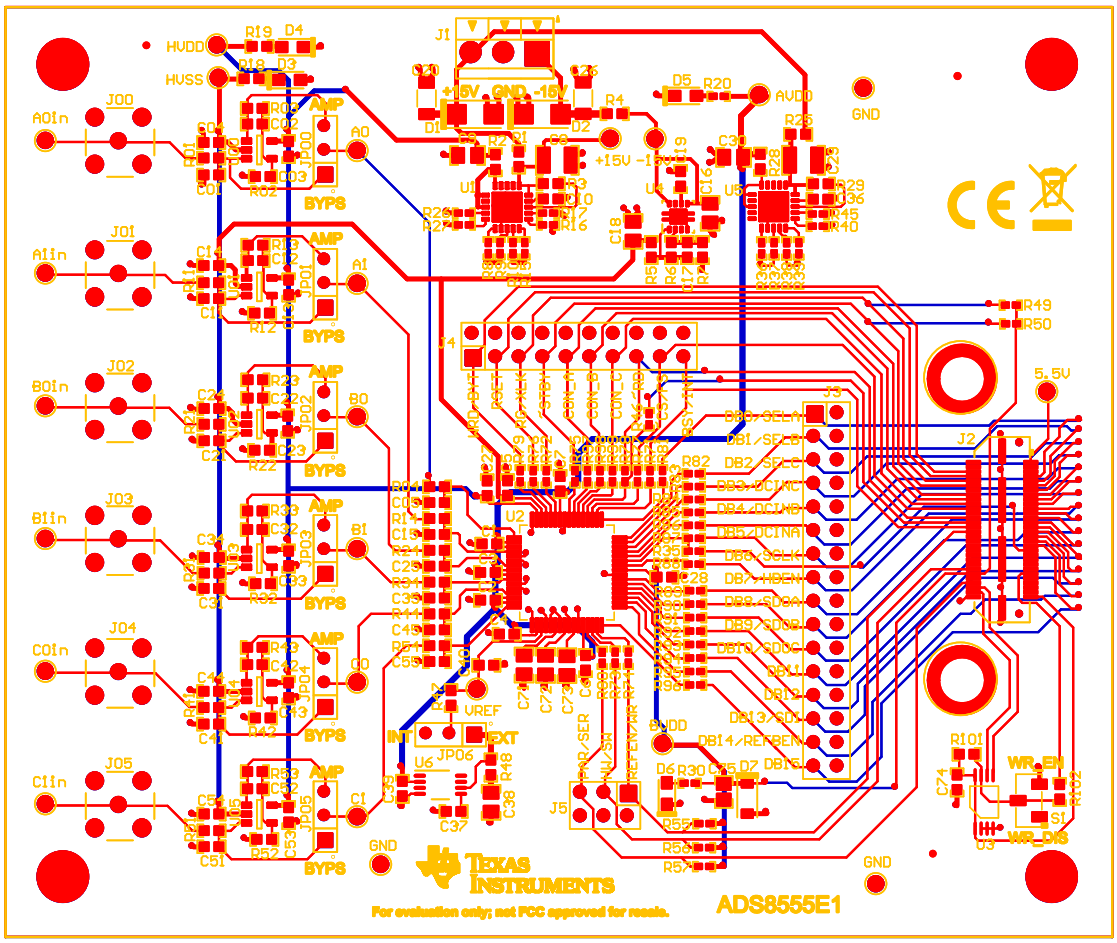

Figure 7-1. Board Layout

7.3 Schematics

Figure 7-2 shows a schematic for the amplifier drive section of the ADS8555EVM. The amplifier is by default a buffer and can be bypassed by using a jumper.

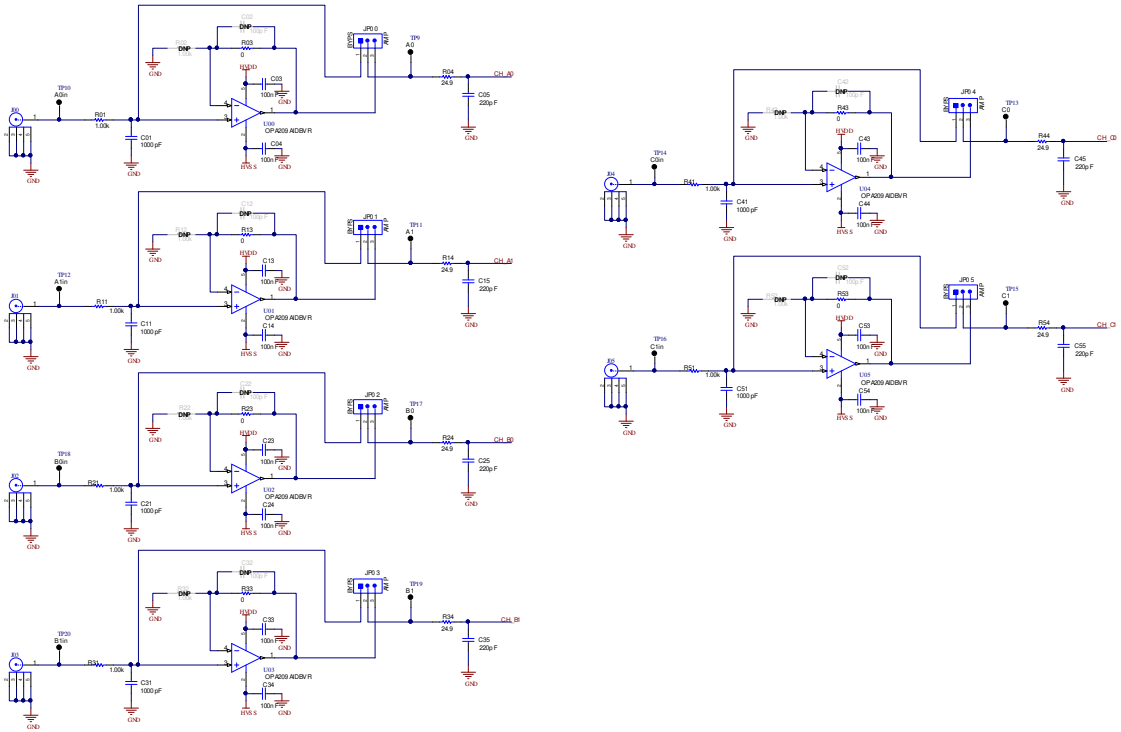

Figure 7-2. Amplifier Drive Schematic

Figure 7-3 shows the LDOs used to generate the AVDD, HVDD, and HVSS supplies.

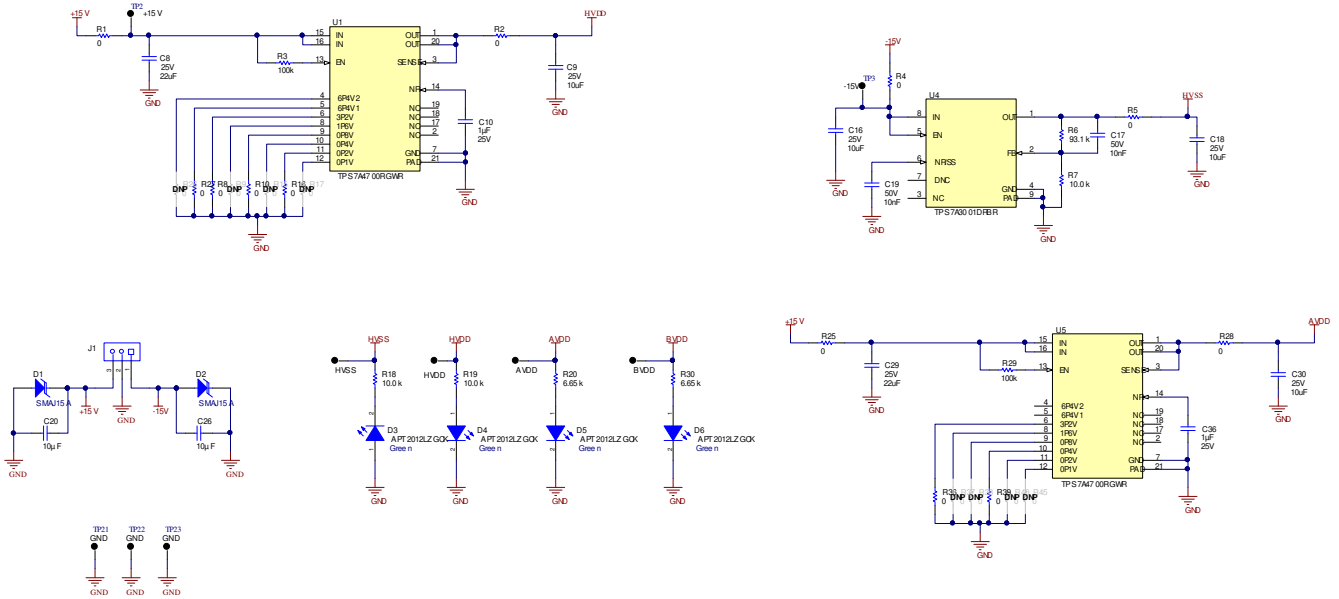

Figure 7-3. LDO Schematic

Figure 7-4 shows the ADC decoupling, digital connections, and reference connections.

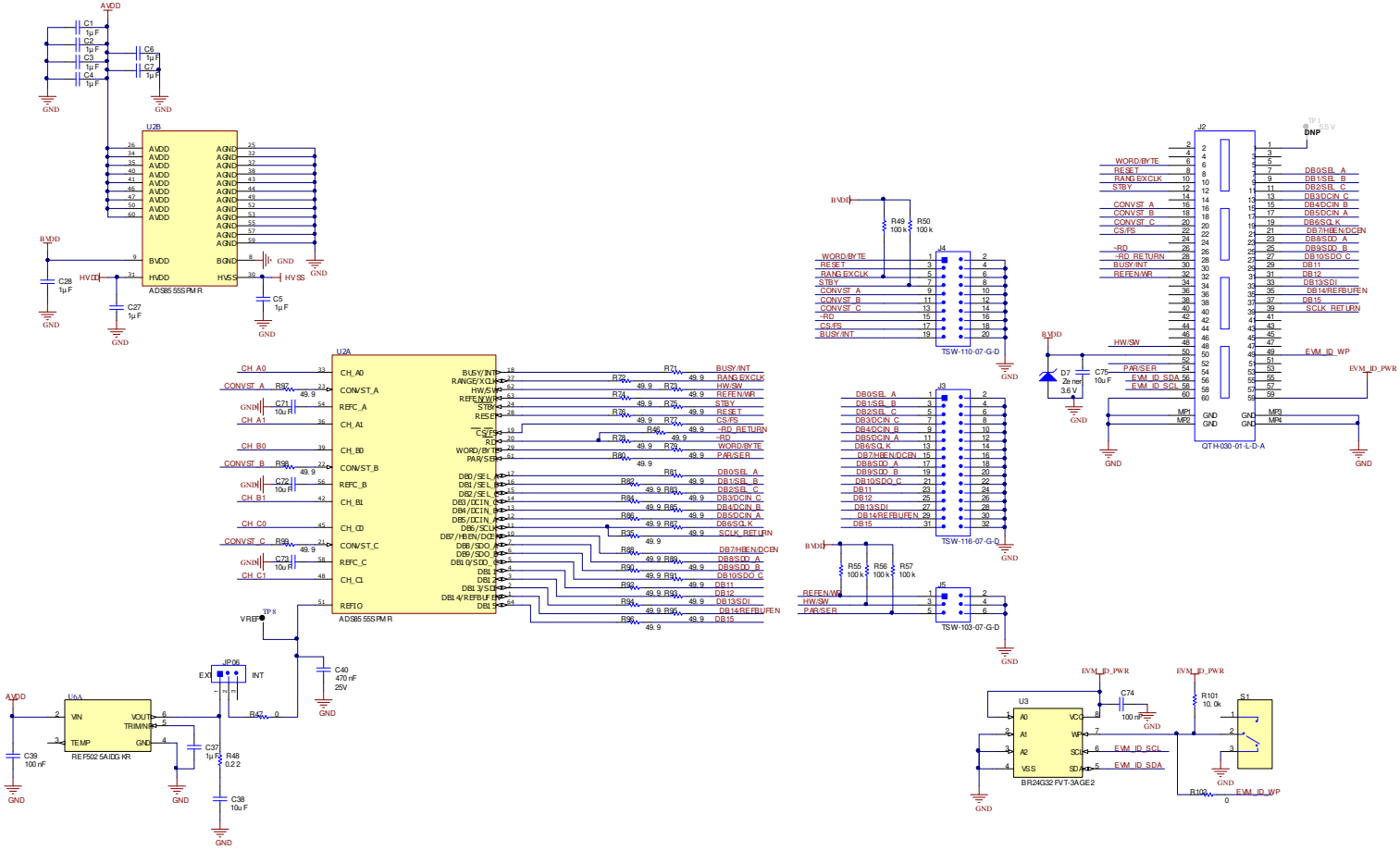

Figure 7-4. ADC, Reference, and Digital I/O Schematic

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2009) to Revision A (May 2021)	Page
• Changed entire document because of substantial changes in EVM hardware and software	1

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