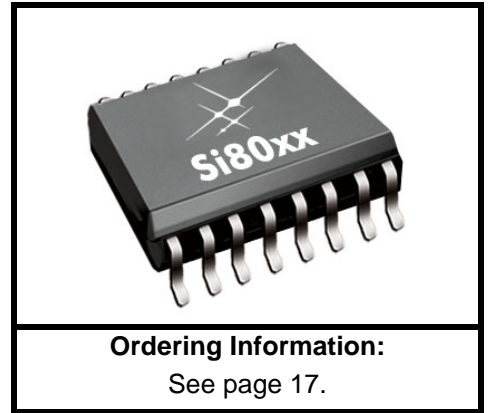


## 1 kV THREE TO SIX-CHANNEL DIGITAL ISOLATORS

### Features

- High-speed operation
  - DC to 10 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage
  - 3.15 – 5.5 V
- Up to 1000 V<sub>RMS</sub> isolation
- High electromagnetic immunity
- Low power consumption (typical)
  - 2.3 mA per channel at 10 Mbps
- Tri-state outputs with ENABLE
- Schmitt trigger inputs
- Default low output
- Precise timing (typical)
  - 40 ns propagation delay
  - 20 ns pulse width distortion
  - 100 ns minimum pulse width
- Transient Immunity 50 kV/μs
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C
- RoHS-compliant packages
  - QSOP-16



### Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated ADC, DAC
- Power inverters
- Communication systems

### Description

Skyworks' family of low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors. Data rates up to 10 Mbps are supported, and all devices achieve propagation delays of less than 65 ns. Enable inputs provide a single point control for enabling and disabling output drive. Ordering options include a choice of 1kV<sub>RMS</sub> isolation ratings.

TABLE OF CONTENTS

| <u>Section</u>                                    | <u>Page</u> |
|---------------------------------------------------|-------------|
| <b>1. Electrical Specifications</b> .....         | <b>3</b>    |
| <b>2. Functional Description</b> .....            | <b>7</b>    |
| 2.1. Theory of Operation .....                    | 7           |
| <b>3. Device Operation</b> .....                  | <b>8</b>    |
| 3.1. Device Startup .....                         | 10          |
| 3.2. Undervoltage Lockout .....                   | 10          |
| 3.3. Layout Recommendations .....                 | 11          |
| 3.4. Fail-Safe Operating Mode .....               | 11          |
| <b>4. Pin Descriptions (Si8030/35)</b> .....      | <b>12</b>   |
| <b>5. Pin Descriptions (Si8040/45)</b> .....      | <b>13</b>   |
| <b>6. Pin Descriptions (Si8050)</b> .....         | <b>14</b>   |
| <b>7. Pin Descriptions (Si8055)</b> .....         | <b>15</b>   |
| <b>8. Pin Descriptions (Si8065)</b> .....         | <b>16</b>   |
| <b>9. Ordering Guide</b> .....                    | <b>17</b>   |
| <b>10. Package Outline: 16-Pin QSOP</b> .....     | <b>18</b>   |
| <b>11. Land Pattern: 16-Pin QSOP</b> .....        | <b>20</b>   |
| <b>12. Top Markings</b> .....                     | <b>21</b>   |
| 12.1. Top Marking (16-Pin QSOP) .....             | 21          |
| 12.2. Top Marking Explanation (16-Pin QSOP) ..... | 21          |
| <b>Revision History</b> .....                     | <b>22</b>   |

## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

| Parameter                      | Symbol    | Min  | Typ | Max | Unit |
|--------------------------------|-----------|------|-----|-----|------|
| Ambient Operating Temperature* | $T_A$     | -40  | 25  | 125 | °C   |
| Supply Voltage                 | $V_{DD1}$ | 3.15 | —   | 5.5 | V    |
|                                | $V_{DD2}$ | 3.15 | —   | 5.5 | V    |

\*Note: The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

**Table 2. Electrical Characteristics**

( $V_{DD1} = 3.15$  to  $5.5$  V,  $V_{DD2} = 3.15$  to  $5.5$  V,  $T_A = -40$  to  $125$  °C)

| Parameter                             | Symbol    | Test Condition             | Min                      | Typ  | Max  | Unit |
|---------------------------------------|-----------|----------------------------|--------------------------|------|------|------|
| VDD Undervoltage Threshold            | VDDUV+    | $V_{DD1}, V_{DD2}$ rising  | 2.65                     | 2.80 | 3.05 | V    |
| VDD Undervoltage Threshold            | VDDUV-    | $V_{DD1}, V_{DD2}$ falling | 2.2                      | 2.50 | 2.75 | V    |
| VDD Undervoltage Threshold Hysteresis | VDDHYS    |                            | —                        | 270  | —    | mV   |
| Positive-Going Input Threshold        | VT+       | All inputs rising          | 1.4                      | 1.6  | 1.9  | V    |
| Negative-Going Input Threshold        | VT-       | All inputs falling         | 1.0                      | 1.2  | 1.4  | V    |
| Input Hysteresis                      | $V_{HYS}$ |                            | —                        | 0.40 | —    | V    |
| High Level Input Voltage              | $V_{IH}$  |                            | 2.0                      | —    | —    | V    |
| Low Level input voltage               | $V_{IL}$  |                            | —                        | —    | 0.8  | V    |
| High Level Output Voltage             | $V_{OH}$  | $I_{OH} = -4$ mA           | $V_{DD1}, V_{DD2} - 0.4$ | 4.8  | —    | V    |
| Low Level Output Voltage              | $V_{OL}$  | $I_{OL} = 4$ mA            | —                        | 0.2  | 0.4  | V    |
| Input Leakage Current                 | $I_L$     |                            | —                        | —    | ±10  | µA   |
| Output Impedance <sup>1</sup>         | $Z_O$     |                            | —                        | 50   | —    | Ω    |
| Enable Input High Current             | $I_{ENH}$ | $V_{ENx} = V_{IH}$         | —                        | 2.0  | —    | µA   |
| Enable Input Low Current              | $I_{ENL}$ | $V_{ENx} = V_{IL}$         | —                        | 16   | —    | µA   |
| Supply Current (DC)                   | $V_{DD1}$ | $V_I = 0, 1$               | —                        | 4.4  | 7.5  | mA   |
|                                       | $V_{DD2}$ | $C_L = 15$ pF              | —                        | 7.5  | 10   | mA   |

**Notes:**

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2.  $t_{PSK(P-P)}$  is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

# Si80xx-1kV

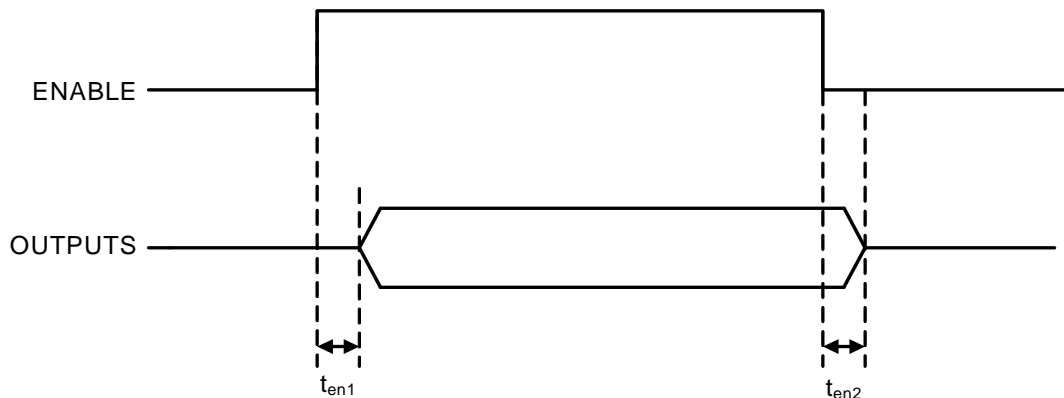
**Table 2. Electrical Characteristics (Continued)**

( $V_{DD1} = 3.15$  to  $5.5$  V,  $V_{DD2} = 3.15$  to  $5.5$  V,  $T_A = -40$  to  $125$  °C)

| Parameter                                       | Symbol             | Test Condition                                              | Min | Typ | Max | Unit        |
|-------------------------------------------------|--------------------|-------------------------------------------------------------|-----|-----|-----|-------------|
| Supply Current (10 Mbps)                        |                    |                                                             |     |     |     |             |
| $V_{DD1}$                                       |                    | $V_I = 5$ MHz                                               | —   | 4.4 | 7.5 | mA          |
| $V_{DD2}$                                       |                    | $C_L = 15$ pF                                               | —   | 9.4 | 12  | mA          |
| Maximum Data Rate                               |                    |                                                             | 0   | —   | 10  | Mbps        |
| Minimum Pulse Width                             |                    |                                                             | —   | —   | 100 | ns          |
| Propagation Delay                               | $t_{PHL}, t_{PLH}$ | See Figure 2                                                | 20  | 40  | 65  | ns          |
| Pulse Width Distortion<br>$ t_{PLH} - t_{PHL} $ | PWD                | See Figure 2                                                | —   | 20  | 30  | ns          |
| Propagation Delay Skew <sup>2</sup>             | $t_{PSK(P-P)}$     |                                                             | —   | 20  | 30  | ns          |
| Channel-Channel Skew                            | $t_{PSK}$          |                                                             | —   | 20  | 30  | ns          |
| Output Rise Time                                | $t_r$              | $C_L = 15$ pF<br>See Figure 2                               | —   | 2.5 | 4.0 | ns          |
| Output Fall Time                                | $t_f$              | $C_L = 15$ pF<br>See Figure 2                               | —   | 2.5 | 4.0 | ns          |
| Common Mode<br>Transient Immunity               | CMTI               | $V_I = V_{DD}$ or $0$ V<br>$V_{CM} = 1500$ V (see Figure 3) | 35  | 50  | —   | kV/ $\mu$ s |
| Enable to Data Valid                            | $t_{en1}$          | See Figure 1                                                | —   | 10  | —   | ns          |
| Enable to Data Tri-State                        | $t_{en2}$          | See Figure 1                                                | —   | 10  | —   | ns          |
| Start-up Time <sup>3</sup>                      | $t_{SU}$           |                                                             | —   | 40  | —   | $\mu$ s     |

**Notes:**

1. The nominal output impedance of an isolator driver channel is approximately  $50 \Omega$ ,  $\pm 40\%$ , which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2.  $t_{PSK(P-P)}$  is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.



**Figure 1. ENABLE Timing Diagram**

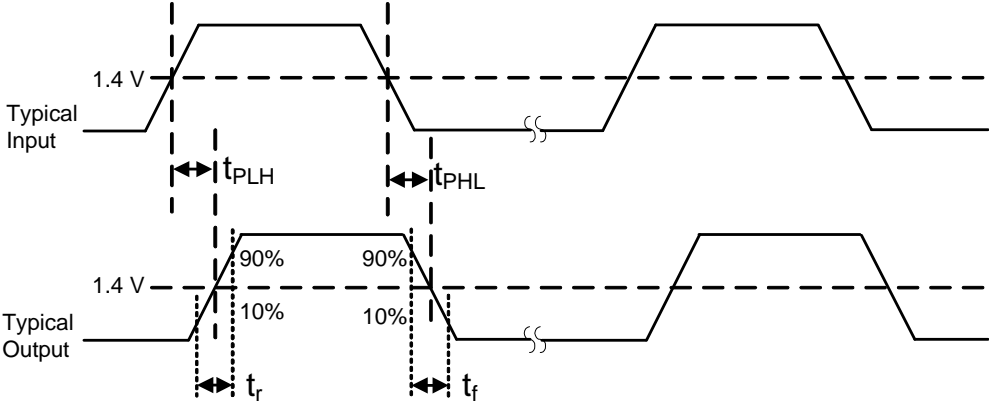


Figure 2. Propagation Delay Timing

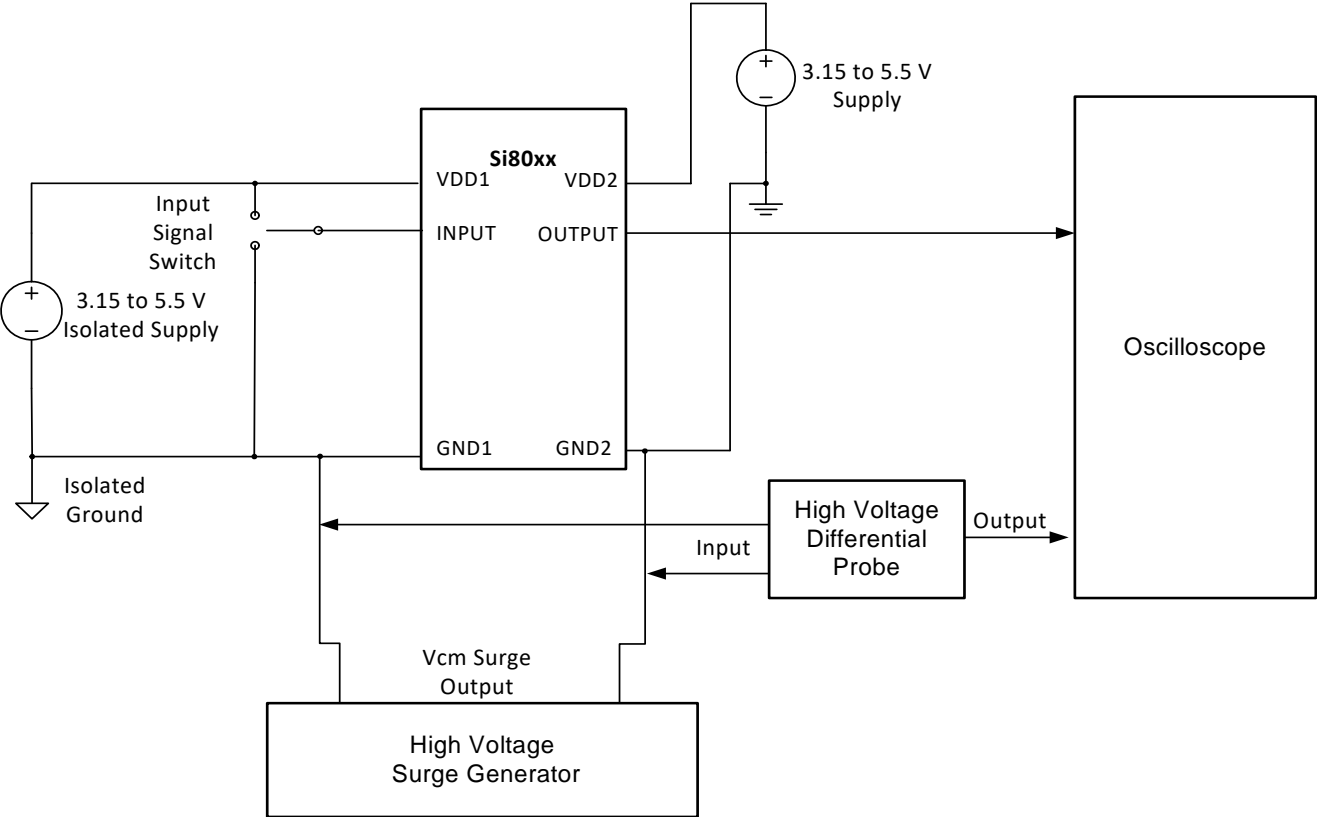


Figure 3. Common Mode Transient Immunity Test Circuit

# Si80xx-1kV

**Table 3. Thermal Characteristics**

| Parameter                             | Symbol        | QSOP-16 | Unit |
|---------------------------------------|---------------|---------|------|
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 105     | °C/W |
| Max Junction Temperature              | $T_J$         | 130     | °C   |

**Table 4. Absolute Maximum Ratings<sup>1</sup>**

| Parameter                                              | Symbol             | Min  | Typ | Max            | Unit      |
|--------------------------------------------------------|--------------------|------|-----|----------------|-----------|
| Storage Temperature <sup>2</sup>                       | $T_{STG}$          | -65  | —   | 150            | °C        |
| Ambient Temperature Under Bias                         | $T_A$              | -40  | —   | 125            | °C        |
| Junction Temperature                                   | $T_J$              | —    | —   | 150            | °C        |
| Supply Voltage                                         | $V_{DD1}, V_{DD2}$ | -0.5 | —   | 7.0            | V         |
| Input Voltage                                          | $V_I$              | -0.5 | —   | $V_{DD} + 0.5$ | V         |
| Output Voltage                                         | $V_O$              | -0.5 | —   | $V_{DD} + 0.5$ | V         |
| Output Current Drive Channel                           | $I_O$              | —    | —   | 22             | mA        |
| Latchup Immunity <sup>3</sup>                          |                    | —    | —   | 100            | V/ns      |
| Lead Solder Temperature (10 s)                         |                    | —    | —   | 260            | °C        |
| Maximum Isolation (Input to Output) (1 sec)<br>QSOP-16 |                    | —    | —   | 1500           | $V_{RMS}$ |

**Notes:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from -40 to 150 °C.
3. Latchup immunity specification is for slew rate applied across GND1 and GND2.

## 2. Functional Description

### 2.1. Theory of Operation

The Si80xx comprises a transmitter and a receiver separated by a semiconductor-based isolation barrier. The Si80xx uses a high-frequency internal oscillator on the transmitter to modulate digital input signals across the capacitive isolation barrier. On the receiver side, these signals are demodulated back to the corresponding digital output signals that are galvanically isolated from the input. This simple and elegant architecture provides a robust data path and requires no special considerations or initialization at start-up. A simplified block diagram for an Si80xx data channel is shown in Figure 4.

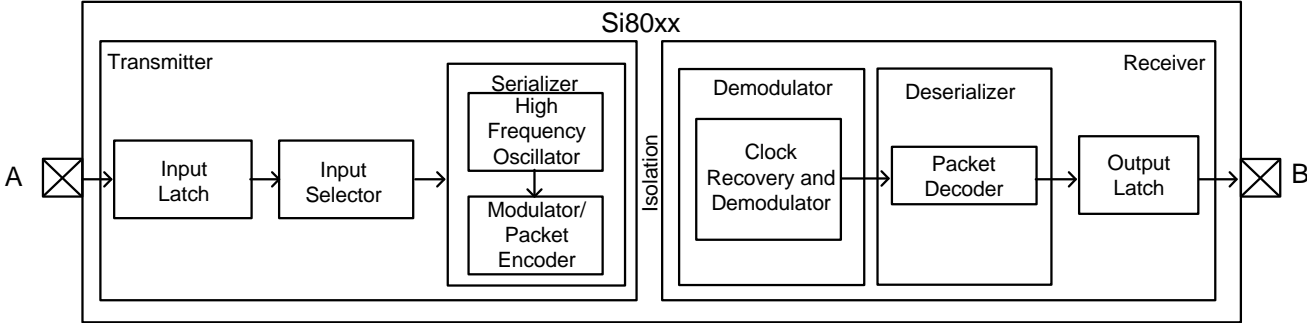


Figure 4. Simplified Channel Diagram

The transmitter consists of an input stage that latches in data from up to six asynchronous channels, followed by a serializer stage where the data is compressed into serial data packets that are then coupled across the capacitive isolation barrier. The receiver consists of a demodulator block that converts the modulated signal back into serial data packets that are then deserialized and latched to the output.

# Si80xx-1kV

## 3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 5, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 5 to determine outputs when power supply (VDD) is not present. Additionally, refer to Table 6 for logic conditions when enable pins are used.

**Table 5. Si80xx Logic Operation**

| V <sub>I</sub><br>Input <sup>1,2</sup> | EN<br>Input <sup>1,2,3,4</sup> | VDDI<br>State <sup>1,5,6</sup> | VDDO<br>State <sup>1,5,6</sup> | V <sub>O</sub> Output <sup>1,2</sup> | Comments                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H                                      | H or NC                        | P                              | P                              | H                                    | Enabled, normal operation.                                                                                                                                                                                                                                                                                                      |
| L                                      | H or NC                        | P                              | P                              | L                                    |                                                                                                                                                                                                                                                                                                                                 |
| X <sup>7</sup>                         | L                              | P                              | P                              | Hi-Z <sup>8</sup>                    | Disabled.                                                                                                                                                                                                                                                                                                                       |
| X <sup>7</sup>                         | H or NC                        | UP                             | P                              | L                                    | Upon transition of VDDI from unpowered to powered, V <sub>O</sub> returns to the same state as V <sub>I</sub> after Start-up Time, t <sub>SU</sub>                                                                                                                                                                              |
| X <sup>7</sup>                         | L                              | UP                             | P                              | Hi-Z <sup>8</sup>                    | Disabled.                                                                                                                                                                                                                                                                                                                       |
| X <sup>7</sup>                         | X <sup>7</sup>                 | P                              | UP                             | Undetermined                         | Upon transition of VDDO from unpowered to powered, V <sub>O</sub> returns to the same state as V <sub>I</sub> after Start-up Time, t <sub>SU</sub> , if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V <sub>O</sub> returns to Hi-Z after Start-up Time, t <sub>SU</sub> , if EN is L. |

**Notes:**

1. VDDI and VDDO are the input and output power supplies. V<sub>I</sub> and V<sub>O</sub> are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si80xx is operating in noisy environments.
4. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. "Powered" state (P) is defined as 3.15 V < VDD < 5.5 V.
6. "Unpowered" state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).



Table 6. Enable Input Truth<sup>1</sup>

| P/N                                  | EN <sup>2,3</sup> | Operation                                                                                          |
|--------------------------------------|-------------------|----------------------------------------------------------------------------------------------------|
| Si8030<br>Si8040<br>Si8050           | H                 | Outputs B1, B2, B3, B4, B5, B6 are enabled and follow input state.                                 |
|                                      | L                 | Outputs B1, B2, B3, B4, B5, B6 are disabled and Logic Low or in high impedance state. <sup>3</sup> |
| Si8035<br>Si8045<br>Si8055<br>Si8065 | —                 | Outputs B1, B2, B3, B4, B5, B6 are enabled and follow input state.                                 |

**Notes:**

1. Enable, EN, can be used for multiplexing, for clock sync, or other output control. EN is internally pulled-up to local VDD by a 16  $\mu$ A current source allowing it to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN if it is left floating. If EN is unused, it is recommended that it be connected to an external logic level, especially if the Si80xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

# Si80xx-1kV

## 3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

## 3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when  $V_{DD1}$  falls below  $V_{DD1(UVLO-)}$  and exits UVLO when  $V_{DD1}$  rises above  $V_{DD1(UVLO+)}$ . Side B operates the same as Side A with respect to its  $V_{DD2}$  supply. See Figure 5 for more details.

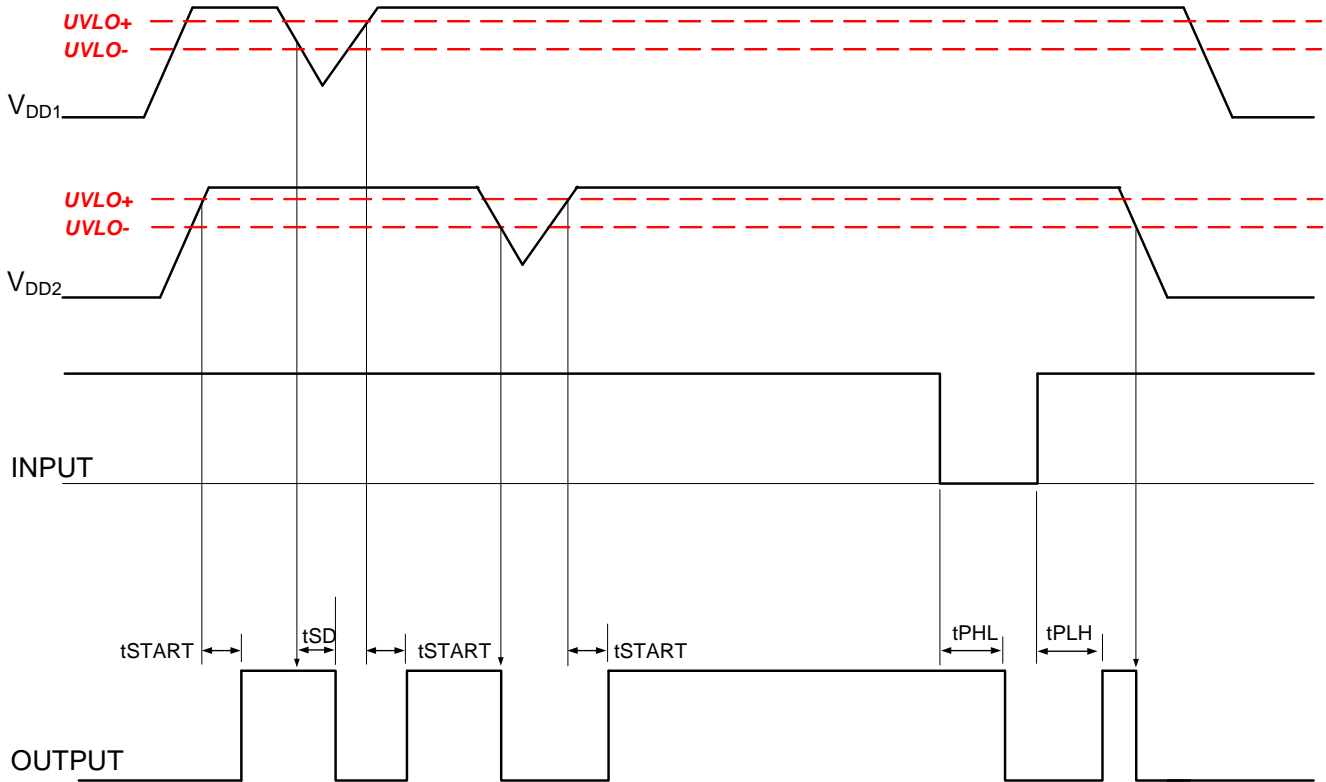


Figure 5. Device Behavior during Normal Operation

### 3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with  $>30 V_{AC}$ ) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with  $<30 V_{AC}$ ) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

#### 3.3.1. Supply Bypass

The Si80xx family requires a  $0.1 \mu\text{F}$  bypass capacitor between  $V_{DD1}$  and GND1 and  $V_{DD2}$  and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors ( $50\text{--}300 \Omega$ ) in series with the inputs and outputs if the system is excessively noisy.

#### 3.3.2. Output Pin Termination

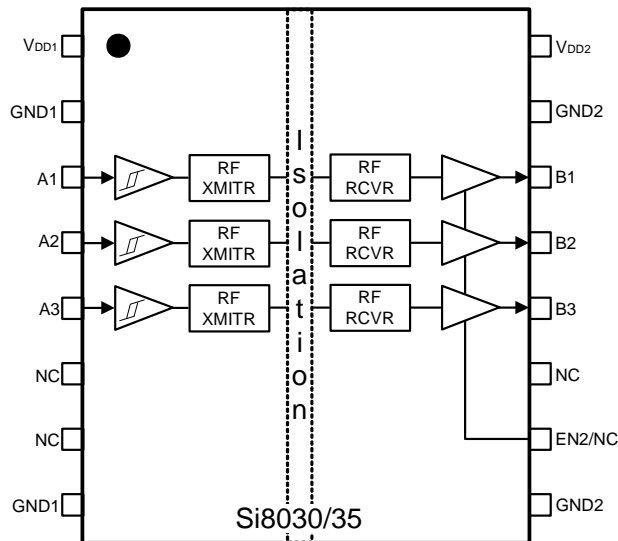
The nominal output impedance of an isolator driver channel is approximately  $50 \Omega$ ,  $\pm 40\%$ , which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

### 3.4. Fail-Safe Operating Mode

The default output state of Si80xx devices is logic low when the output supply is powered.

# Si80xx-1kV

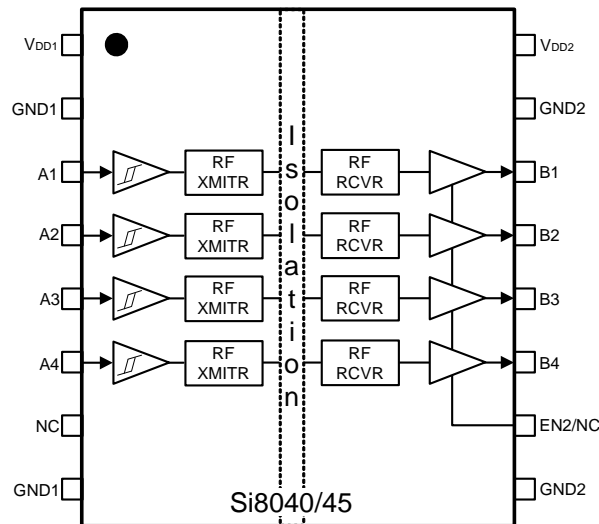
## 4. Pin Descriptions (Si8030/35)



| Name             | Pin# | Type           | Description                                        |
|------------------|------|----------------|----------------------------------------------------|
| V <sub>DD1</sub> | 1    | Supply         | Side 1 power supply.                               |
| GND1             | 2    | Ground         | Side 1 ground.                                     |
| A1               | 3    | Digital Input  | Side 1 digital input.                              |
| A2               | 4    | Digital Input  | Side 1 digital input.                              |
| A3               | 5    | Digital Input  | Side 1 digital input.                              |
| NC*              | 6    | NA             | No Connect.                                        |
| NC*              | 7    | NA             | No Connect.                                        |
| GND1             | 8    | Ground         | Side 1 ground.                                     |
| GND2             | 9    | Ground         | Side 2 ground.                                     |
| EN2/NC*          | 10   | Digital Input  | Side 2 active high enable on Si8030. NC on Si8035. |
| NC*              | 11   | NA             | No Connect.                                        |
| B3               | 12   | Digital Output | Side 2 digital output.                             |
| B2               | 13   | Digital Output | Side 2 digital output.                             |
| B1               | 14   | Digital Output | Side 2 digital output.                             |
| GND2             | 15   | Ground         | Side 2 ground.                                     |
| V <sub>DD2</sub> | 16   | Supply         | Side 2 power supply.                               |

**\*Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V<sub>DD</sub> or tied to GND.

## 5. Pin Descriptions (Si8040/45)

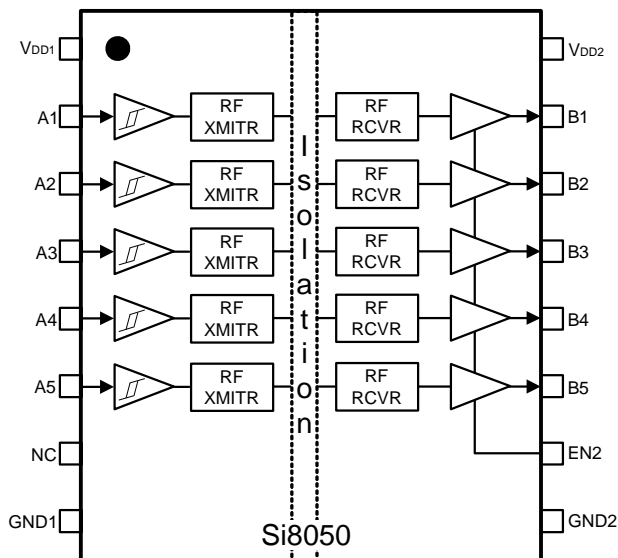


| Name             | Pin# | Type           | Description                                        |
|------------------|------|----------------|----------------------------------------------------|
| V <sub>DD1</sub> | 1    | Supply         | Side 1 power supply.                               |
| GND1             | 2    | Ground         | Side 1 ground.                                     |
| A1               | 3    | Digital Input  | Side 1 digital input.                              |
| A2               | 4    | Digital Input  | Side 1 digital input.                              |
| A3               | 5    | Digital Input  | Side 1 digital input.                              |
| A4               | 6    | Digital Input  | Side 1 digital input.                              |
| NC*              | 7    | NA             | No Connect.                                        |
| GND1             | 8    | Ground         | Side 1 ground.                                     |
| GND2             | 9    | Ground         | Side 2 ground.                                     |
| EN2/NC*          | 10   | Digital Input  | Side 2 active high enable on Si8040. NC on Si8045. |
| B4               | 11   | Digital Output | Side 2 digital output.                             |
| B3               | 12   | Digital Output | Side 2 digital output.                             |
| B2               | 13   | Digital Output | Side 2 digital output.                             |
| B1               | 14   | Digital Output | Side 2 digital output.                             |
| GND2             | 15   | Ground         | Side 2 ground.                                     |
| V <sub>DD2</sub> | 16   | Supply         | Side 2 power supply.                               |

**\*Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V<sub>DD</sub> or tied to GND.

# Si80xx-1kV

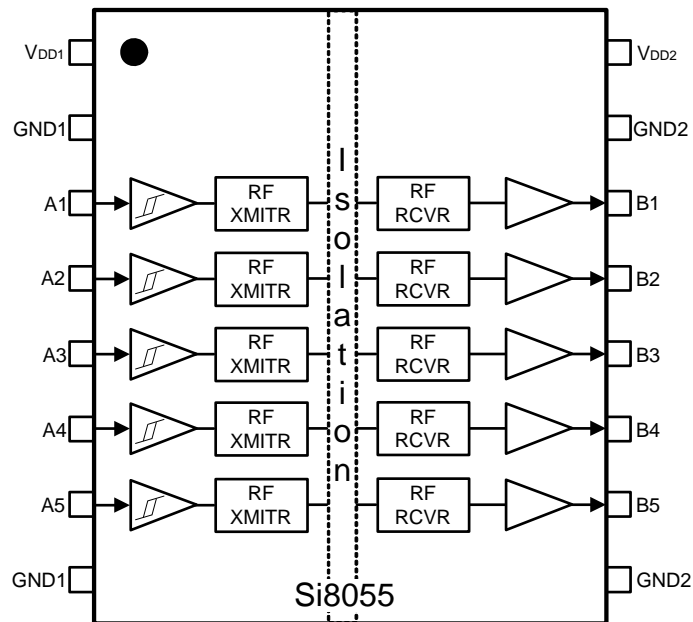
## 6. Pin Descriptions (Si8050)



| Name             | Pin# | Type           | Description                          |
|------------------|------|----------------|--------------------------------------|
| V <sub>DD1</sub> | 1    | Supply         | Side 1 power supply.                 |
| A1               | 2    | Digital Input  | Side 1 digital input.                |
| A2               | 3    | Digital Input  | Side 1 digital input.                |
| A3               | 4    | Digital Input  | Side 1 digital input.                |
| A4               | 5    | Digital Input  | Side 1 digital input.                |
| A5               | 6    | Digital Input  | Side 1 digital input.                |
| NC*              | 7    | NA             | No connect.                          |
| GND1             | 8    | Ground         | Side 1 ground.                       |
| GND2             | 9    | Ground         | Side 2 ground.                       |
| EN2              | 10   | Digital Input  | Side 2 active high enable on Si8050. |
| B5               | 11   | Digital Output | Side 2 digital output.               |
| B4               | 12   | Digital Output | Side 2 digital output.               |
| B3               | 13   | Digital Output | Side 2 digital output.               |
| B2               | 14   | Digital Output | Side 2 digital output.               |
| B1               | 15   | Digital Output | Side 2 digital output.               |
| V <sub>DD2</sub> | 16   | Supply         | Side 2 power supply.                 |

**\*Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V<sub>DD</sub> or tied to GND.

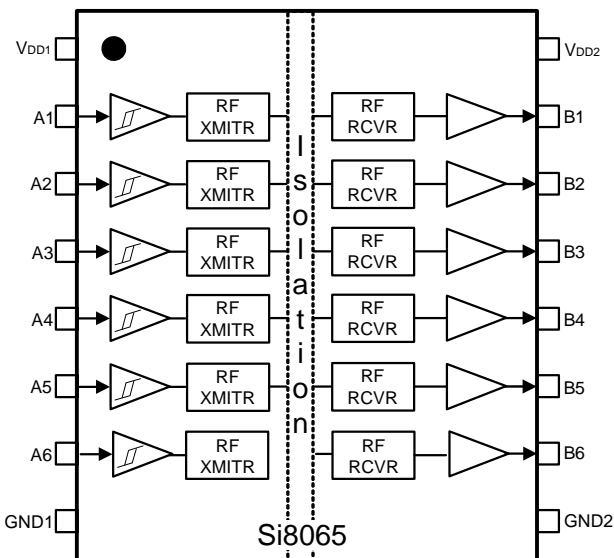
## 7. Pin Descriptions (Si8055)



| Name             | Pin# | Type           | Description            |
|------------------|------|----------------|------------------------|
| V <sub>DD1</sub> | 1    | Supply         | Side 1 power supply.   |
| GND1             | 2    | Ground         | Side 1 ground.         |
| A1               | 3    | Digital Input  | Side 1 digital input.  |
| A2               | 4    | Digital Input  | Side 1 digital input.  |
| A3               | 5    | Digital Input  | Side 1 digital input.  |
| A4               | 6    | Digital Input  | Side 1 digital input.  |
| A5               | 7    | Digital Input  | Side 1 digital input.  |
| GND1             | 8    | Ground         | Side 1 ground.         |
| GND2             | 9    | Ground         | Side 2 ground.         |
| B5               | 10   | Digital Output | Side 2 digital output. |
| B4               | 11   | Digital Output | Side 2 digital output. |
| B3               | 12   | Digital Output | Side 2 digital output. |
| B2               | 13   | Digital Output | Side 2 digital output. |
| B1               | 14   | Digital Output | Side 2 digital output. |
| GND2             | 15   | Ground         | Side 2 ground.         |
| V <sub>DD2</sub> | 16   | Supply         | Side 2 power supply.   |

# Si80xx-1kV

## 8. Pin Descriptions (Si8065)



| Name             | Pin# | Type           | Description            |
|------------------|------|----------------|------------------------|
| V <sub>DD1</sub> | 1    | Supply         | Side 1 power supply.   |
| A1               | 2    | Digital Input  | Side 1 digital input.  |
| A2               | 3    | Digital Input  | Side 1 digital input.  |
| A3               | 4    | Digital Input  | Side 1 digital input.  |
| A4               | 5    | Digital Input  | Side 1 digital input.  |
| A5               | 6    | Digital Input  | Side 1 digital input.  |
| A6               | 7    | Digital Input  | Side 1 digital input.  |
| GND1             | 8    | Ground         | Side 1 ground.         |
| GND2             | 9    | Ground         | Side 2 ground.         |
| B6               | 10   | Digital Output | Side 2 digital output. |
| B5               | 11   | Digital Output | Side 2 digital output. |
| B4               | 12   | Digital Output | Side 2 digital output. |
| B3               | 13   | Digital Output | Side 2 digital output. |
| B2               | 14   | Digital Output | Side 2 digital output. |
| B1               | 15   | Digital Output | Side 2 digital output. |
| V <sub>DD2</sub> | 16   | Supply         | Side 2 power supply.   |



## 9. Ordering Guide

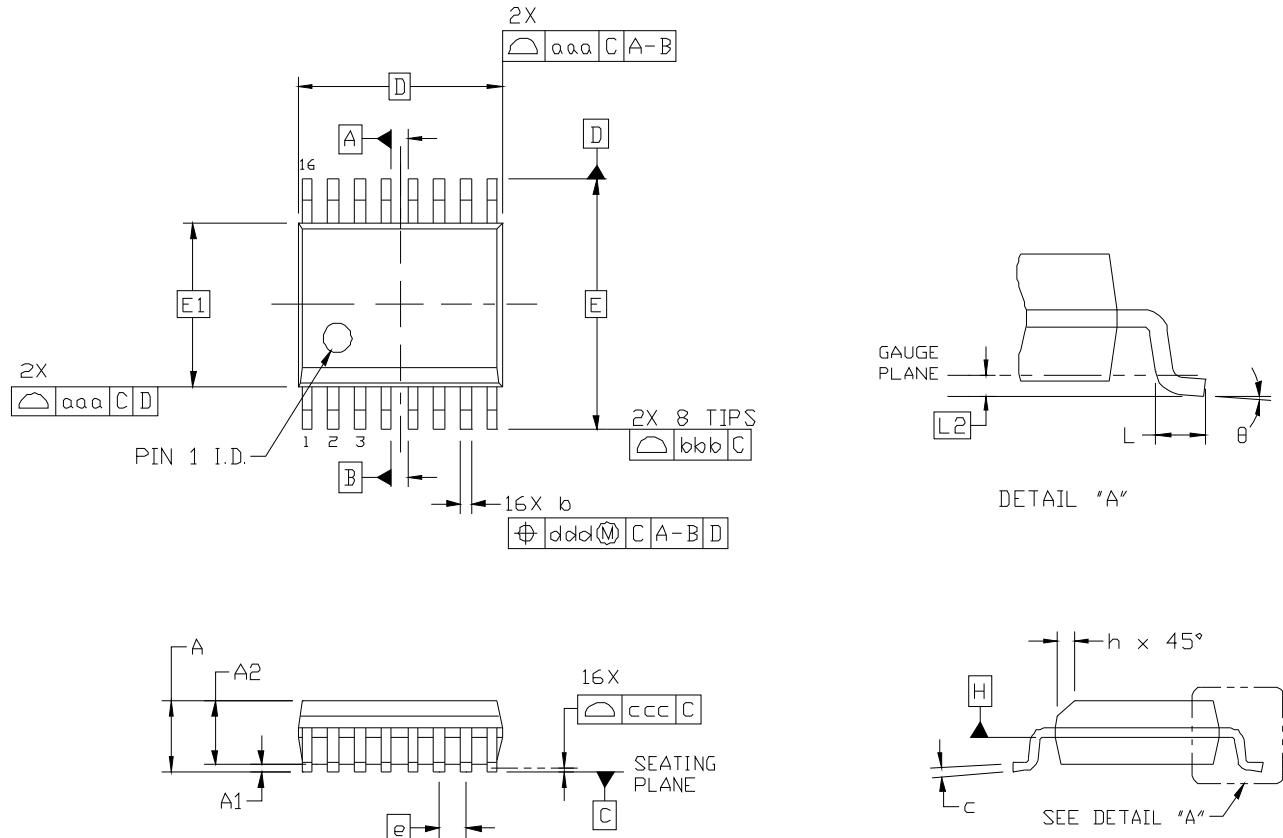
**Table 7. Ordering Guide for Valid OPNs<sup>1,2,3</sup>**

| Ordering Part Number (OPN)                                                                                                                                                                                                                                                                                                                              | Number of Inputs/Outputs | Default Output State | Output Enable Yes/No | Isolation Rating (kVrms) | Package |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------|----------------------|--------------------------|---------|
| <b>Si803x</b>                                                                                                                                                                                                                                                                                                                                           |                          |                      |                      |                          |         |
| Si8030AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 3                        | Low                  | Yes                  | 1                        | QSOP-16 |
| Si8035AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 3                        | Low                  | No                   | 1                        | QSOP-16 |
| <b>Si804x</b>                                                                                                                                                                                                                                                                                                                                           |                          |                      |                      |                          |         |
| Si8040AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 4                        | Low                  | Yes                  | 1                        | QSOP-16 |
| Si8045AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 4                        | Low                  | No                   | 1                        | QSOP-16 |
| <b>Si805x</b>                                                                                                                                                                                                                                                                                                                                           |                          |                      |                      |                          |         |
| Si8050AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 5                        | Low                  | Yes                  | 1                        | QSOP-16 |
| Si8055AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 5                        | Low                  | No                   | 1                        | QSOP-16 |
| <b>Si806x</b>                                                                                                                                                                                                                                                                                                                                           |                          |                      |                      |                          |         |
| Si8065AA-B-IU                                                                                                                                                                                                                                                                                                                                           | 6                        | Low                  | No                   | 1                        | QSOP-16 |
| <b>Notes:</b>                                                                                                                                                                                                                                                                                                                                           |                          |                      |                      |                          |         |
| <ol style="list-style-type: none"> <li>1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.</li> <li>2. "Si" and "SI" are used interchangeably.</li> <li>3. Add an "R" at the end of the device to denote tape and reel option.</li> </ol> |                          |                      |                      |                          |         |

# Si80xx-1kV

## 10. Package Outline: 16-Pin QSOP

Figure 6 illustrates the package details for the Si80xx in a 16-pin QSOP package. Table 8 lists the values for the dimensions shown in the illustration.



**Figure 6. 16-pin QSOP Package**

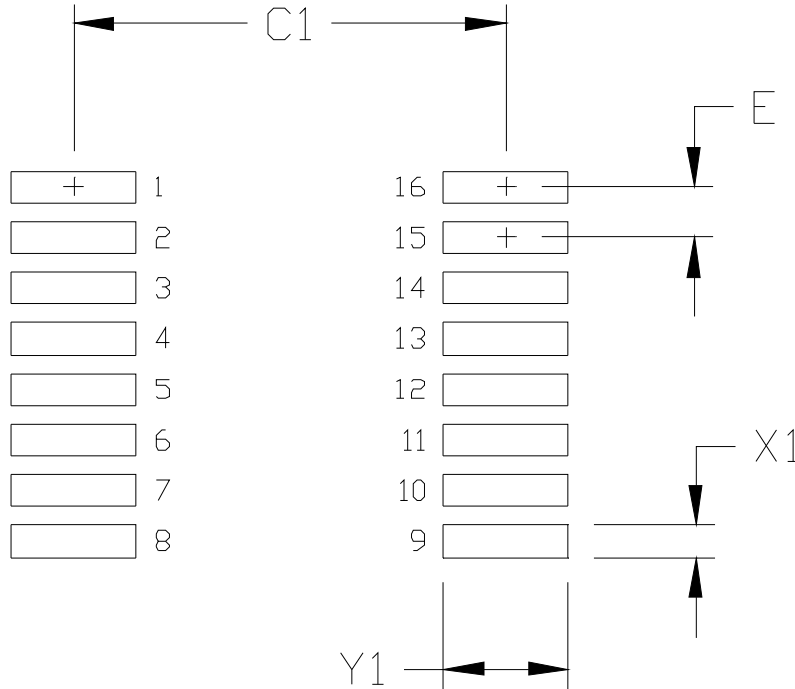
Table 8. Package Diagram Dimensions

| Dimension                                                                                                                                                                                                                                                                                                                                                                                 | Min       | Max  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------|
| A                                                                                                                                                                                                                                                                                                                                                                                         | —         | 1.75 |
| A1                                                                                                                                                                                                                                                                                                                                                                                        | 0.10      | 0.25 |
| A2                                                                                                                                                                                                                                                                                                                                                                                        | 1.25      | —    |
| b                                                                                                                                                                                                                                                                                                                                                                                         | 0.20      | 0.30 |
| c                                                                                                                                                                                                                                                                                                                                                                                         | 0.17      | 0.25 |
| D                                                                                                                                                                                                                                                                                                                                                                                         | 4.89 BSC  |      |
| E                                                                                                                                                                                                                                                                                                                                                                                         | 6.00 BSC  |      |
| E1                                                                                                                                                                                                                                                                                                                                                                                        | 3.90 BSC  |      |
| e                                                                                                                                                                                                                                                                                                                                                                                         | 0.635 BSC |      |
| L                                                                                                                                                                                                                                                                                                                                                                                         | 0.40      | 1.27 |
| L2                                                                                                                                                                                                                                                                                                                                                                                        | 0.25 BSC  |      |
| h                                                                                                                                                                                                                                                                                                                                                                                         | 0.25      | 0.50 |
| $\theta$                                                                                                                                                                                                                                                                                                                                                                                  | 0°        | 8°   |
| aaa                                                                                                                                                                                                                                                                                                                                                                                       | 0.10      |      |
| bbb                                                                                                                                                                                                                                                                                                                                                                                       | 0.20      |      |
| ccc                                                                                                                                                                                                                                                                                                                                                                                       | 0.10      |      |
| ddd                                                                                                                                                                                                                                                                                                                                                                                       | 0.25      |      |
| <b>Notes:</b>                                                                                                                                                                                                                                                                                                                                                                             |           |      |
| <ol style="list-style-type: none"> <li>All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li> <li>This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.</li> <li>Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol> |           |      |

# Si80xx-1kV

## 11. Land Pattern: 16-Pin QSOP

Figure 7 illustrates the recommended land pattern details for the Si80xx in a 16-pin QSOP package. Table 9 lists the values for the dimensions shown in the illustration.



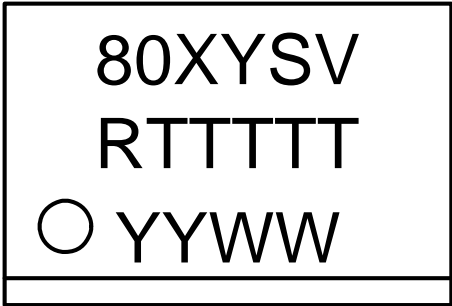
**Figure 7. 16-Pin QSOP PCB Land Pattern**

**Table 9. 16-Pin QSOP Land Pattern Dimensions**

| Dimension                                                                                                                                                                                                                                                                                                      | Feature            | (mm)  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------|
| C1                                                                                                                                                                                                                                                                                                             | Pad Column Spacing | 5.40  |
| E                                                                                                                                                                                                                                                                                                              | Pad Row Pitch      | 0.635 |
| X1                                                                                                                                                                                                                                                                                                             | Pad Width          | 0.40  |
| Y1                                                                                                                                                                                                                                                                                                             | Pad Length         | 1.55  |
| <b>Notes:</b>                                                                                                                                                                                                                                                                                                  |                    |       |
| <ol style="list-style-type: none"> <li>1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).</li> <li>2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.</li> </ol> |                    |       |

12. Top Markings

12.1. Top Marking (16-Pin QSOP)



12.2. Top Marking Explanation (16-Pin QSOP)

|                                                        |                                                                                        |                                                                                                                                                                                                                             |
|--------------------------------------------------------|----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Line 1 Marking:</b>                                 | Base Part Number<br>Ordering Options<br><br>(See Ordering Guide for more information). | 80 = Isolator product series<br>XY = Channel Configuration<br>X = # of data channels (6, 5, 4, 3)<br>Y = # of reverse channels (0)*<br>S = operating mode:<br>A = default output = low<br>V = Insulation rating<br>A = 1 kV |
| <b>Line 2 Marking:</b>                                 | RTTTTT = Mfg Code                                                                      | Manufacturing code from assembly house<br>"R" indicates revision                                                                                                                                                            |
| <b>Line 3 Marking:</b>                                 | YY = Year<br>WW = Work Week                                                            | Assigned by the Assembly House. Corresponds to the year and work week of the mold date.                                                                                                                                     |
| <b>*Note:</b> Si8035/45/55/65 have 0 reverse channels. |                                                                                        |                                                                                                                                                                                                                             |

## REVISION HISTORY

### Revision 1.1

July, 2018

- Removed references to default output high option.
- Updated "Features" on front page.
- Updated "3. Device Operation" on page 8.
- Updated "3.4. Fail-Safe Operating Mode" on page 11.
- Updated "9. Ordering Guide" on page 17.
- Updated "12. Top Markings" on page 21.

### Revision 1.0

January, 2014

### Revision 0.9

October, 2013

- Initial revision.



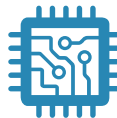
# SKYWORKS®

**Connecting Everyone  
and Everything,  
All the Time**



**Portfolio**

[www.skyworksinc.com](http://www.skyworksinc.com)



**Quality**

[www.skyworksinc.com/quality](http://www.skyworksinc.com/quality)



**Support & Resources**

[www.skyworksinc.com/support](http://www.skyworksinc.com/support)

**Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.**

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, Clockbuilder®, DSPLL®, ISOModem®, ProSLIC®, and SiPHY® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at [www.skyworksinc.com](http://www.skyworksinc.com), are incorporated by reference.

Skyworks Solutions, Inc. | Nasdaq: SWKS | [sales@skyworksinc.com](mailto:sales@skyworksinc.com) | [www.skyworksinc.com](http://www.skyworksinc.com)

USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540 |  