AT91SAM7X-EK
Evaluation Board
for AT91SAM7X and AT91SAM7XC

User Guide

Table of Contents

Section 1

Overview

1.1 Scope

The AT91SAM7X-EK and the AT91SAM7XC-EK evaluation kits enable evaluation capabilities and code development of applications running on the AT91SAM7X or the AT91SAM7XC microcontroller.

This guide focuses on the AT91SAM7X-EK board as a common evaluation platform for the AT91SAM7X and AT91SAM7XC devices in a 100-lead LQFP package.

1.2 Deliverables

The package contains the following items:

- a board marked AT91SAM7X-EK
- one A/B-type USB cable
- one crossed serial RS232 cable
- one RJ45 crossed Ethernet cable
- universal input AC/DC power supply with US and EU plug adapter
- one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 The AT91SAM7X-EK Evaluation Board

Depending on the model of the kit, the board is equipped with either an AT91SAM7X256 or an AT91SAM7XC256 (100-pin LQFP Green package) together with the following interfaces:

- USB device port
- DBGU serial communication port
- RS232 serial communication port with RTS/CTS
- JTAG/ICE debug interface connector
- serial CAN communication ports
- MII Ethernet 100-base TX with auto MDIX capability
- buffered analog input and PWM output

- Power LED and general-purpose LEDs
- DataFlash® card slot
- expansion connector
- Atmel® serial DataFlash
- One footprint for Atmel Serial EEPROM (MN11)

Section 2

Setting Up the AT91SAM7X-EK Evaluation Board

2.1 Electrostatic Warning

The AT91SAM7X-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM7X-EK evaluation board, the following items are required:

- the AT91SAM7X-EK evaluation board itself
- an A/B-type USB cable

or

- a DC USB power adapter (5V at 0.5 A) with USB A/B cable

Note: The kit is not delivered with a JTAG/ICE interface which is required to start evaluating the device.

2.3 Layout

Figure 2-1. Layout - Top View

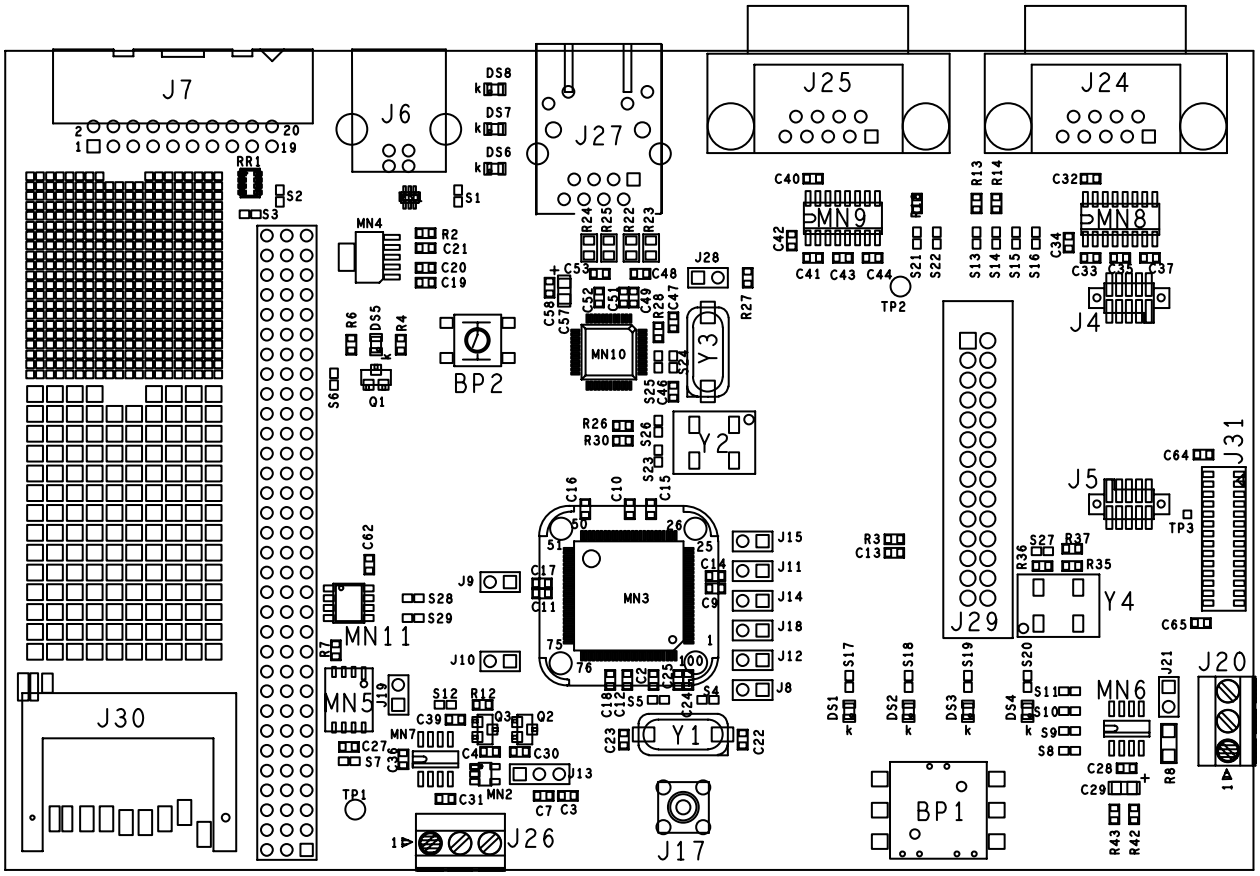
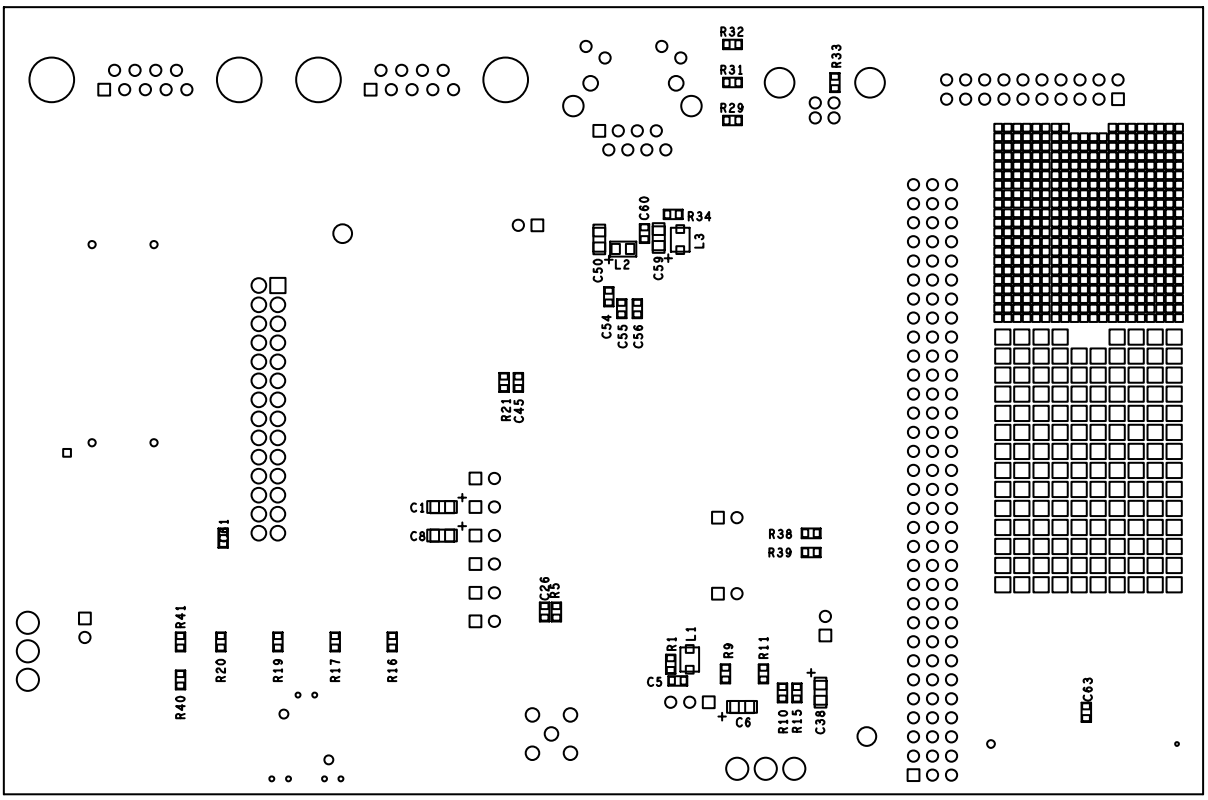


Figure 2-2. Layout - Bottom View



2.4 Powering Up the Board

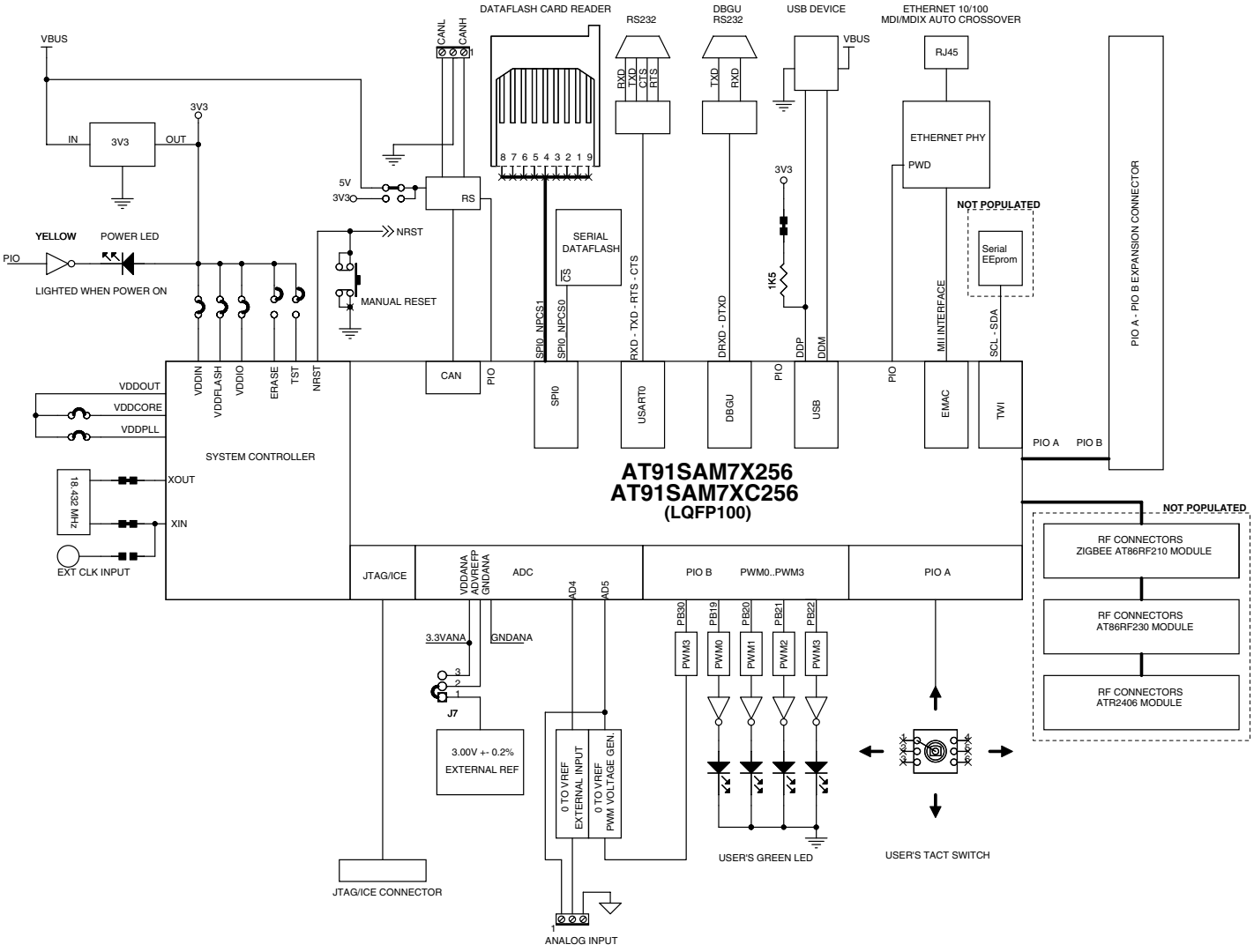
The AT91SAM7X-EK board is self-powered by the USB port or by a USB power adapter.

2.5 Getting Started

The AT91SAM7X-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the evaluation kit.

2.6 AT91SAM7X-EK Block Diagram

Figure 2-3. Block Diagram



Section 3

Board Description

3.1 AT91SAM7X Microcontroller

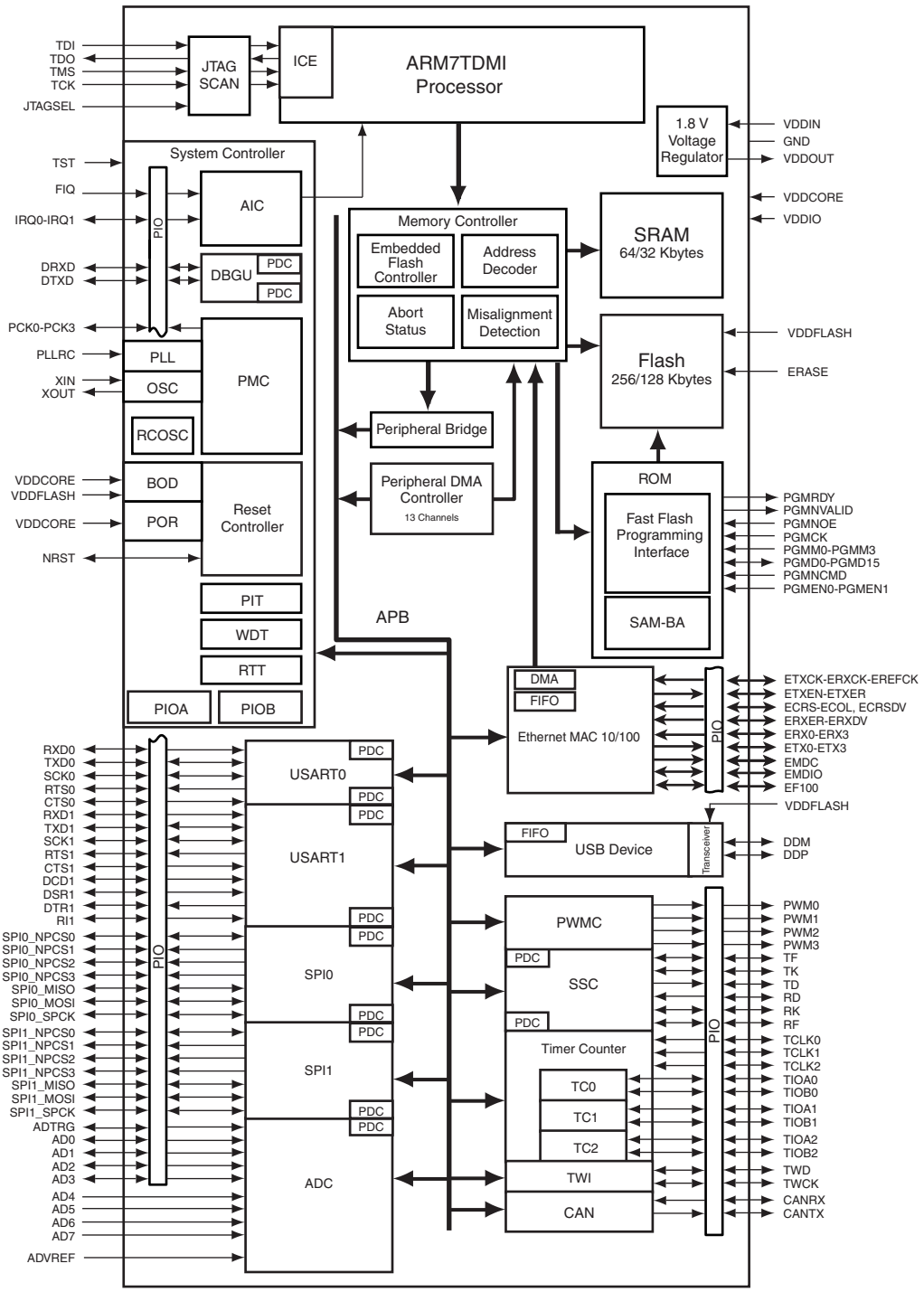
- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™, Debug Communication Channel Support
- Internal High-speed Flash
  - 256 Kbytes (AT91SAM7X256) Organized in 1024 Pages of 256 Bytes
  - 128 Kbytes (AT91SAM7X128) Organized in 512 Pages of 256 Bytes
    - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
    - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
    - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
    - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
    - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
  - 64 Kbytes (AT91SAM7X256)
  - 32 Kbytes (AT91SAM7X128)
- Memory Controller (MC)
  - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells and Low-power Factory-calibrated Brownout Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)

  - Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- Two Parallel Input/Output Controllers (PIO)
  - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Thirteen Peripheral DMA Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 1352-byte Configurable Integrated FIFOs
- One Ethernet MAC 10/100 base-T
  - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
  - Integrated 28-byte FIFOs and Dedicated DMA Channels for Transmit and Receive
- One Part 2.0A and Part 2.0B Compliant CAN Controller
  - Eight Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer

- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit Power Width Modulation Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support Only, All Two-wire Atmel EEPROMs Supported
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA™ Boot Assistance
  - Default Boot program
  - Interface with SAM-BA Graphic User Interface
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- 5V-tolerant I/Os, Including Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 100-lead LQFP Green Package

3.2 AT91SAM7X Block Diagram

Figure 3-1. Block Diagram



3.3 AT91SAM7XC Microcontroller

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™, Debug Communication Channel Support
- Internal High-speed Flash
  - 256 Kbytes (AT91SAM7XC256) Organized in 1024 Pages of 256 Bytes
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    - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
    - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
    - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
    - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
    - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
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  - Based on Power-on Reset Cells and Low-power Factory-calibrated Brownout Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
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  - Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
  - Four Programmable External Clock Signals
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  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
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  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
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- Two Parallel Input/Output Controllers (PIO)
  - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Seventeen Peripheral DMA Controller (PDC) Channels
- One Advanced Encryption System (AES)
  - 128-bit Key Algorithm, Compliant with FIPS PUB 197 Specifications
  - Buffer Encryption/Decryption Capabilities with PDC
- One Triple Data Encryption System (TDES)
  - Two-key or Three-key Algorithms, Compliant with FIPS PUB 46-3 Specifications
  - Optimized for Triple Data Encryption Capability
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 1352-byte Configurable Integrated FIFOs
- One Ethernet MAC 10/100 base-T
  - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
  - Integrated 28-byte FIFOs and Dedicated DMA Channels for Transmit and Receive
- One Part 2.0A and Part 2.0B Compliant CAN Controller
  - Eight Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
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  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
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  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
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  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
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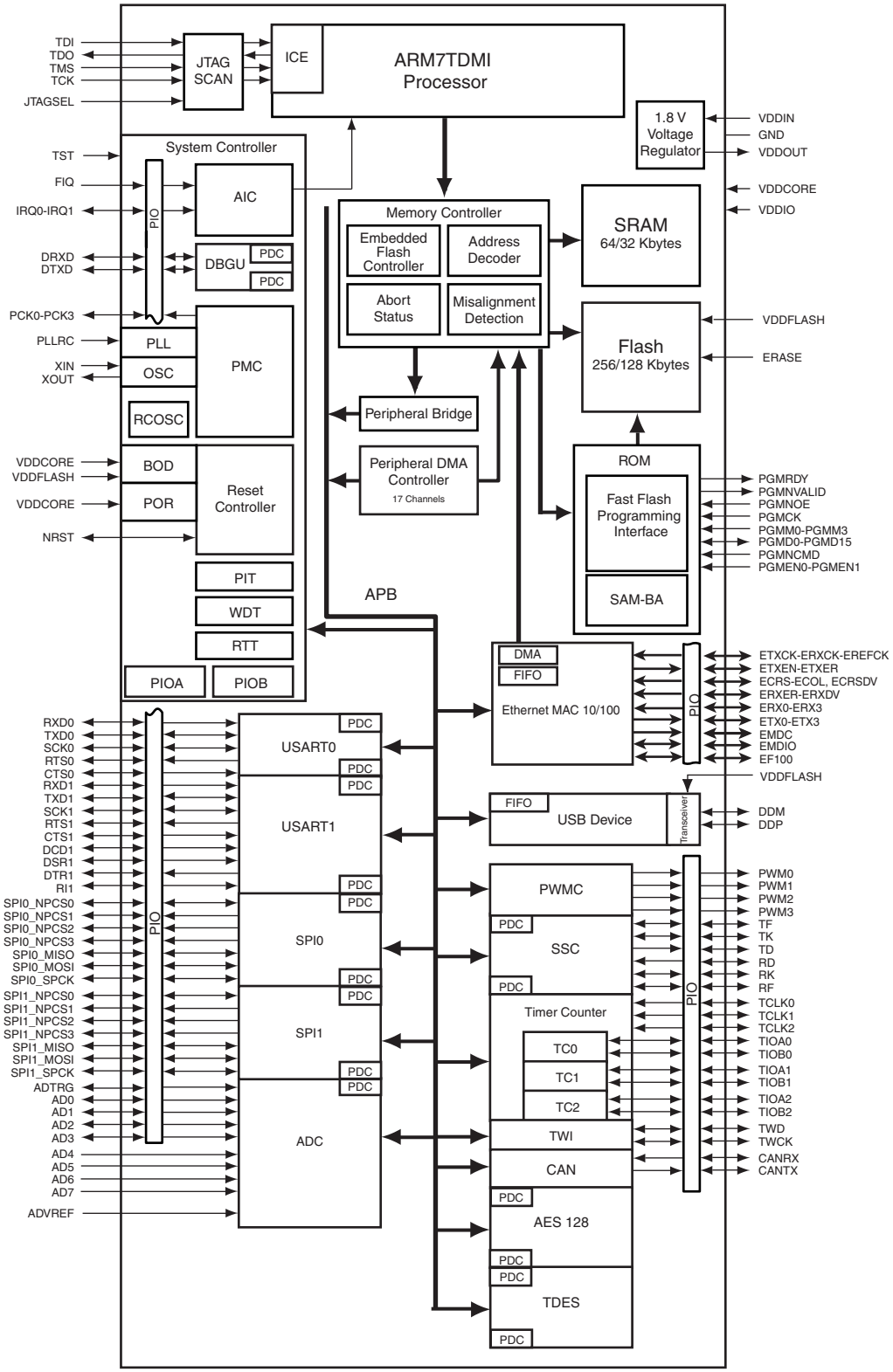
- 5V-tolerant I/Os, Including Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 100-lead LQFP Green Package

3.4 AT91SAM7XC Export Regulations Statement

These commodities, technology or software will be exported from France and the applicable Export Administration Regulations will apply. French, United States and other relevant laws, regulations and requirements regarding the export of products may restrict sale, export and re-export of these products; please assure you conduct your activities in accordance with the applicable relevant export regulations.

3.5 AT91SAM7XC Block Diagram

Figure 3-2. Block Diagram



3.6 Memory

- 256 Kbytes of Internal High-speed Flash
- 64 Kbytes of Internal High-speed SRAM
- Atmel serial DataFlash®
- One footprint for Atmel Serial EEPROM memory. The user can fit an AT24C128AN or AT24C256AN or AT24C512AN in 8S1 package as well as a cryptomemory AT88C25616C-SI

3.7 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- 32 KHz internal RC oscillator

3.8 Reset Circuitry

- Internal reset controller with a bidirectional reset pin
- External reset pushbutton

3.9 Power Supply Circuitry

- USB powered, the dynamic power consumption on VDDCORE is less than 90 mA at full speed when running out of the Flash. The total current at power-up is less than 100 mA.
- External power can be applied via USB Power adapter 5V 0.5A with USB A/B cable
- On-chip embedded VDDCORE 1.8V regulator
- On-board 3.3V 400 mA linear regulator

3.10 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
- One Serial interface (RS232 COM Port) via RS-232 DB9 male socket
- USB V2.0 Full-speed compliant, 12 Mbits per second (UDP)
- One CAN 2.0B communication port via the 3-position printed circuit terminal block
- One MII Ethernet 100-base TX (auto MDI/MDI-X crossover cable)

3.11 Analog Interface

- One selectable 0.2% 3.00V Vref or 3.3V ANA
- One 3-position printed circuit terminal block
- Two analog up to Vref inputs. One external user input and one back-looped with buffered PWM3 output.
- One buffered PWM3 analog output (up to Vref)

3.12 User Interface

- One 5-way joystick (4 directions and push for confirmation)
- Four general-purpose buffered green user LEDs (PWM controlled)

- One yellow power LED (can also be software controlled)

3.13 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU serial RS232 COM Port

3.14 Expansion Slot

- One DataFlash card slot
- All I/Os of the AT91SAM7X and the AT91SAM7XC are routed to peripheral extension connectors (J16). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J8	Opened	Erases all internal Flash memory when the board is powered. To do that, the user will have to close the J8 at least 200 ms.
J9	Opened	Do not use: Factory test mode. J9 is not populated
J10	Opened	Selects ICE mode or JTAG mode (Closed). J10 is not populated.
J11	Closed	VDDIN Jumper (1)
J12	Closed	VDDFLASH Jumper(1)
J13	1-2	ADVREF Jumper select 1-2: 3.00V Voltage reference 2-3: VDDANA
J14	Closed	VDDCORE Jumper (1)
J15	Closed	VDDIO Jumper (1)
J17	Opened	External XIN clock input. **S4 and S5 must be open.** J17 is not populated.
J18	Closed	VDDPLL Jumper (1)
J19	Closed	Enables the use of the NPCS00 (PA12).
J21	Closed	Enables 120 ohms CAN bus resistance termination.
J28	Closed	Enables Ethernet Auto MDIX control.
S1	Closed	Enables permanent pull up on USB DP.
S2	Closed	The System Reset signal (NRST) is connected to the ICE/JTAG socket (J7, pin 15).
S3	Opened	Disables 5V (VUSB) power supply on J16 extension connector.

Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
S4 - S5	Closed	Enables the use of 18.432MHz crystal. Must be open if an external clock is used.
S6	Closed	Enables the Power Led control (PB25).
S7	Opened	Disables Serial DataFlash write protect.
S8	Closed	Enables the use of the TXD CAN transceiver (PA20)
S9	Closed	Enables the use of the RXD CAN transceiver (PA19)
S10	Closed	Enables control of the Standby/Normal mode for CAN transceivers (PA2)
S11	Opened	Enables control of the Standby/Normal mode for CAN transceivers (PA2). **If S11 is closed, S10 must be open.**
S12	Closed	Enables the use of PWM3 Analog Output (PB30)
S13	Closed	Enables the use of the TXD0 signal (PA1)
S14	Closed	Enables the use of the RTS0 signal (PA3)
S15	Closed	Enables the use of the RXD0 signal (PA0)
S16	Closed	Enables the use of the CTS0 signal (PA4)
S17	Closed	Enables the use of the User LED DS1 (PB19)
S18	Closed	Enables the use of the User LED DS2 (PB20)
S19	Closed	Enables the use of the User LED DS3 (PB21)
S20	Closed	Enables the use of the User LED DS4 (PB22)
S21	Closed	Enables the use of the DBGU TXD signal (PA28)
S22	Closed	Enables the use of the DBGU RXD signal (PA27)
S23	Opened	ETHERNET MII is the default mode. To evaluate the RMII mode, the user change S23 to S26 configuration in the following way: S23 Closed, S24 Opened, S25 Closed, S26 Opened
S24	Closed	
S25	Opened	
S26	Closed	
S27	Opened	Reserved
S28	Closed	Enables the use of the SCL of MN11 (PA11)
S29	Closed	Enables the use of the SDA of MN11 (PA10)
TP1	N.A	GND Test point.
TP2	N.A	GND Test point.

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

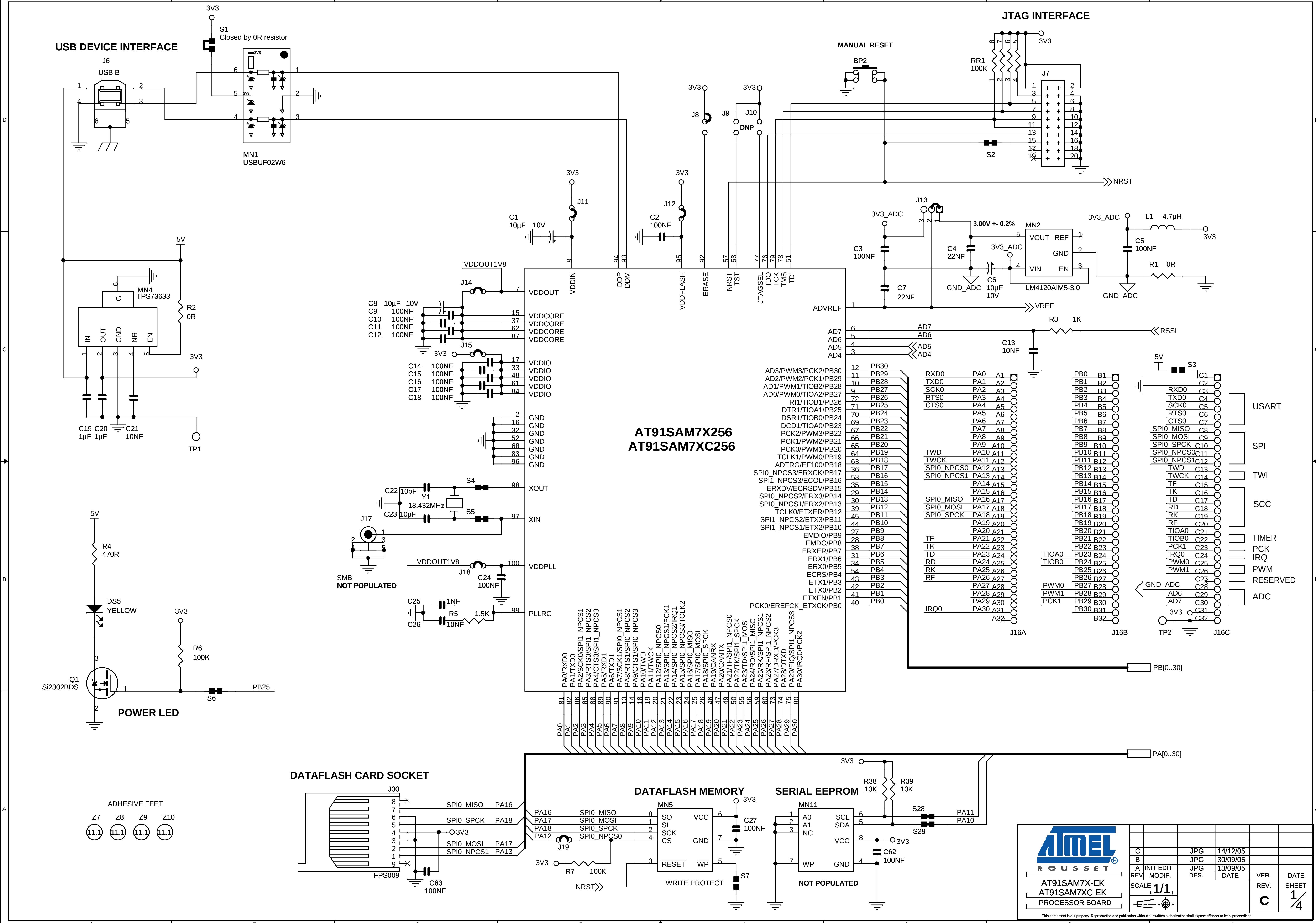
Section 5

Schematics

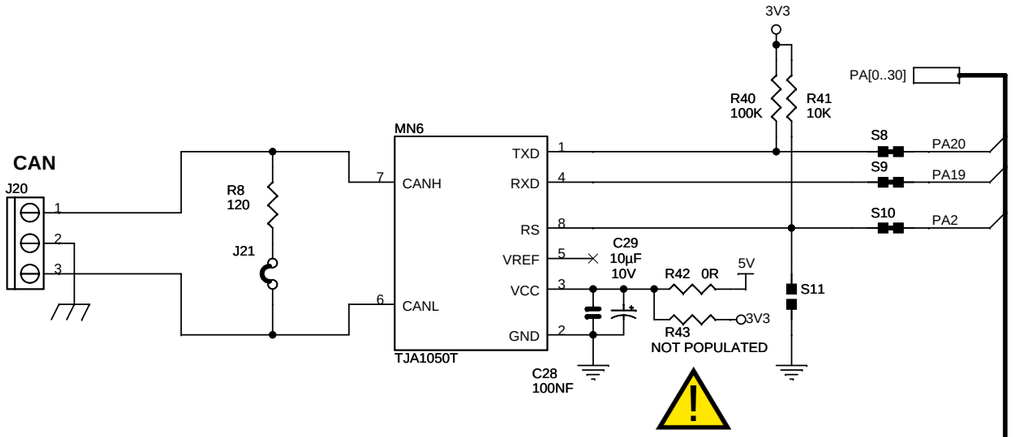
5.1 Schematics

This section contains the following schematics:

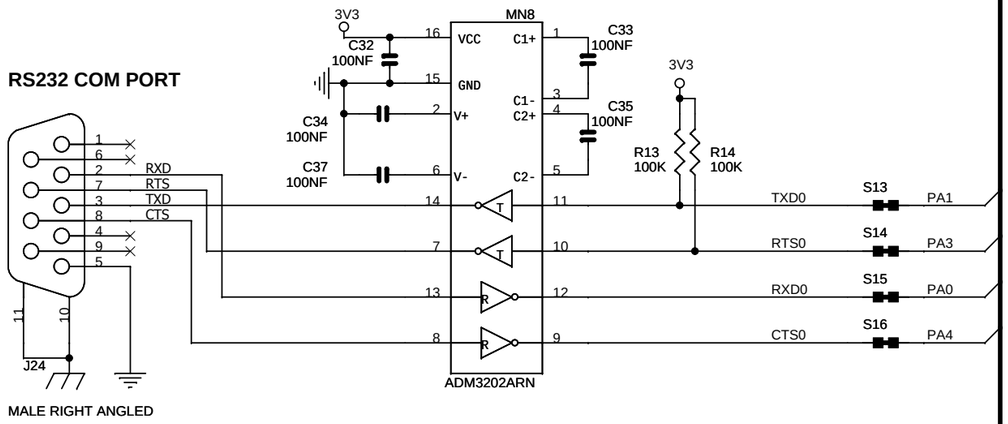
- Processor Board
- I/O
- Ethernet
- RF modules


USB DEVICE INTERFACE
J6
USB B
S1
Closed by 0R resistor
MN1
USBUF02W6
MANUAL RESET
BP2
JTAG INTERFACE
RR1
100K
J7
S2
NRST
J8
J9
J10
DNP
J11
J12
C1
10µF 10V
C2
100NF
VDDOUT1V8
J14
C8 10µF 10V
C9 100NF
C10 100NF
C11 100NF
C12 100NF
J15
C14 100NF
C15 100NF
C16 100NF
C17 100NF
C18 100NF
5V
MN4
TPS73633
R2
0R
IN OUT GND NR EN
3V3
C19 C20 C21
1µF 1µF 10NF
TP1
AT91SAM7X256
AT91SAM7XC256
VDDOUT
VDDCORE
VDDIO
GND
XOUT
XIN
VDDPLL
PLLRC
VDDIN
DDP
DDM
VDDFLASH
ERASE
NRST
TST
JTAGSEL
TDO
TCK
TMS
TDI
ADVREF
AD7
AD6
AD5
AD4
C22 10pF
Y1
18.432MHz
C23 10pF
S4
S5
J17
SMB
NOT POPULATED
J18
C24
100NF
C25
1NF
R5
1.5K
10NF
C26
J13
3V3_ADC
3.00V +- 0.2%
MN2
VOUT REF
GND
VIN EN
LM4120AIM5-3.0
C3
100NF
C4
22NF
C6
10µF
10V
C7
22NF
GND_ADC
VREF
L1 4.7µH
C5
100NF
R1 0R
R3 1K
RSSI
C13
10NF
S3
USART
SPI
TWI
SCC
TIMER
PCK
IRQ
PWM
RESERVED
ADC
J16A
J16B
TP2
J16C
PB[0..30]
PA[0..30]
R4
470R
DS5
YELLOW
R6
100K
Q1
Si2302BDS
S6
PB25
POWER LED
ADHESIVE FEET
Z7 Z8 Z9 Z10
DATAFLASH CARD SOCKET
J30
FPS009
C63
100NF
DATAFLASH MEMORY
MN5
SO VCC
SI
SCK
CS GND
RESET WP
C27
100NF
J19
R7 100K
S7
WRITE PROTECT
SERIAL EEPROM
MN11
A0 SCL
A1 SDA
NC
VCC
WP GND
NOT POPULATED
R38
10K
R39
10K
S28
S29
C62
100NF
ROUSSET
AT91SAM7X-EK
AT91SAM7XC-EK
PROCESSOR BOARD
C JPG 14/12/05
B JPG 30/09/05
A INIT EDIT JPG 13/09/05
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. C
SHEET 1/4
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.

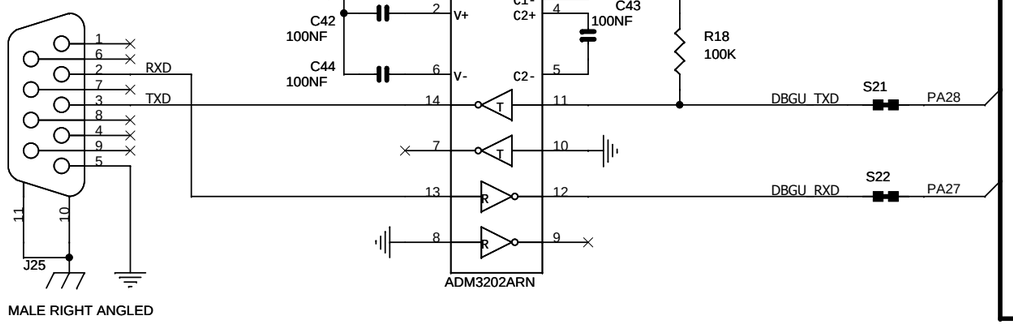
CAN

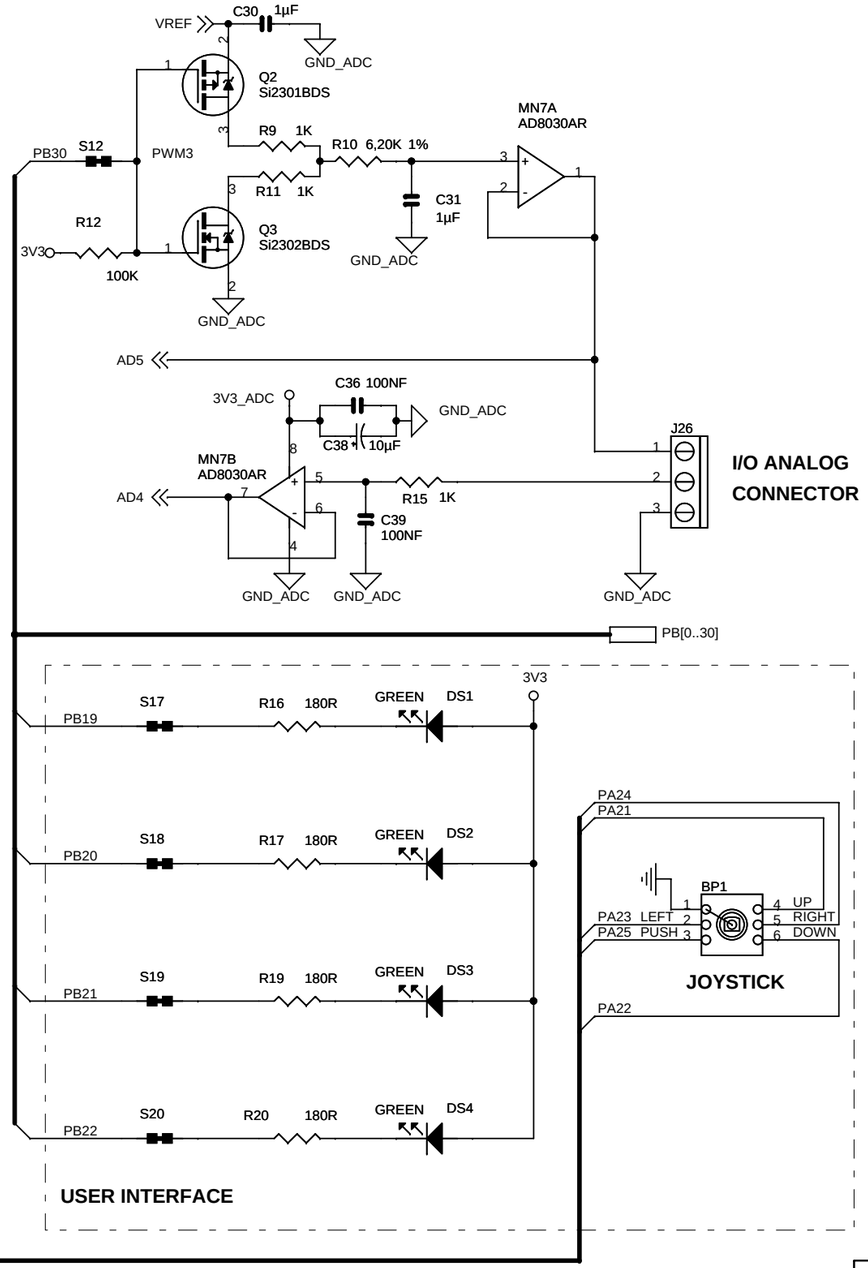


RS232 COM PORT



SERIAL DEBUG PORT





REV	MODIF.	DES.	DATE	VER.	DATE
C		JPG	14/12/05		
B		JPG	30/09/05		
A	INIT EDIT	JPG	13/09/05		

AT91SAM7X-EK
AT91SAM7XC-EK
I/O

SCALE 1/1

REV. C

SHEET 2/4

MII Factory setting

3V3 — R21 10K — Y2 (1 OE, 2 VSS, 4 VDD, 3 OUT, 50 MHz) — SG-8002JC-50.0000M-PCB — C45 100NF

PB[0..30]

Cut S23 — Cut S25 — Closed by 0R resistor S24 — Closed by 0R resistor S26

C46 22PF — C47 22PF — Y3 25MHz

MN10 (DM9161AE)

PB0	REFCK	42	REF_CLK/XT2	XT1	43
PB11	ETX3	17	TXD3	TX+	7
PB10	ETX2	18	TXD2	TX-	8
PB3	ETX1	19	TXD1	RX+	3
PB2	ETX0	20	TXD0	RX-	4
PB1	ETXEN	21	TX_EN		
		22	TX_CLK/ISOLATE		
PB14	ERX3	26	RXD3/PHYAD3		
PB13	ERX2	27	RXD2/PHYAD2		
PB6	ERX1	28	RXD1/PHYAD1		
PB5	ERX0	29	RXD0/PHYAD0		
PB17	ERXCK	34	RX_CLK/10BTSER		
PB15	ERXDV	37	RX_DV/TESTMODE		
PB12	ETXER	16	TX_ER/TXD4		
PB7	ERXER	38	RX_ER/RXD4/RPTR		
PB16	ECOL	36	COL/RMII	AVDDR	1
PB4	ECRS	35	CRS/PHYAD4	AVDDR	2
PB8	EMDC	24	MDC	AVDDT	9
PB9	EMDIO	25	MDIO	AGND	5
PB26	IRQ	32	MDINTR	AGND	6
		39	DISMDIX	AGND	46
		41	DVDD	BGRESG	47
		30	DVDD	BGRES	48
		23	DVDD	LEDMODE	31
		15	DGND	LED0/OP0	11
		33	DGND	LED1/OP1	12
		44	DGND	LED2/OP2	13
PB18		10	PWRDWN	CABLESTS/LINKSTS	14
NRST		40	RESET	N.C	45

3V3 — R26 10K — R27 10K — J28

3V3 — C54 100NF — C55 100NF — C56 100NF

C48 100NF

R22 49R9 1% — R23 49R9 1% — R24 49R9 1% — R25 49R9 1% — C53 100NF

L2 742792093 — VCCA — C49 100NF — C51 100NF — C52 100NF — C50 10V 10µF

J27 (RJ45 ETHERNET CONNECTOR, J00-0061)

1	TD+	TX+	1
4	CT		
2	TD-	TX-	2
3	RD+	RX+	3
5	CT		
6	RD-	RX-	6
7	NC		4
			5
8	1nF		7
			8

75 — 75 — 75 — 75 — 15 — 16

DS6 YELLOW FULL DUPLEX — R29 1K

DS7 GREEN SPEED 100 — R31 1K — 3V3

DS8 GREEN LINK&ACT — R32 1K

R28 6,80K 1% — R30 10K — 3V3

PB18 — NRST

NOT POPULATED: L3 4.7µH

3V3 — C57 10µF 10V — C58 100NF — C59 10µF 10V — C60 100NF — VCCA

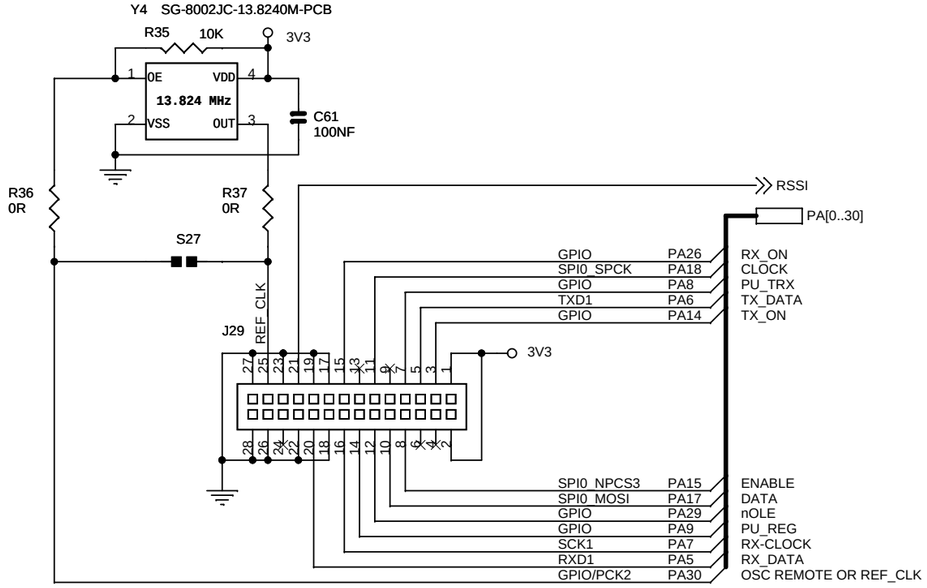
R33 0R — R34 0R

C		JPG	14/12/05		
B		JPG	30/09/05		
A	INIT EDIT	JPG	13/09/05		
REV	MODIF.	DES.	DATE	VER.	DATE

AT91SAM7X-EK
AT91SAM7XC-EK
ETHERNET

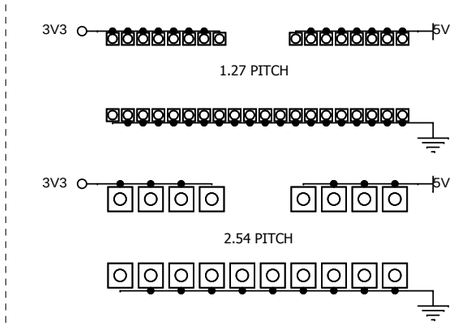
SCALE 1/1 — REV. C — SHEET 3/4

ATR2406 2.4 GHz RF CONNECTORS MODULE

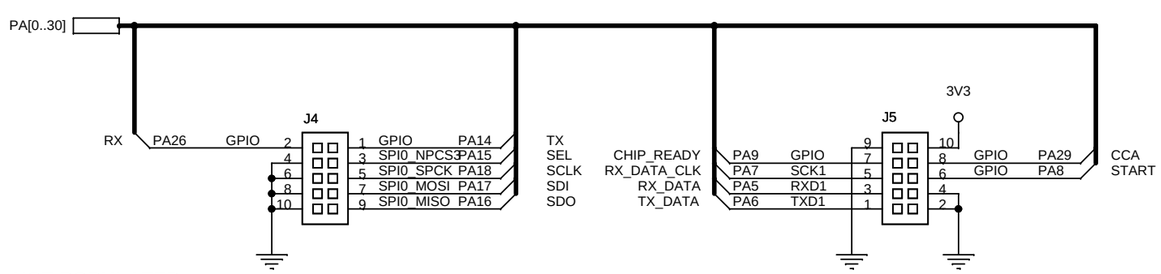


NOT POPULATED

USER'S GRID AERA

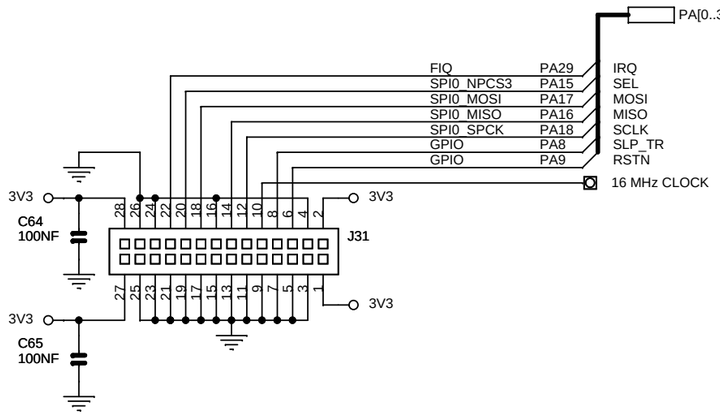


AT86RF210 ZIGBEE CONNECTORS MODULE



NOT POPULATED

AT86RF230 CONNECTORS MODULE



NOT POPULATED

REV	MODIF.	DES.	DATE	VER.	DATE
C		JPG	14/12/05		
B		JPG	30/09/05		
A	INIT EDIT	JPG	13/09/05		

AT91SAM7X-EK
AT91SAM7XC-EK
RF MODULES

SCALE 1/1

REV. C

SHEET 4/4

Section 6

Errata

6.1 DM9161A Ethernet Phy Connections

The Ethernet interface works as presented in the schematics, but the connections are not in compliance with Davicom recommendations.

To comply with Davicom recommendations on connecting this device, J27-4 and J27-5 (RJ45 connector, CT) should be connected to the VCCA side of L2. In the current schematics (ETHERNET, Sheet 3/4), the VCCA side of L2 is connected to MN10-1 and MN10-2 (DM9161A, AVDDR).

For additional information, refer to the Davicom datasheet for DM9161A and associated Application Notes available on http://www.davicom.com.tw/.

6.2 TWI line pullups for Fast Mode operation

In order to use the TWI in Fast Mode (up to 400 Kbits/s), the default 10 KΩ resistors R38 and R39 should be replaced by smaller values (e.g., 2.2 KΩ).

Note that there is no need to change the pull-up resistors if the TWI is used in Standard Mode (up to 100 Kbits/s).

Section 7

Revision History

7.1 Revision History

Table 7-1. Change History

Document	Comments	Change Request Ref.
6195A	First issue.	
6195B	Updated Figure 2-3 with new signal names. Updated document to show new product functionalities. New board block diagram and schematics issued.	05-430
6195C	Updated document to contain new product AT91SAM7XC. Added new section with Errata.	
6195D	Removed references to 32 Mbit serial DataFlash (AT45DB321C-CNC) in Section 1.3 and in Section 3.6. Inserted new Figure 2-3 and new schematics in Section 5.	2862
6195E	Added Errata Section 6.2 ”TWI line pullups for Fast Mode operation”	4084

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Atmel Europe
Le Krebs
8, rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines
Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-47-50
Fax: (33) 4-76-58-47-60

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6195E–ATARM–22-Mar-07