*Click **here** for production status of specific part numbers.*

MAX20012B

Automotive Low-Voltage 2-Channel Step-Down Controller

General Description

The MAX20012B is a dual-output, high-efficiency synchronous step-down controller IC that operates with a 3.0V to 5.5V input voltage range and provides a 0.5V to 1.5875V output voltage range. The controller architecture enables up to 12A of load current per phase. Channel one has an option to operate with two phases to deliver higher load current, making this device ideal for automotive point-of-load (PoL) and post-regulation applications.

The IC achieves ±2% output error over load, line, and temperature ranges. The IC features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions.

The MAX20012B is offered with factory-preset output voltages (see the *Selector Guide* for options). The I^2C interface supports dynamic voltage adjustment with programmable slew rates for each channel. Other features include programmable soft-start, overcurrent, and overtemperature protections.

Applications

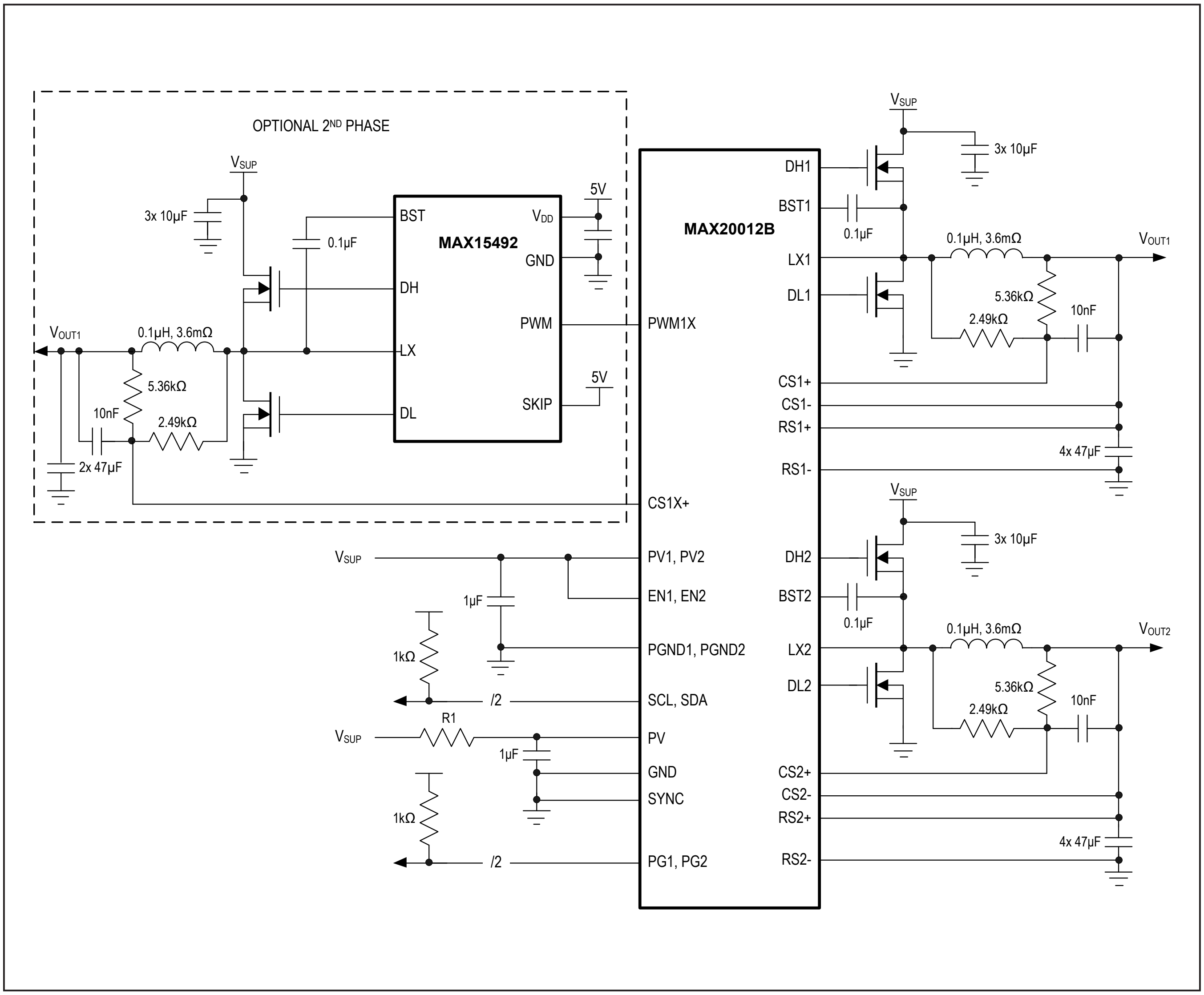
- Automotive

Benefits and Features

- 2-Channel High-Efficiency DC-DC Controller in a Small Solution Size
  - 3.0V to 5.5V Operating Supply Voltage
  - OUT1 Supports 24A (with Two Phases)
  - OUT2 Supports 12A
- High-Precision Regulator for Applications Processors
  - ±2% Output-Voltage Accuracy
  - Differential Remote Voltage Sensing
  - I^2C-Controlled Output Voltage: 0.5V to 1.27V in 10mV Steps
  - 0.625V to 1.5875V in 12.5mV Steps
  - Excellent Load-Transient Performance
- Low-Noise Features Reduce EMI
  - 2.2MHz Operation
  - Spread-Spectrum Option
  - Frequency-Synchronization Input/Output
  - Current-Mode, Forced-PWM, and Skip Operation
- Robust for the Automotive Environment
  - Individual Enable Inputs and PGOOD Outputs
  - Low $R_{DS(ON)}$ External FETs
  - Overtemperature and Short-Circuit Protection
  - 32-Pin (5mm x 5mm) TQFN with Exposed Pad
  - -40°C to +125°C Operating Temperature Range
  - AECQ-100 Qualified

***Ordering Information** appears at end of data sheet.*

Typical Operating Circuit



Absolute Maximum Ratings

PV1, PV2 to PGND_ ....-0.3V to +6V
PV to GND....................-0.3V to +6V
EN_, RS_+, RS_-, SYNC to GND....................-0.3V to PV + 0.3V
PG_, ADDR, SDA, SCL to GND....................-0.3V to +6V
DH_ to LX_....................-0.3V to BST_ + 0.3V
DL_ to PGND_ ....-0.3V to PV_ + 0.3V
BST_ to LX_....................-0.3V to +6V
LX_ to PGND_....................-0.3V to +18V
CS1+ to CS1-, CS2+ to CS2- ....-0.3V to +0.3V
CS_-, CS1X+ to GND....................-0.3V to +6V
PWM1X to GND ....-0.3V to PV + 0.3V
GND to PGND_ ....-0.3V to +0.3V
Output Short-Circuit Duration....................Continuous
Continuous Power Dissipation (T_A = +70°C) (Multilayer Board)
32-Pin TQFN (derate 34.5mW/°C above +70°C)...2758.6mW
Operating Temperature Range.................... -40°C to +125°C
Junction Temperature....................+150°C
Storage Temperature Range.................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow)....................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 32-PIN TQFN	
Package Code	T3255+6
Outline Number	21-0140
Land Pattern Number	90-0603
PACKAGE TYPE: 32-PIN SW TQFN	
Package Code	T3255Y+6
Outline Number	21-100041
Land Pattern Number	90-100066
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

($V_{PV} = V_{PV\_}$ = 5V, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{IN\_}$	Fully operational	3.0		5.5	V
Undervoltage Lockout (UVLO)		Rising		2.9	3	V
		Falling	2.6	2.7		
UVLO Hysteresis				200		mV
Supply Current (Skip Mode)	$I_{IN\_}$	EN1 = high, EN2 = low, $V_{CS1X+} = V_{PV\_}$, V_{CS1} = 0V (Note 2)		570		µA
		EN1 = EN2 = high, $V_{CS1X+} = V_{PV\_}$, $V_{CS1} = V_{CS2}$ = 0V (Note 2)		1100		
Shutdown Supply Current	I_{SHDN}	EN1 = EN2 = low		5	10	µA

Electrical Characteristics (continued)

(V_{PV} = $V_{PV\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}	Internally generated		2.0	2.2	2.4	MHz
Spread Spectrum	Δf/f	CONFIG.SS = 1			+3		%
Voltage Accuracy	V_{OUT}	$V_{CS\_}$ = 0mV to 50mV, 3.0V ≤ $V_{PV\_}$ ≤ 5.5V (Note 2)	0.80V to 1.5875V	-2		+2	%
			0.50V to 0.79V	-15		+15	mV
High-Side Output-Drive Resistance		Rising			1.5		Ω
		Falling			0.7		
Low-Side Output-Drive Resistance		Rising			0.7		Ω
		Falling			0.3		
Peak Current-Limit Threshold	V_{LIM}	Measured across V_{CS} (Note 2)			60		mV
Skip Current Threshold	V_{SKIP}	Measured across V_{CS} (Note 2			12		mV
Maximum Duty Cycle		PWM mode		90		99	%
Minimum On-Time					35		ns
LX_ Leakage Current		V_{PV} = $V_{PV\_}$ = 6V, LX_ = PGND_ or PV_, T_A = +25°C			0.1		µA
OUT2 Phase Shift		(Note 3)			180		Degrees
CS_- Pulldown Resistance		$V_{EN\_}$ = 0V			5		Ω
THERMAL OVERLOAD							
Thermal-Shutdown Temperature		T_J rising			165		°C
Hysteresis					15		°C
POWER GOOD							
PG_ Overvoltage (OV) Threshold (Rising)		Percentage of nominal output, blanked during slewing	0.5V < V_{OUT} < 0.79V	105	108	111	%
			0.8V < V_{OUT} < 1.5875V	106	108	110	
PG_ Undervoltage (UV) Threshold (Falling)		Percentage of nominal output, blanked during slewing	0.5V < V_{OUT} < 0.79V	89	92	95	%
			0.8V < V_{OUT} < 1.5875V	90	92	94	
Active Timeout Period					256		Clocks
UV/OV Propagation Delay					5		µs
PG_ Output High Leakage Current		T_A = +25°C				1	µA
PG_ Output Low Level		3.0V ≤ $V_{PV\_}$ ≤ 5.5V, sinking 2mA				0.2	V

Electrical Characteristics (continued)

(V_{PV} = $V_{PV\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

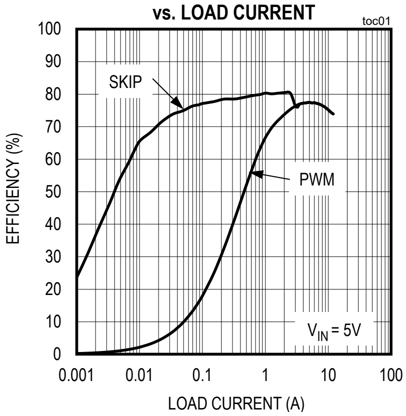
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (EN_, ADDR)						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis				0.1		V
Input Leakage Current		0V ≤ V_{PV} ≤ 5.5V, T_A = +25°C		1		µA
Enable Time		Rising EN_ to first rising DH_		140		µs
PWM1X						
Output Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output High	V_{OH}	$V_{PV\_}$ = V_{PV} = 5.0V, I_{SOURCE} = 3mA	4.2			V
DIGITAL INPUT (SYNC)						
Input High Level	V_{IH}		1.8			V
Input Low Level	V_{IL}				0.4	V
Input Hysteresis				0.1		V
Input Pulldown				100		kΩ
Input Frequency Range			1.8		2.6	MHz
SYNC OUTPUT (CONFIG.SO[1:0] = 10)						
Output Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output High	V_{OH}	$V_{PV\_}$ = V_{PV} = 5.0V, I_{SOURCE} = 3mA	4.2			V
DIGITAL INPUTS (SDA, SCL)						
Input High Level	V_{IH_I2C}		1.2			V
Input Low Level	V_{IL_I2C}				0.5	V
Input Hysteresis				0.1		V
Input Leakage Current		0V ≤ V_{PV} ≤ 5.5V, T_A = +25°C		1		µA
I²C INTERFACE						
Clock Frequency	f_{SCL}				1	MHz
Setup Time (Repeated) START	$t_{SU:STA}$	(Note 3)	160			ns
Hold Time (Repeated) START	$t_{HD:STA}$	(Note 3)	160			ns
SCL Low Time	t_{LOW}	(Note 3)	160			ns
SCL High Time	t_{HIGH}	(Note 3)	60			ns
Data Setup Time	$t_{SU:DAT}$	(Note 3)	50			ns
Data Hold Time	$t_{HD:DAT}$	(Note 3)	0		70	ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 3)	160			ns
Spike Suppression				20		ns
SDA Output Low	V_{OL_SDA}	I_{SINK} = 13mA			0.4	V

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.
Note 2: $V_{CS\_}$ = (V_{CS_+}) - (V_{CS_-}).
Note 3: Specifications are guaranteed by design, not production tested.

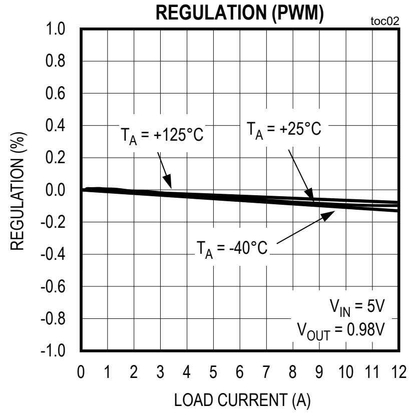
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

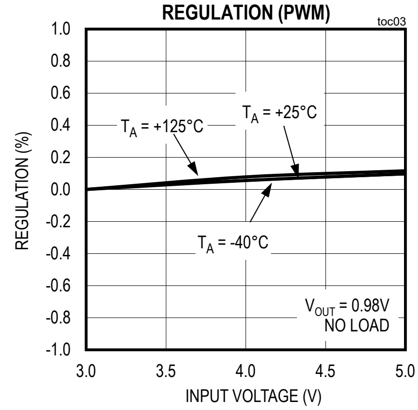
OUT1 EFFICIENCY vs. LOAD CURRENT



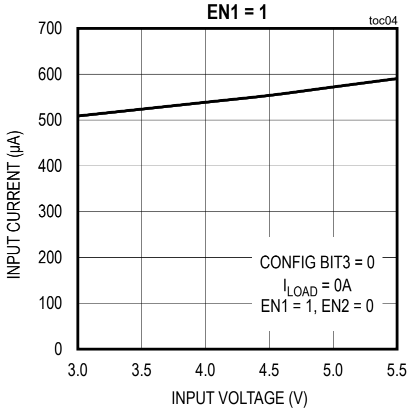
OUT1 LOAD REGULATION (PWM)



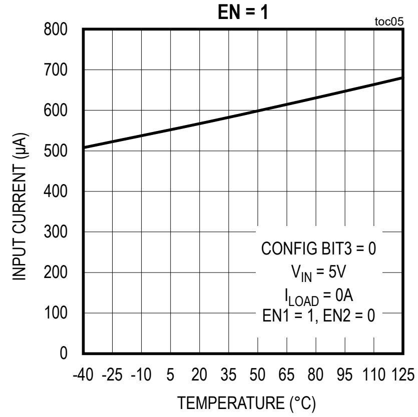
OUT1 LINE REGULATION (PWM)



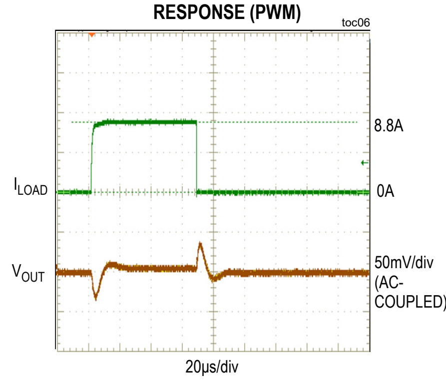
SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP), EN1 = 1



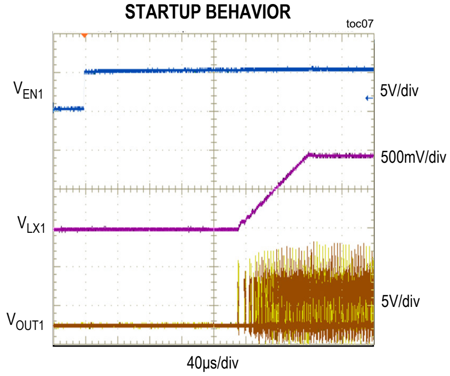
SUPPLY CURRENT vs. TEMPERATURE (SKIP), EN = 1



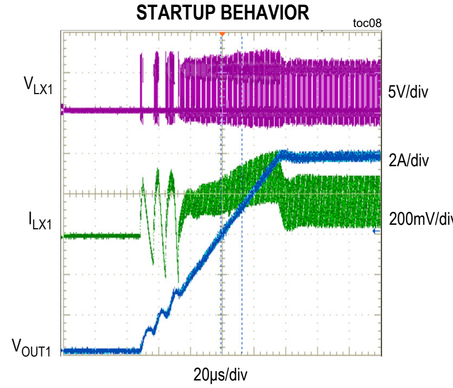
OUT1 DUAL MODE LOAD-TRANSIENT RESPONSE (PWM)



OUT1 0.1Ω LOAD STARTUP BEHAVIOR

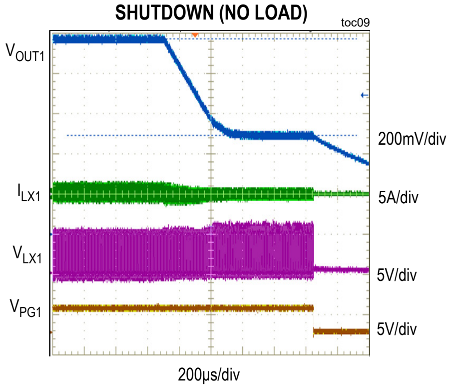


OUT1 DUAL MODE 0.2Ω LOAD STARTUP BEHAVIOR

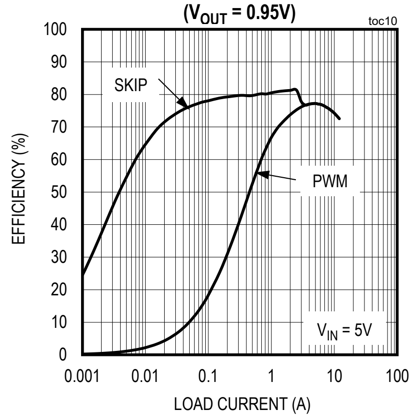


(T_A = +25°C, unless otherwise noted.)

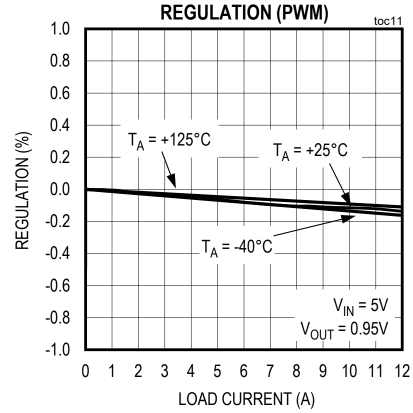
OUT1 DUAL MODE SHUTDOWN (NO LOAD)



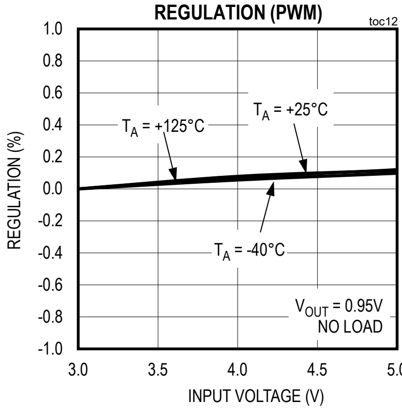
OUT2 EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.95V)



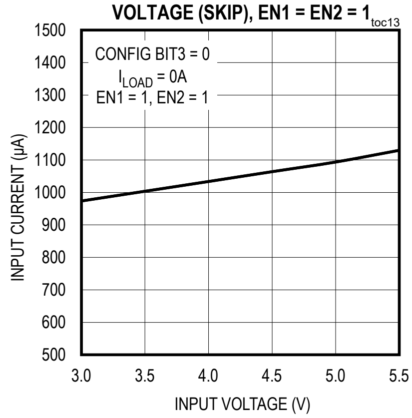
OUT2 LOAD REGULATION (PWM)



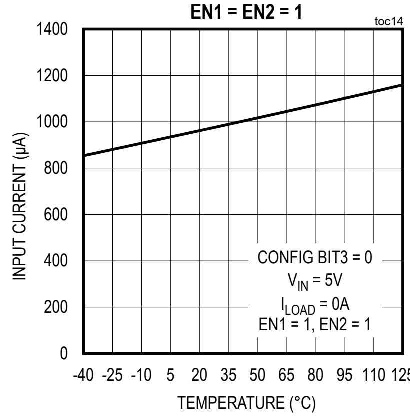
OUT2 LINE REGULATION (PWM)



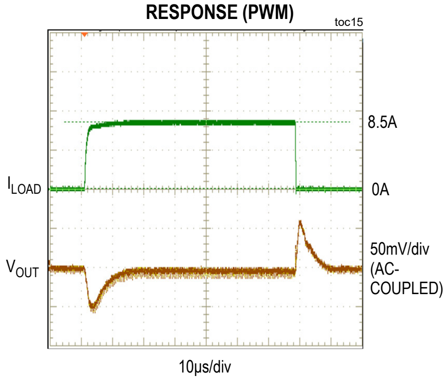
SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP), EN1 = EN2 = 1



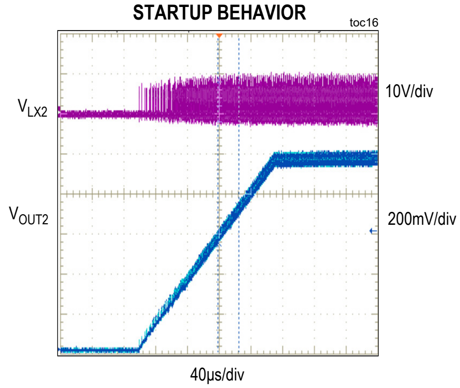
SUPPLY CURRENT vs. TEMPERATURE (SKIP), EN1 = EN2 = 1



OUT2 LOAD-TRANSIENT RESPONSE (PWM)



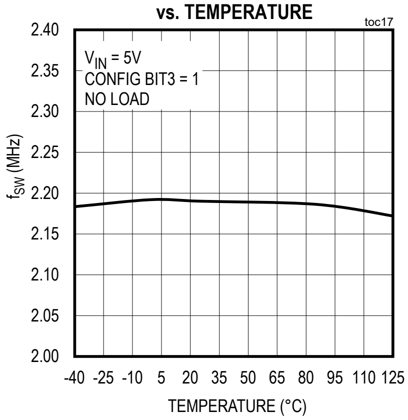
OUT2 0.2Ω LOAD STARTUP BEHAVIOR



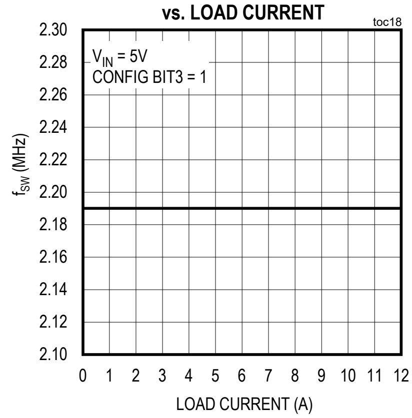
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

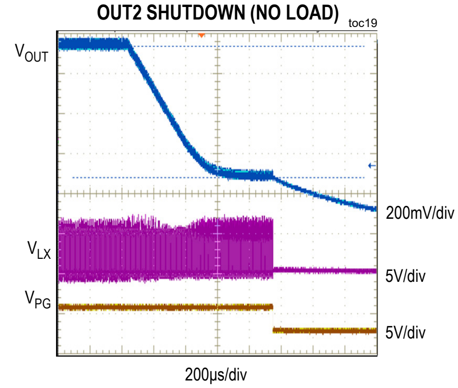
SWITCHING FREQUENCY vs. TEMPERATURE



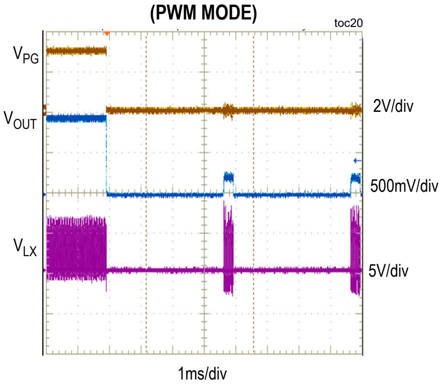
SWITCHING FREQUENCY vs. LOAD CURRENT



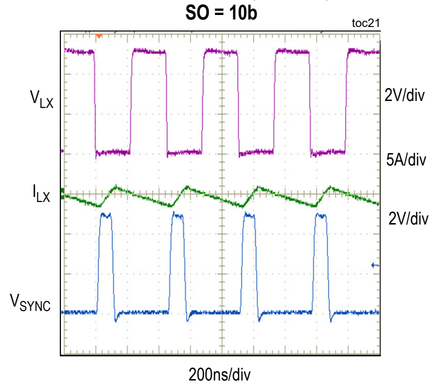
OUT2 SHUTDOWN (NO LOAD)



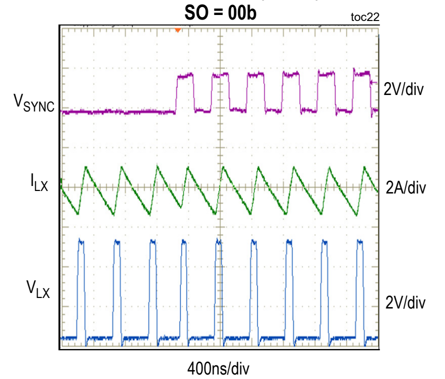
SHORT CIRCUIT (PWM MODE)



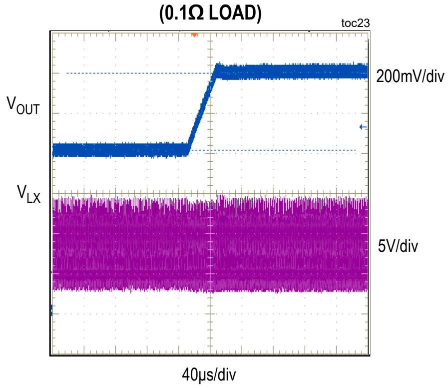
SYNC FUNCTION (OUTPUT), SO = 10b



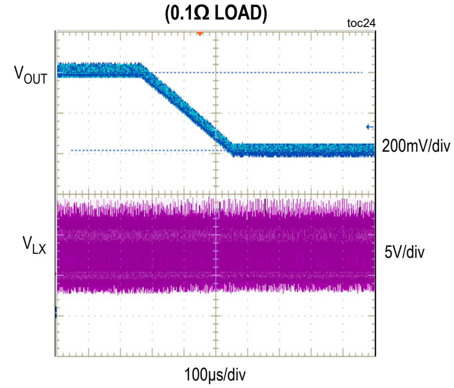
SYNC FUNCTION (INPUT), SO = 00b



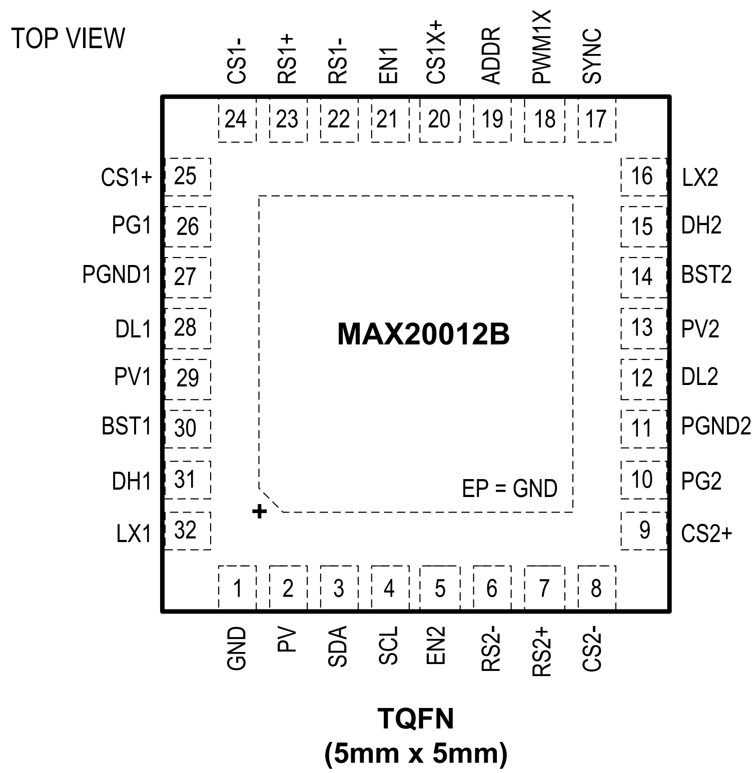
DVS RISING 0.8V TO 1.18V (0.1Ω LOAD)



DVS FALLING 1.18V TO 0.8V (0.1Ω LOAD)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	GND	Analog Ground
2	PV	Analog Input Supply. Connect a 1µF ceramic capacitor from PV to GND. Connect PV to PV1 and PV2 through a 10Ω resistor.
3	SDA	I2C Data I/O
4	SCL	I2C Clock Input
5	EN2	Active-High Digital Enable Input for DCDC2. Drive EN2 high for normal operation. Connect EN2 to GND if DCDC2 is not used.
6	RS2-	DCDC2 Remote Voltage-Sense Negative Input
7	RS2+	DCDC2 Remote Voltage-Sense Positive Input
8	CS2-	Current-Sense Negative Input for DCDC2. Connect CS2- to the negative side of the current-sense element.
9	CS2+	Current-Sense Positive Input for DCDC2. Connect CS2+ to the positive side of the current-sense element. See the *Current-Limit/Short-Circuit Protection* section.

PIN	NAME	FUNCTION
10	PG2	Open-Drain DCDC2 Reset Output. This output remains low for 120µs after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull up PG2 with an external resistor.
11	PGND2	Power Ground for DCDC2
12	DL2	Low-Side Gate Drive for DCDC2
13	PV2	Input-Voltage Pin for DCDC2. Bypass this pin with enough input capacitance to supply current to the buck controller. Connect PV1 and PV2 together externally. See the *Input Capacitor* section.
14	BST2	Bootstrap Capacitor for High-Side Driver of Buck 2. Connect a 0.1µF from LX2 to BST2.
15	DH2	High-Side Gate Drive for DCDC2
16	LX2	Inductor Connection for DCDC2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
17	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency forced-PWM mode operation. When configured as an output, connect SYNC to other devices' SYNC inputs.
18	PWM1X	PWM Output for Optional 2nd Phase of DCDC1. Connect to the MAX15492 PWM pin. If unused, leave PWM1X unconnected.
19	ADDR	I^2C Address Select. Connect to GND or PV to select between two different I^2C addresses. See the *Selector Guide* for default I^2C settings.
20	CS1X+	Current-Sense Positive Input for the 2nd Phase of DCDC1. Connect CS1X+ to the positive side of the current-sense element. To disable phase 2, short CS1X+ to PV.
21	EN1	Active-High Digital Enable Input for DCDC1. Drive EN1 high for normal operation. Connect EN1 to GND if DCDC1 is not used.
22	RS1-	DCDC1 Remote Voltage-Sense Negative Input
23	RS1+	DCDC1 Remote Voltage-Sense Positive Input
24	CS1-	Current-Sense Negative Input for DCDC1. Connect CS1- to the negative side of the current-sense element.
25	CS1+	Current-Sense Positive Input for DCDC1. Connect CS1+ to the positive side of the current-sense element. See the *Current-Limit/Short-Circuit Protection* section.
26	PG1	Open-Drain DCDC1 Reset Output. This output remains low for 120µs after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull up PG1 with an external resistor.
27	PGND1	Power Ground for DCDC1
28	DL1	Low-Side Gate Drive for DCDC1
29	PV1	Input-Voltage Pin for DCDC1. Bypass this pin with enough input capacitance to supply current to the buck controller. Connect PV1 and PV2 together externally. See the *Input Capacitor* section.
30	BST1	Bootstrap Capacitor for High-Side Driver of DCDC1. Connect a 0.1µF from LX1 to BST1.
31	DH1	High-Side Gate Drive of DCDC1
32	LX1	Inductor Connection for DCDC1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
—	EP	Exposed Pad. Connect EP to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND1, PGND2, and GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

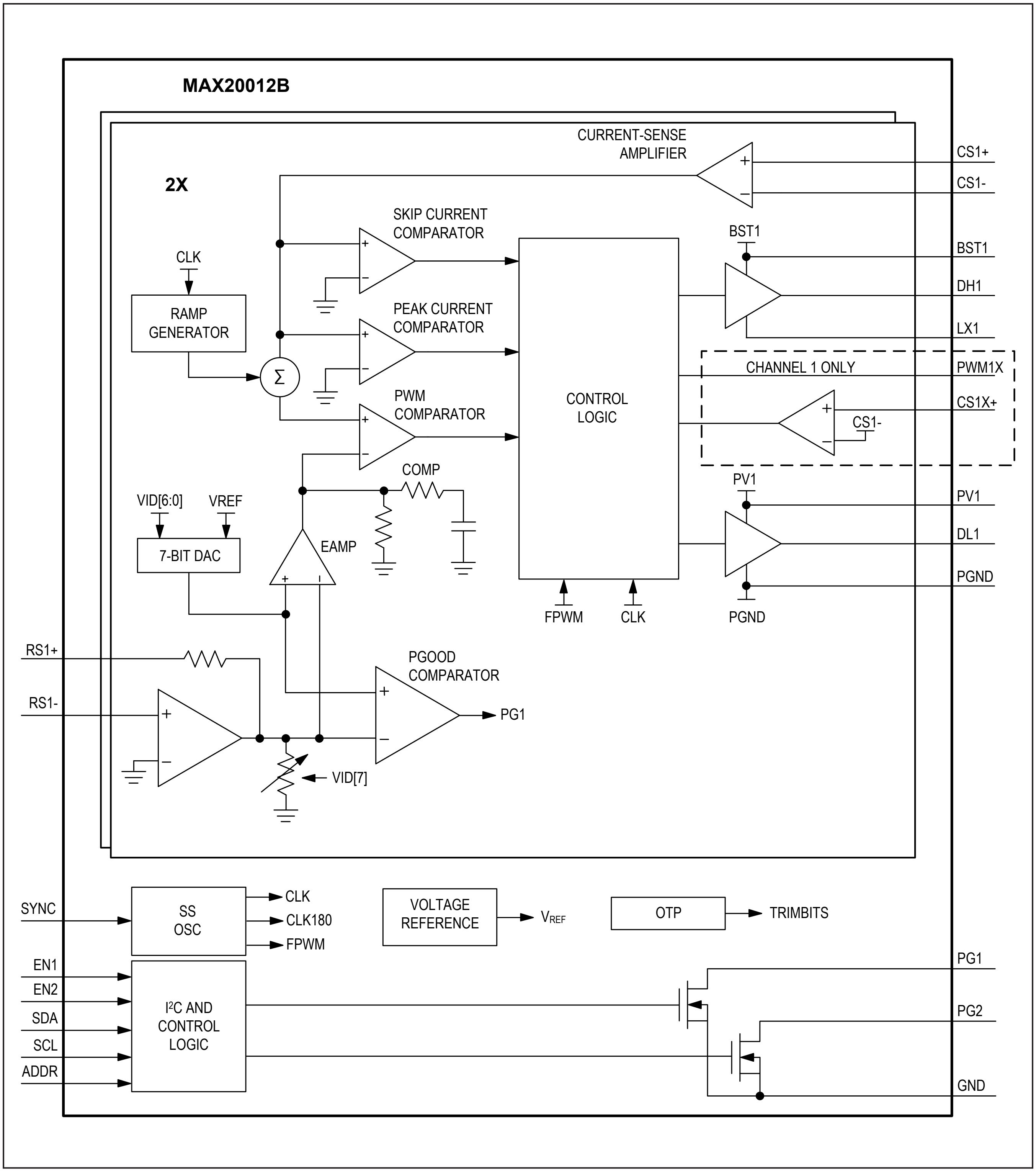


Figure 1. Internal Block Diagram

Detailed Description

The MAX20012B is a dual-output, high-efficiency synchronous step-down controller IC that operates with a 3.0V to 5.5V input voltage range and provides a 0.50V to 1.5875V output voltage range. The IC delivers up to 12A of load current per channel and achieves ±2% output error over load, line, and temperature ranges. The IC can operate as a 2-phase controller to deliver currents in excess of 21A.

The PWM input forces the IC either into a 2.2MHz fixed-frequency PWM mode or a low-power pulse-frequency modulation mode (skip). Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency. The I²C-programmable synchronization I/O (SYNC) enables system synchronization.

The IC is offered with a factory-preset output voltage that is dynamically adjustable through the I²C interface. The output voltage can be set to any desired value between 0.50V to 1.5875V.

Additional features include fixed power-good delay, overcurrent, and overtemperature protections (Figure 1).

I²C Interface

The IC features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 1MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 2 shows the 2-wire interface timing diagram.

A master device communicates to the IC by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. The IC's SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SDA and SCL inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

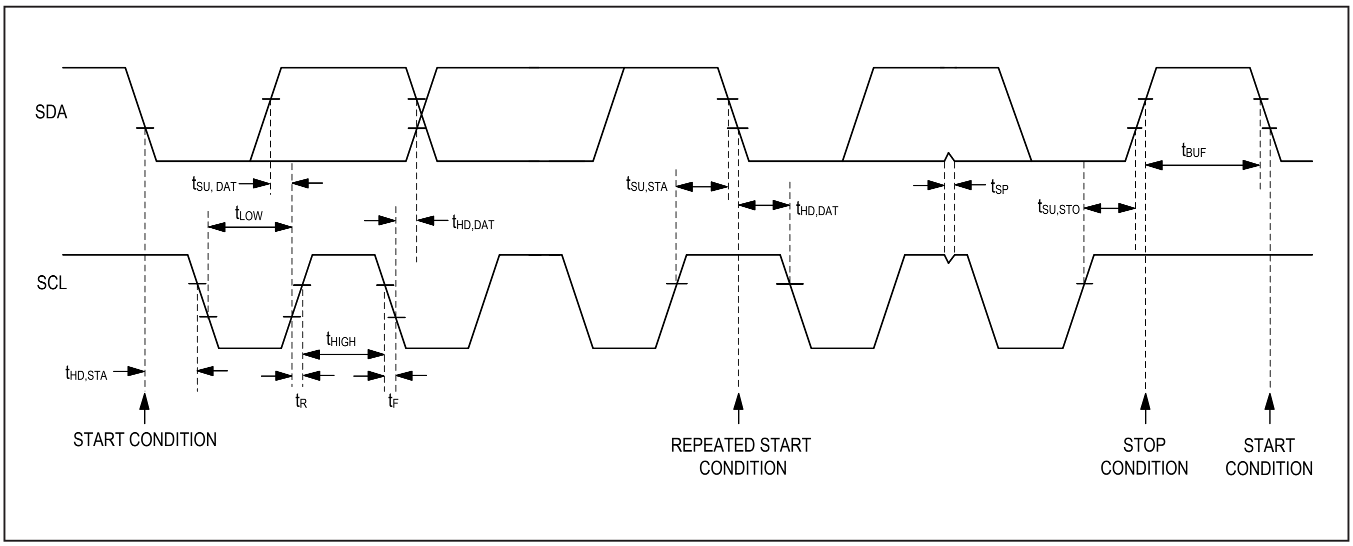


Figure 2. I²C Timing Diagram

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 3). A START (S) condition from the master signals the beginning of a transmission to the device. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

The device recognizes a STOP condition at any point during data transmission, unless the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock-signal generation for the I2C bus is the responsibility of the master device. The I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX20012B does not use any form of clock stretching to hold down the clock line.

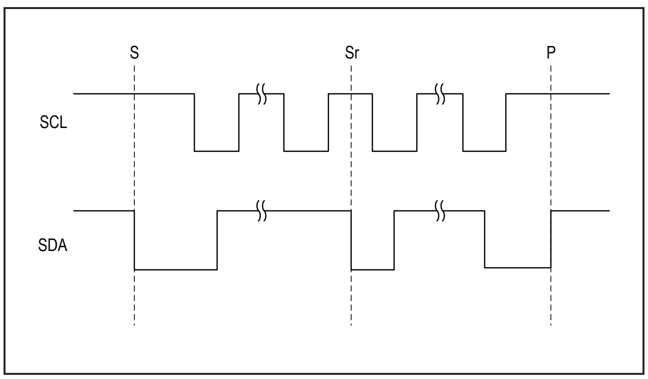


Figure 3. START, STOP, and Repeated START Conditions

I2C General Call Address

The MAX20012B does not implement the I2C specifications' "general call address." If the device sees the general call address (0b0000_0000), it does not issue an acknowledge.

Slave Address

Once the device is enabled, the I2C slave address is set by the ADDR pin (Table 1). Each output channel has a unique slave address. The address is defined as the 7 most significant bits (MSBs), followed by the R/W bit. Set the R/W bit to 1 to configure the IC to read mode. Set the R/W bit to 0 to configure the IC to write mode. The address is the first byte of information sent to the devices after the START condition.

Table 1. I2C Slave Addresses

ADDR PIN	A6	A5	A4	A3	A2*	A1*	A0	WRITE	READ
0	0	1	1	1	0	0	0	0x70	0x71
1	0	1	1	1	0	0	1	0x72	0x73
0	0	1	1	1	0	1	0	0x74	0x75
1	0	1	1	1	0	1	1	0x76	0x77
0	0	1	1	1	1	0	0	0x78	0x79
1	0	1	1	1	1	0	1	0x7A	0x7B

**See the Selector Guide for default settings.*

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 4). The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

Write Data Format

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to the register address, one byte of data to the command register, and a STOP condition. Figure 5 illustrates the proper format for one frame.

Read Data Format

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to the register address, a restart condition, the slave address with the read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 5 illustrates the proper format for one frame.

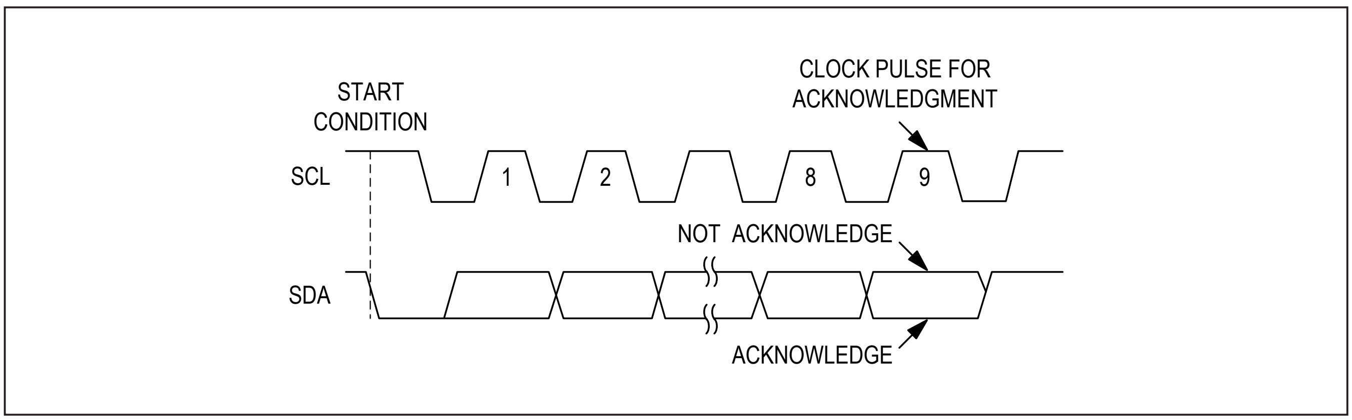


Figure 4. Acknowledge Condition

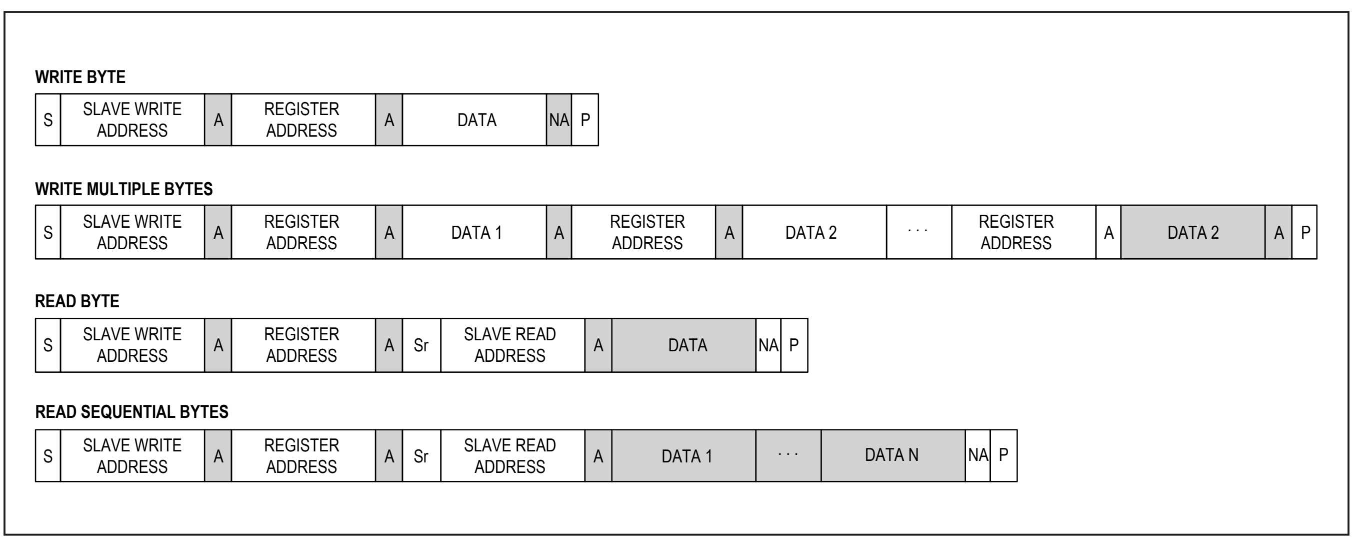


Figure 5. Data Format of I^2C Interface

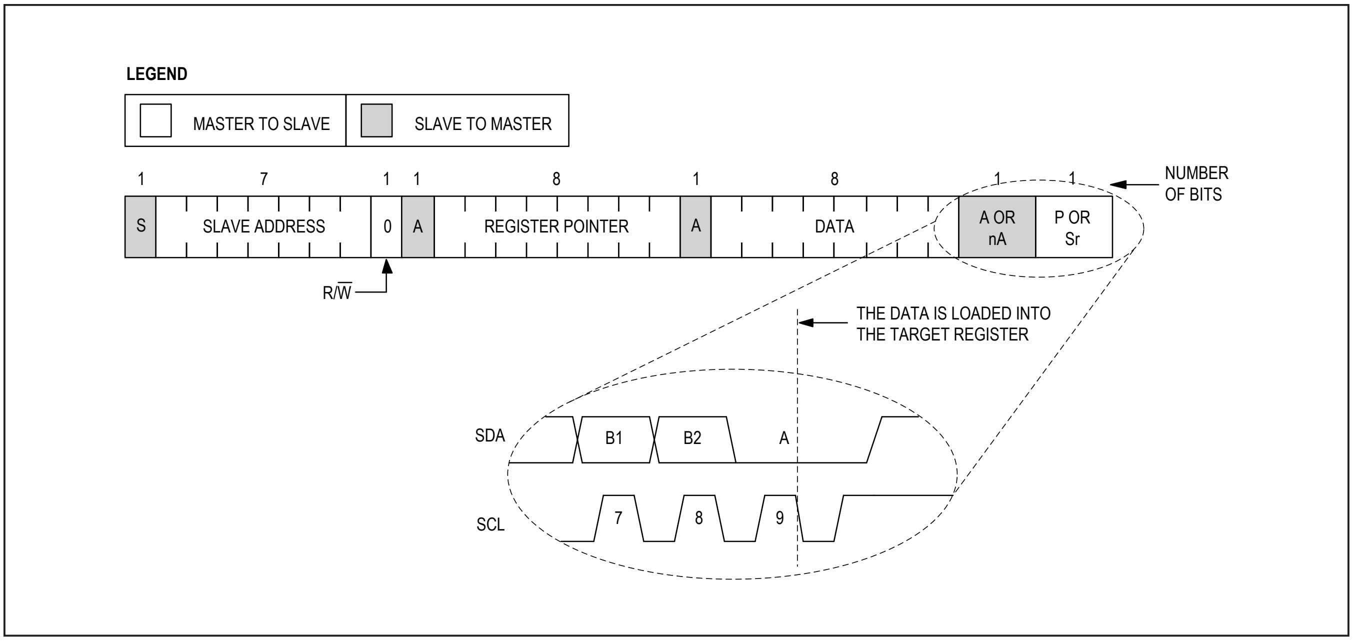


Figure 6. Write Byte Format

Writing to a Single Register

Figure 6 shows the protocol for the I^{2}C master device to write one byte of data to the MAX20012B. This protocol is the same as the SMBus specification's "write byte" protocol.

The "write byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9) The master sends a STOP condition (P) or a Repeated START condition (Sr).

Writing Multiple Bytes Using Register Data Pairs

Figure 7 shows the protocol for the I^{2}C master device to write multiple bytes to the MAX20012B using register-data pairs. This protocol allows the I^{2}C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a STOP condition.

The "writing multiple bytes using register-data pairs" protocol is not supported by the RTC functional block.

The "multiple byte register-data pair" protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8) Steps 5–7 are repeated as many times as the master requires.
9) The master sends a STOP condition. During the rising edge of the stop-related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

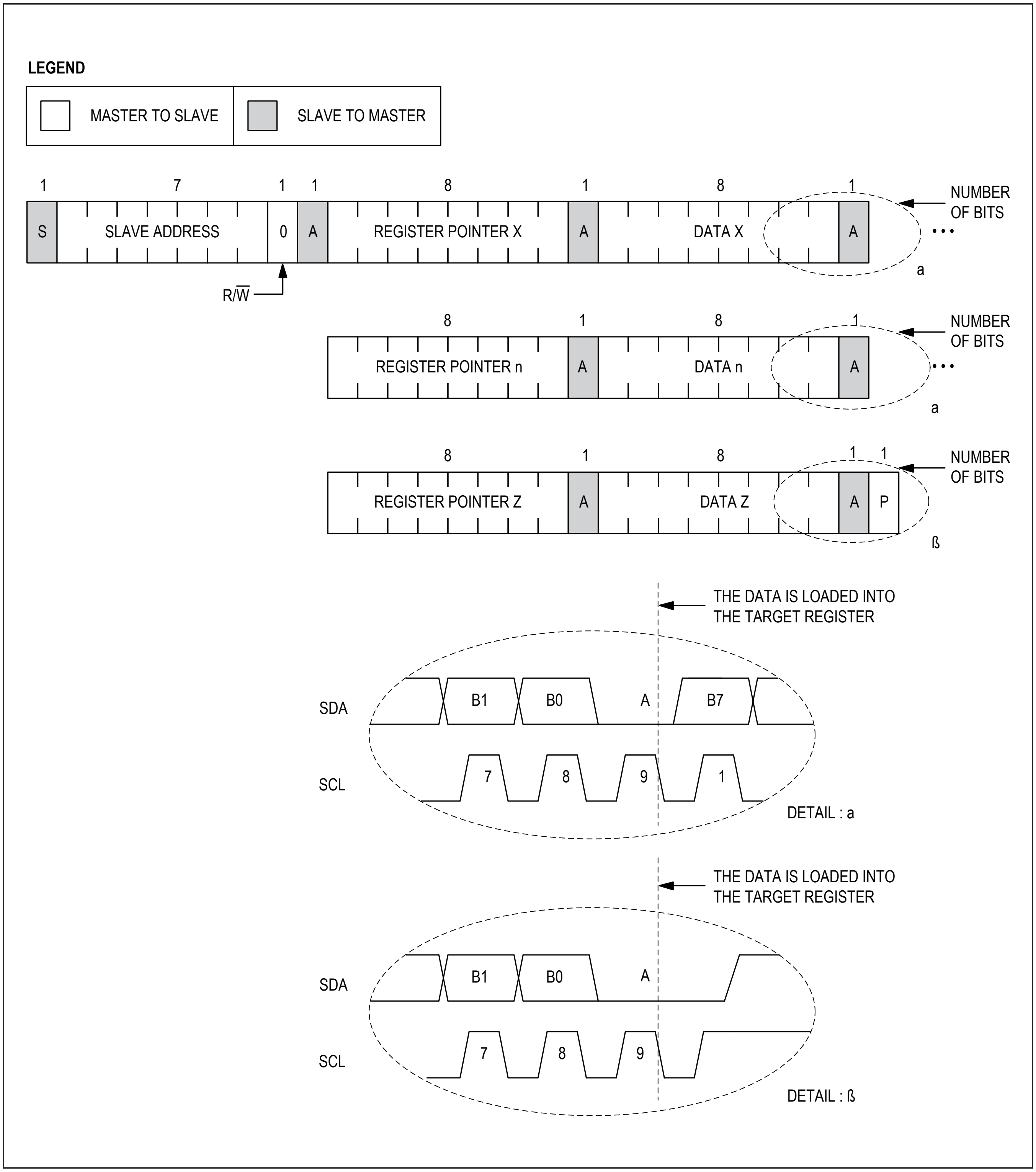


Figure 7. Write Register-Data Pair Format

Both outputs have an identical register set, as defined below. They are accessed individually by using each channel's unique I2C address. Each channel has the same register set accessed through their individual I2C address (see Table 1).

Table 2. Register Map

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	CMD	R/W	POWER-ON RESET
ID	DEV3	DEV2	DEV1	DEV0	R3	R2	R1	R0	0x00	R	0x23, 0x33
—	—	—	—	—	—	—	—	—	0x01	R/W	0x00
VIDMAX	—	VMAX6	VMAX5	VMAX4	VMAX3	VMAX2	VMAX1	VMAX0	0x02	R/W	OTP
TCONFIG	ENTRK	—	—	—	—	—	TA1	TA0	0x03	R/W	0x02
STATUS	INTERR	TRKERR	VRHOT	UV	OV	OC	VMERR	0	0x04	R	0x00
CONFIG	VSTEP	—	—	—	FPWM	SS	SO1	SO0	0x05	R/W	OTP
SLEW	—	—	—	—	SR3	SR2	SR1	SR0	0x06	R/W	OTP
VID	—	VID6	VID5	VID4	VID3	VID2	VID1	VID0	0x07	R/W	OTP
TRACKVID	—	—	TVID5	TVID4	TVID3	TVID2	TVID1	TVID0	0x2B	R/W	0x00

Table 3. Identification Register (ID)

	7	6	5	4	3	2	1	0
	DEV3	DEV2	DEV1	DEV0	R3	R2	R1	R0
	0	0	1	0	0	1	0	0
	0	0	1	1	0	1	0	0

BIT	BIT DESCRIPTION
DEV[3:0]	Device ID: MAX20012B OUT1 = 0x2 MAX20012B OUT2 = 0x3
R[3:0]	MAX20012B = 0x4

VIDMAX								
BIT NO.	7	6	5	4	3	2	1	0
NAME	—	VMAX6	VMAX5	VMAX4	VMAX3	VMAX2	VMAX1	VMAX0
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
VMAX[6:0]	Maximum Voltage Setting. If VID[] > VMAX[], then a fault is set and the actual voltage is capped by VMAX[]. See Table 10 for VID output-voltage selections.

Table 5. Tracking Mode Register (TCONFIG)

TCONFIG								
BIT NO.	7	6	5	4	3	2	1	0
NAME	ENTRK	—	—	—	—	—	TA1	TA0
POR	0	0	0	0	0	0	1	0

BIT	BIT DESCRIPTION
ENTRK	Enable Tracking Mode. When '1' and VSTEP = '1' then tracking mode is enabled: 0 = Disabled 1 = Enabled
TA[1:0]	The I²C address of the MAX20024 used for LDO4 voltage tracking: 00 = 0x38 01 = 0x3C 10 = 0x78 11 = 0x7C

Table 6. Configuration Register (CONFIG)

CONFIG								
BIT NO.	7	6	5	4	3	2	1	0
NAME	VSTEP	—	—	—	FPWM	SS	SO1	SO0
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
VSTEP	Voltage Step Size. Sets the voltage step size for the LSB of VID: 0 = 10mV 1 = 12.5mV
FPWM	Forced-PWM Mode: 0 = Mode controlled by SYNC pin. When SYNC is output, device is always in FPWM mode. 1 = Forced-PWM Mode. Overrides SYNC skip mode setting when SYNC is an input.
SS	Spread-Spectrum Clock Setting: 0 = Disabled 1 = +3% spread
SO[1:0]	SYNC I/O Select: 00 = Master: Input, rising edge starts cycle 01 = Master: Input, falling edge starts cycle 10 = Master: Output, falling edge starts cycle 11 = Unused

Table 7. Status Register (STATUS)

STATUS								
BIT NO.	7	6	5	4	3	2	1	0
NAME	INTERR	TRKERR	VRHOT	UV	OV	OC	VMERR	0
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
INTERR	Internal Hardware Error: This bit is set to ‘1’ when ATE trimming and testing not complete.
TRKERR	Tracking Address Error: This bit is set to ‘1’ when **ENTRK** == 1 & VSTEP == 0.
VRHOT	Thermal Shutdown Indication: A thermal shutdown has occurred since the last time this register was read.
UV	VOUT Undervoltage: This bit indicates if the output is currently under the target voltage.
OV	VOUT Overvoltage: This bit indicates if the output is currently over the target voltage.
OC	VOUT Overcurrent: This bit indicates if an overcurrent event has occurred since the last time the STATUS register was read.
VMERR	VOUTMAX Error. Set to 1 if **VID[]** > **VOUTMAX[]** in normal mode, or **TVID[]** > **VOUTMAX[]** in tracking mode.

Table 8. Slew-Rate Register (SLEW)

SR[3:0]	SOFT-START SLEW RATE (MV/MS) (NOTE 1)	RISING DVS SLEW RATE (MV/MS) (NOTE 1 AND 2)
XXXX0000	22	22
XXXX0001	11	22
XXXX0010	5.5	22
XXXX0011	11	11
XXXX0100	5.5	11
XXXX0101	22	22
XXXX0110	22	22
XXXX0111	11	22
XXXX1000	5.5	22
XXXX1001	5.5	5.5
XXXX1010 – XXXX1111	Reserved	Reserved

Note 1: *VSTEP = ‘0’; when VSTEP = ‘1’, increase by a factor of 1.25.*
Note 2: *Falling DVS slew rate is -1.375mV/µs.*

Table 9. Output-Voltage Register (VID)

	7	6	5	4	3	2	1	0
	—	VID6	VID5	VID4	VID3	VID2	VID1	VID0
	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
VID[6:0]	Target Voltage Setting. V_{OUT} ramps at the programmed DVS ramp rate until it reaches programmed VID. See Table 10 for VID output-voltage selections.

Table 10. VID Output-Voltage Selection

VID[6:0]	V_{OUT} (V) (VSTEP = 0)	V_{OUT} (V) VSTEP = 1	VID[6:0]	V_{OUT} (V) (VSTEP = 0)	V_{OUT} (V) VSTEP = 1	VID[6:0]	V_{OUT} (V) (VSTEP = 0)	V_{OUT} (V) VSTEP = 1
0x00	OFF	OFF	0x20	0.810	1.0125	0x40	1.130	1.4125
0x01	0.500	0.6250	0x21	0.820	1.0250	0x41	1.140	1.4250
0x02	0.510	0.6375	0x22	0.830	1.0375	0x42	1.150	1.4375
0x03	0.520	0.6500	0x23	0.840	1.0500	0x43	1.160	1.4500
0x04	0.530	0.6625	0x24	0.850	1.0625	0x44	1.170	1.4625
0x05	0.540	0.6750	0x25	0.860	1.0750	0x45	1.180	1.4750
0x06	0.550	0.6875	0x26	0.870	1.0875	0x46	1.190	1.4875
0x07	0.560	0.7000	0x27	0.880	1.1000	0x47	1.200	1.5000
0x08	0.570	0.7125	0x28	0.890	1.1125	0x48	1.210	1.5125
0x09	0.580	0.7250	0x29	0.900	1.1250	0x49	1.220	1.5250
0x0A	0.590	0.7375	0x2A	0.910	1.1375	0x4A	1.230	1.5375
0x0B	0.600	0.7500	0x2B	0.920	1.1500	0x4B	1.240	1.5500
0x0C	0.610	0.7625	0x2C	0.930	1.1625	0x4C	1.250	1.5625
0x0D	0.620	0.7750	0x2D	0.940	1.1750	0x4D	1.260	1.5750
0x0E	0.630	0.7875	0x2E	0.950	1.1875	0x4E	1.270	1.5875
0x0F	0.640	0.8000	0x2F	0.960	1.2000	—	—	—
0x10	0.650	0.8125	0x30	0.970	1.2125	—	—	—
0x11	0.660	0.8250	0x31	0.980	1.2250	—	—	—
0x12	0.670	0.8375	0x32	0.990	1.2375	—	—	—
0x13	0.680	0.8500	0x33	1.000	1.2500	—	—	—
0x14	0.690	0.8625	0x34	1.010	1.2625	—	—	—
0x15	0.700	0.8750	0x35	1.020	1.2750	—	—	—
0x16	0.710	0.8875	0x36	1.030	1.2875	—	—	—
0x17	0.720	0.9000	0x37	1.040	1.3000	—	—	—
0x18	0.730	0.9125	0x38	1.050	1.3125	—	—	—
0x19	0.740	0.9250	0x39	1.060	1.3250	—	—	—
0x1A	0.750	0.9375	0x3A	1.070	1.3375	—	—	—
0x1B	0.760	0.9500	0x3B	1.080	1.3500	—	—	—
0x1C	0.770	0.9625	0x3C	1.090	1.3625	—	—	—
0x1D	0.780	0.9750	0x3D	1.100	1.3750	—	—	—
0x1E	0.790	0.9875	0x3E	1.110	1.3875	—	—	—
0x1F	0.800	1.0000	0x3F	1.120	1.4000	—	—	—

Table 11. Tracking Voltage Register (TRACKVID)

	TVID							
BIT NO.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	0	0	TVID5	TVID4	TVID3	TVID2	TVID1	TVID0
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
TVID[5:0]	Tracking VID: This is used to calculate the new VID when in tracking mode. See Table 12 for TRACKVID output-voltage selections.

Table 12. TRACKVID Output-Voltage Selections

TVID[5:0]	VOUT	TVID[5:0]	VOUT	TVID[5:0]	VOUT	TVID[5:0]	VOUT
0x00	0.8000	0x10	1.0000	0x20	1.2000	0x30	1.4000
0x01	0.8125	0x11	1.0125	0x21	1.2125	0x31	1.4125
0x02	0.8250	0x12	1.0250	0x22	1.2250	0x32	1.4250
0x03	0.8375	0x13	1.0375	0x23	1.2375	0x33	1.4375
0x04	0.8500	0x14	1.0500	0x24	1.2500	0x34	1.4500
0x05	0.8625	0x15	1.0625	0x25	1.2625	0x35	1.4625
0x06	0.8750	0x16	1.0750	0x26	1.2750	0x36	1.4750
0x07	0.8875	0x17	1.0875	0x27	1.2875	0x37	1.4875
0x08	0.9000	0x18	1.1000	0x28	1.3000	0x38	1.5000
0x09	0.9125	0x19	1.1125	0x29	1.3125	0x39	1.5125
0x0A	0.9250	0x1A	1.1250	0x2A	1.3250	0x3A	1.5250
0x0B	0.9375	0x1B	1.1375	0x2B	1.3375	0x3B	1.5375
0x0C	0.9500	0x1C	1.1500	0x2C	1.3500	0x3C	1.5500
0x0D	0.9625	0x1D	1.1625	0x2D	1.3625	0x3D	1.5625
0x0E	0.9750	0x1E	1.1750	0x2E	1.3750	0x3E	1.5750
0x0F	0.9875	0x1F	1.1875	0x2F	1.3875	0x3F	1.5875

Voltage-Tracking Mode

The MAX20012B features a special voltage-tracking mode where the device listens to I2C write commands targeted at LDO4 of the MAX20024 PMIC. Any time the CNFG1_L4.TV_L4[5:0] (register 0x2B) is updated, the value is copied to the TRACKVID register. When tracking is enabled (TCONFIG.ENTRK = 1 and CONFIG.VSTEP = 1), the TRACKVID value is used instead of the VID register to set the output voltage. The I2C address of the MAX20024 PMIC must be selected in the TCONFIG register for tracking to work properly.

PG Output

The IC features an open-drain PGOOD output that asserts when the output voltage is between the PG_UV and PG_OV thresholds. PG_ is asserted after the power-good active timeout period. An additional 220μs (typ) PG_ delay exists following soft-start or DVS slewing. PG_ is deasserted after a UV/OV propagation delay if the output voltage is outside the PG_ UV/OV thresholds, or after the first DVS command after soft-start. Connect PG_ to a pullup supply with a 20kΩ resistor.

Soft-Start

The IC includes a programmable soft-start rate. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Dynamic Voltage Scaling

The step-down regulators feature dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. DVS registers for OUT1 and OUT2 are programmed with VID[6:0]. The rising slew rate during DVS is adjustable with SR[3:0] (see Table 8). The falling slew rate during DVS is fixed at -1.375mV/μs for VSTEP = 0 and -1.719mV/μs for VSTEP = 1. The PG_ comparator is masked to prevent false PG_ interrupts during the DVS period. I2C DVS commands should only be issued when the output voltage is no longer slewing and is in a stable state.

Shutdown

During shutdown, the output voltage is ramped down at the 1.375mV/μs slew rate. The CS- pulldown is enabled as needed to assist in the ramp down. When powering down in skip mode under light load, the falling ramp may be based on the RC discharge curve based on C_{OUT} and the 5Ω pulldown resistance.

Spread-Spectrum Option

The IC features spread-spectrum (SS) operation by varying the internal operating frequency up by 3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to external sync.

Synchronization (SYNC)

SYNC is an I2C-programmable I/O. When configured as an input and the FPWM bit = 0, driving SYNC low or unconnected places the converter in skip mode. Forcing SYNC logic-high places the IC in forced-PWM (FPWM) mode. Input triggering on the rising edge or falling edge is determined by the setting of registers SO[1:0], see Table 6. When SO[1:0] = 2, SYNC is configured as an output. The output clock is 180° out of phase with the internal clock.

Current-Limit/Short-Circuit Protection

The current-limit circuit uses differential current-sense inputs (CS_+ and CS_-) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold (VLIM_ = 57.4mV (typ), 60mV (typ), 62.8mV (max)), the PWM controller turns off the high-side MOSFET.

The high side turns on again once the inductor current drops below the valley current limit. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{IN}). See Figure 8 for current-sense configurations.

If the inductor current exceeds the maximum current limit programmed at CS_+ and CS_-, the respective driver turns off. In an overcurrent mode, this results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. During a hard short, the IC turns off and repeats soft-start every 4ms (at 2.2MHz switching frequency) until the short is removed. For an example, see the short-circuit (PWM mode) waveform (TOC20) in the *Typical Operating Characteristics* section.

PWM/Skip Modes

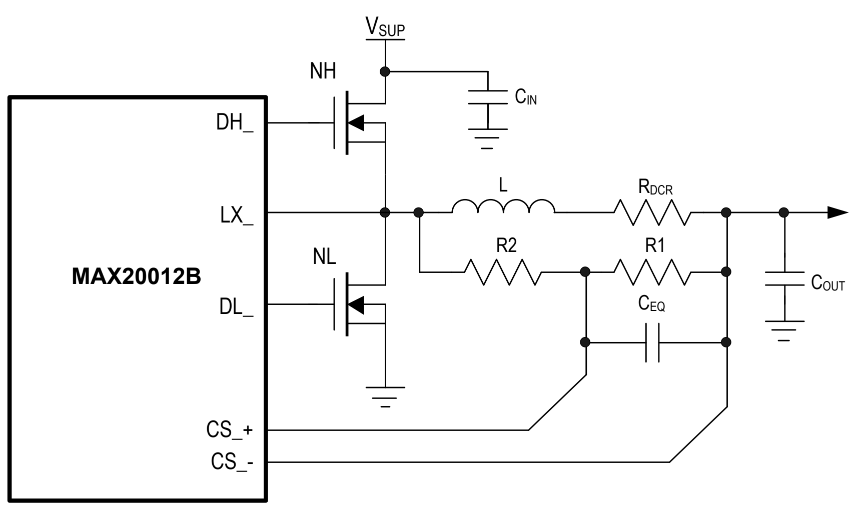
The IC features an input (SYNC) that puts both converters in either skip mode or forced-PWM mode of operation. See the *Pin Description* table for mode detail. In PWM mode of operation, the converter switches at a constant frequency with variable on-time. In skip mode of operation, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often is the case in the PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode. VID updates while the IC is in skip mode are delayed until the next LX_ switching pulse, which is load dependent. If immediate VID update response is required, switch the IC to PWM mode when updating the VID.

Dual-Phase Operation

With the addition of a MAX15492 gate driver IC connected to PWM1X and CS1X+, OUT1 of the MAX20012B can support two phases to increase the output current by a factor of two. The same inductor, FETs, and current-limit network must be used on both phases to ensure proper current balancing. An additional 100μF of ceramic output capacitance is required (for a total of 300μF).

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the IC. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.



$$R_{CSEQ} = \left(\frac{R_1}{R_1 + R_2}\right) R_{DCR}$$

$$R_{DCR} = \frac{L}{C_{EQ}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

Figure 8. Current-Sense Configurations

Lossless Inductor DCR Sensing

High-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor with an equivalent time constant:

$$R_{CSEQ} = \left(\frac{R1}{R_1 + R_2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

where R_{CSEQ} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistance. Use the inductance and R_{DCR} values provided by the inductor manufacturer.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CS_+ and CS_-. Place the sense network close to the device with short, direct traces, making a Kelvin-sense connection to the current-sense network.

High-Side Gate-Drive Supply (BST1)

The high-side MOSFET is turned on by closing an internal switch between BST1 and DH1 and transferring the bootstrap capacitor's (at BST1) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX1 voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time the bootstrap diode recharges the positive terminal of the bootstrap capacitor. The selected n-channel high-side MOSFET determines the appropriate boost-capacitance values ($C_{BST\_}$ in the *Typical Operating Circuit*) according to the following equation:

$$C_{BST\_} = \frac{Q_G}{\Delta V_{BST1}}$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST1} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST1} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST1} = 100mV to 300mV) when determining $C_{BST\_}$.

The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases.

C_{BST2} is calculated using the same method described for C_{BST1}.

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)}\frac{\sqrt{V_{OUT}(V_{PV\_} - V_{OUT})}}{V_{PV\_}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{PV\_} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input-voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{PV\_} - V_{OUT}) \times V_{OUT}}{V_{PV\_} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

and:

$$D = \frac{V_{OUT}}{V_{PV\_}}$$

I_{OUT} is the maximum output current, D is the duty cycle.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20012B: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use the following formula to determine the minimum inductor value:

$$L_{MIN} = 1.3 \times \left[\frac{(V_{PVMAX} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{PVMAX}} \right)}{f_{SW} \times I_{OUTMAX} \times K_{INDMAX}} \right]$$

where f_{SW1} is the operating frequency and 1.3 is a coefficient that accounts for inductance initial precision. K_{INDMAX} is the maximum inductor current ripple. A good initial maximum inductor current ripple is 30% peak to peak (K_{INDMAX} = 0.3).

For proper operation, the chosen inductor value must be ≥ L_{MIN}. The maximum inductor value recommended is twice the chosen value from the above formula.

MOSFET Selection

The gate drivers drive two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs are:

- Drain-to-Source On-Resistance ($R_{DS(ON)}$)
- Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)
- Minimum Threshold Voltage ($V_{TH(MIN)}$)
- Total Gate Charge (Q_G)
- Reverse Transfer Capacitance (C_{RSS})
- Power Dissipation

Both n-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 3.5V. The conduction losses at minimum input voltage should not exceed MOSFET package thermal limits or violate the overall thermal budget. Also ensure that the conduction losses plus switching losses at the maximum input voltage do not exceed package ratings or violate the overall thermal budget. In particular, check that the dV/dt caused by DH_ turning on does not pull up the DL_ gate through its drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Therefore, the power dissipation in the IC due to drive losses must be checked. Both MOSFETs must be selected so that their total gate charge is low enough; therefore, P_V/V_{OUT} can power both drivers without overheating the IC:

$$P_{DRIVE} = V_{OUT} \times (Q_{GTOTH} + Q_{GTOTL}) \times f_{SW1}$$

Where Q_{GTOTL} is the low-side MOSFET total gate charge and Q_{GTOTH} is the high-side MOSFET total gate charge. Select MOSFETs with a Q_{G_TOTAL} of less than 15nC.

The n-channel MOSFETs must deliver the average current to the load and the peak current during switching. Dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the DH_ path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Output Capacitor

Use low-ESR ceramic capacitors on the output. Other capacitor types should be verified with a gain and phase analysis. In single-phase configuration, use a nominal value of 200µF; in dual-phase configuration, use a nominal value of 300µF.

Selector Guide

OPTION SUFFIX	V_{OUT1} (V)					V_{OUT2} (V)				
	VMAX	CONFIG	VID	SLEW	I2C	VMAX	CONFIG	VID	SLEW	I2C
A/V+	0x3B (1.08)	0x0C	0x36 (1.03)	0x04	0x74	0x43 (1.45)	0x8C	0x3B (1.35)	0x04	0x70
A/VY+	0x3B (1.08)	0x0C	0x36 (1.03)	0x04	0x74	0x43 (1.45)	0x8C	0x3B (1.35)	0x04	0x70
B/V+	0x4E (1.27)	0x08	0x47 (1.20)	0x03	0x74	0x3D (1.10)	0x08	0x33 (1.00)	0x03	0x70
C/V+	0x4A (1.23)	0x08	0x31 (0.98)	0x03	0x74	0x4A (1.23)	0x08	0x2E (0.95)	0x03	0x70
D/V+	0x42 (1.15)	0x08	0x29 (0.90)	0x00	0x70	0x42 (1.15)	0.08	0x29 (0.90)	0x00	0x74
E/V+	0x2E (0.95)	0x0C	0x22 (0.83)	0x09	0x70	0x47 (1.20)	0x0C	0x3E (1.11)	0x09	0x74
F/V+	0x4A (1.23)	0x08	0x21 (0.82)	0x03	0x74	0x4A (1.23)	0x08	0x21 (0.82)	0x03	0x70
F/VY+	0x4A (1.23)	0x08	0x21 (0.82)	0x03	0x74	0x4A (1.23)	0x08	0x21 (0.82)	0x03	0x70
G/V+	0x36 (1.03)	0x0C	0x33 (1.00)	0x03	0x70	0x36 (1.03)	0x0C	0x33 (1.00)	0x03	0x74
H/V+	0x2A (0.91)	0x05	0x22 (0.83)	0x09	0x74	0x38 (1.05)	0x05	0x2F (0.96)	0x09	0x70
H/VY+	0x2A (0.91)	0x05	0x22 (0.83)	0x09	0x74	0x38 (1.05)	0x05	0x2F (0.96)	0x09	0x70
J/V+	0x33 (1.25)	0x84	0x0F (0.80)	0x00	0x74	0x27 (1.10)	0x84	0x17 (0.90)	0x00	0x70
K/V+	0x2D (0.94)	0x08	0x24 (0.85)	0x09	0x74	0x48 (1.21)	0x08	0x3D (1.10)	0x09	0x70
L/V+	0x2D (0.94)	0x0C	0x24 (0.85)	0x09	0x74	0x48 (1.21)	0x0C	0x3D (1.10)	0x09	0x70

For variants with different options, contact factory.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20012BATJ_/V+	-40°C to +125°C	32 TQFN-EP*
MAX20012BATJ_/VY+	-40°C to +125°C	32 SW TQFN-EP*

Note: *Insert the desired suffix option from the Selector Guide into the blank.*
/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
SW = Side-wettable TQFN package
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—
1	1/18	Updated *PG Output* section	22
2	3/18	Updated *Selector Guide*	26
3	4/18	Updated *Selector Guide*	26
4	5/18	Updated *Selector Guide*	26
5	12/18	Updated *Selector Guide*	26
6	3/19	Changes to *Table 6* on the *Bit Description*,and *Spread Spectrum Option* section, updated *Selector Guide* and *Ordering Information section*	18, 22, 26
7	5/19	Updated *Package Information* and *Selector Guide*	3, 26
8	8/19	Updated *Selector Guide*	26