IS32FL3265A

HIGH-VOLTAGE, 18-CHANNEL LED DRIVER

March 2020

GENERAL DESCRIPTION

The IS32FL3265A is an LED driver with 18 high voltage (40V) constant current channels. Each channel can be pulse width modulated (PWM) by 8 bits for smooth LED brightness control. In addition, each channel has an 8-bit output current control register which allows fine tuning of the channel current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel is designed to be 60mA, which can be adjusted by one 32 steps global control register. Proprietary algorithms are used in the IS32FL3265A to minimize audible noise caused by the MLCC decoupling capacitors. All registers can be programmed via 1MHz I2C compatible interface.

The IS32FL3265A can be configured to a minimum current consumption mode by either pulling the SDB pin low or by using the software shutdown feature.

The IS32FL3265A is available in eTSSOP-28 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

APPLICATIONS

- Car display panel
- Ambient lighting
- Roof lighting
- Functional lighting

FEATURES

- 3V to 5.5V operating supply
- Output current capability and number of outputs: 60mA × 18 outputs, tolerance voltage 40V
- 1MHz I2C with automatic address increment
- Programmable H/L logic: 1.4V/0.4V, 2.4V/0.6V
- Accurate color rendition
  - 32 steps global current adjust
  - 8-bit dot correction for each channel
  - 8-bit PWM for each channel
- Selectable PWM method (200Hz or 25kHz)
- 256-Step group blink with frequency programmable from 24Hz to 10.66s and duty cycle from 0% to 99.6%
- Clock IO pin for multi-chip synchronization
- Fault report (open detect/thermal roll off /thermal shutdown)
- Thermal roll-off programmable set point
- SDB rising edge resets I2C interface
- EMI reduction technology
  - Spread spectrum
  - Selectable 9 phase delay
- Operating temperature range, -40°C ~ +125°C
- Package: eTSSOP-28
- AEC-Q100 Qualified
- Current accuracy (All output on)
  - Bit to bit: < ±6%
  - Device to device: < ±6%

TYPICAL APPLICATION CIRCUIT

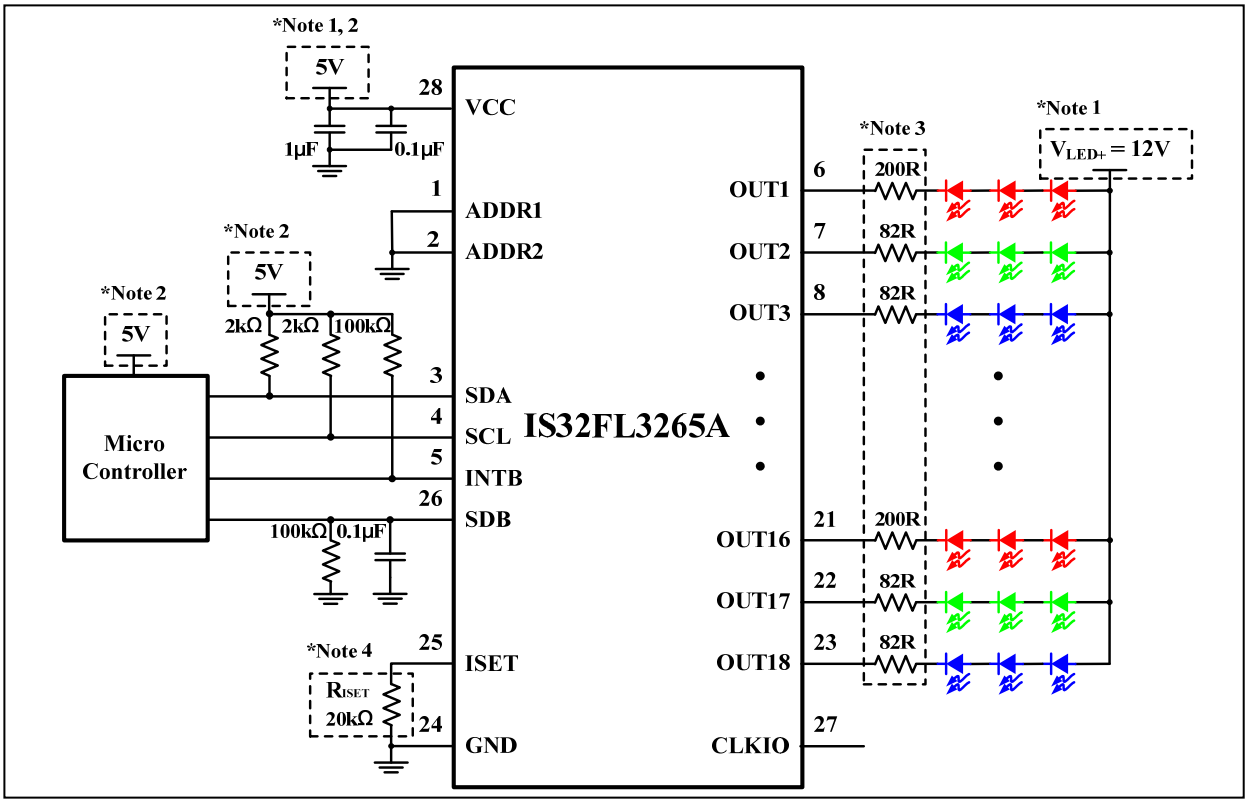


Figure 1 Typical Application Circuit

Note 1: VCC pin should not be higher than 5.5V, VLED+ can be higher than VCC.

Note 2: V_{IH} is the high level voltage for IS32FL3265A's SDA, SCL and INTB, which is usually same as VCC pin and VCC of Micro Controller, e.g. if VCC of Micro Controller is 3.3V, VCC(IS32FL3265A)=V_{IH}=3.3V，if VCC of Micro Controller is 5V, VCC(IS32FL3265A)=V_{IH}=5V, but VCC(IS32FL3265A) should not be lower than 3V.

Note 3: These resistors are for offloading the thermal dissipation (I^2R) away from the IS32FL3265A.

Note 4: The maximum global output current is set by external resistor, R_{ISET}. Please refer to the application information in R_{ISET} section.

Note 5: The IC and LED string should be placed far away from any local antenna in order to prevent EMI contamination.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

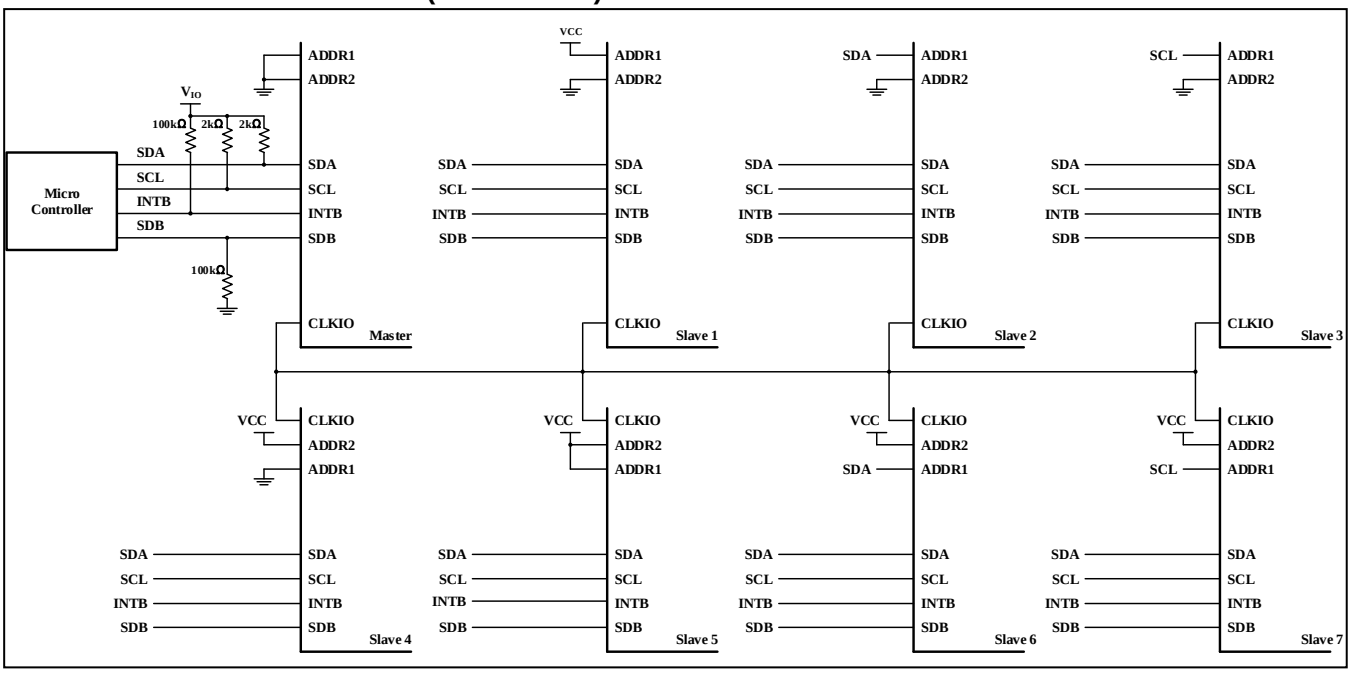
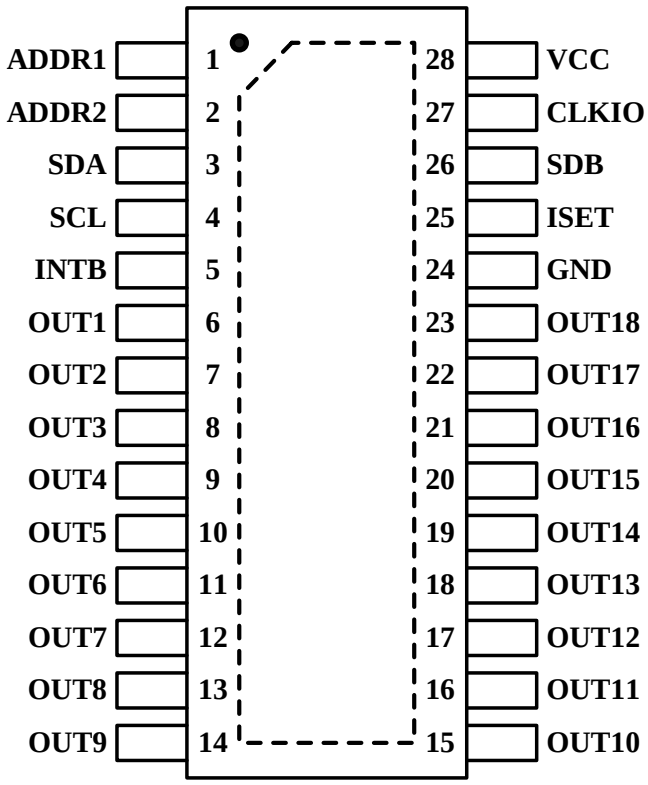


Figure 2 Typical Application Circuit (Eight Device Synchronization)

Note 6: One system should contain only one master, all slave parts should be configured as slave mode before the master is configured as master mode. Master or slave mode is specified by the Configuration Register. The master will output a master clock (CLKIO), and all the other devices configured as slaves will synchronize their CLKIO inputs to the master clock.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-28	

PIN DESCRIPTION

No.	Pin	Description
1	ADDR1	I2C address setting pin.
2	ADDR2	I2C address setting pin.
3	SDA	I2C serial data.
4	SCL	I2C serial clock.
5	INTB	Interrupt output pin. Register 14h can set the function of the INTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function is not used.
6~23	OUT1~OUT18	Output LED current sink channels 1~18.
24	GND	GND pin for control logic.
25	ISET	Input terminal used to connect an external resistor. This regulates the global output current.
26	SDB	Shutdown the chip when pulled low.
27	CLKIO	Cascade connection pin.
28	VCC	Power supply.
	Thermal Pad	Need to connect to GND.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY
IS32FL3265A-ZLA3-TR	eTSSOP-28, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, INTB, CLKIO, ADDR1, ADDR2	-0.3V ~ V_{CC}+0.3V
Voltage at OUT1 to OUT36	40V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	33.8°C/W
Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JESD 51-2A), θ_{JP}	11.08°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 7: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC}= 5V, T_A= T_J = -40°C ~ +125°C, Typical values are at T_J = 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		3		5.5	V
I_{OUT}	Maximum output current	R_{ISET}= 6.8kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF, V_{OUT}= 0.8V (Note 8)		60		mA
	Output current	R_{ISET}= 20kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF	19	20.4	21.8	mA
ΔI_{MAT}	I_{OUT} mismatch (bit to bit)	R_{ISET}= 20kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF (Note 9)		±2	±6	%
ΔI_{OUT}	I_{OUT} accuracy (device to device)	R_{ISET}= 20kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF (Note 10)		±2	±6	%
V_{HR}	Headroom voltage	R_{ISET}= 20kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF		0.3	0.5	V
I_{CC}	Quiescent power supply current	R_{ISET}= 20kΩ, GCC= 0xFF, Scaling= 0xFF, PWM= 0		7.5	9	mA
		VCC= 3.6V, R_{ISET}= 20kΩ, GCC= 0xFF, Scaling= 0xFF, PWM= 0		7.2	8.5	mA
I_{SD}	Shutdown current	R_{ISET}= 20kΩ, V_{SDB}= 0V or software shutdown		4	20	μA
		VCC= 3.6V, R_{ISET}= 20kΩ, V_{SDB}= 0V or software shutdown		1	12	μA
V_{ISET}	ISET voltage	R_{ISET}= 20kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF	0.98	1.0	1.02	V
V_{OD}	OUTx pin open detect threshold	R_{ISET}=20kΩ, GCC= 0x20, Scaling= 0xFF, PWM=0xFF, measured at OUTx	100	150		mV
I_{OZ}	Output leakage current	V_{SDB}= 0V or software shutdown, V_{OUT}= 40V			1	μA
f_{OUT}	PWM frequency of output	Frequency setting=25kHz	22	25	28	kHz
T_{SD}	Thermal shutdown			165		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{CC}= 5V, T_A= T_J = -40°C ~ +125°C, Typical values are at T_J = 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, ADDR1, ADDR2, SDB, CLKIO)						
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V, LGC=0			0.4	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V, LGC=0	1.4			V
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V, LGC=1			0.6	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V, LGC=1	2.4			V
V_{OH}	H level of CLKIO pin output voltage	I_{OH}= -8mA	V_{CC}-0.4V		V_{CC}	V
V_{OL}	L level of CLKIO pin output voltage	I_{OL}= 8mA	0		0.4	V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 11)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{CC} (Note 11)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 11)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 8: The recommended minimum value of R_{ISET} is 6.8kΩ.

Note 9: I_{OUT} mismatch (bit to bit) is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n=1\sim 18)}{\left(\frac{I_{OUT1}+I_{OUT2}+...+I_{OUT18}}{18} \right)} - 1 \right) \times 100\%$$

Note 10: I_{OUT} accuracy (device to device) is calculated:

$$\Delta I_{OUT} = \left(\frac{\left(\frac{I_{OUT1}+I_{OUT2}+...+I_{OUT18}}{18} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 20.4mA (R_{ISET}= 20kΩ, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF).

Note 11: Guaranteed by design.

DETAILED DESCRIPTION

I2C INTERFACE

The IS32FL3265A uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS32FL3265A has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDR1/2 pins. The complete slave address is:

Table 1 Slave Address:

ADDR2	ADDR1	A7:A5	A4:A3	A2:A1	A0
GND	GND	100	00	00	0/1
GND	SCL		00	01	
GND	SDA		00	10	
GND	VCC		00	11	
SCL	GND		01	00	
SCL	SCL		01	01	
SCL	SDA		01	10	
SCL	VCC		01	11	
SDA	GND		10	00	
SDA	SCL		10	01	
SDA	SDA		10	10	
SDA	VCC		10	11	
VCC	GND		11	00	
VCC	SCL		11	01	
VCC	SDA		11	10	
VCC	VCC		11	11	

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;
ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;
ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;
ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz (Fast-mode plus). In this discussion, the master is the microcontroller and the slave is the IS32FL3265A.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS32FL3265A's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS32FL3265A has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32FL3265A, the register address byte is sent, most significant bit first. IS32FL3265A must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS32FL3265A must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS32FL3265A, load the address of the data register that the first data byte is intended for. During the IS32FL3265A acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS32FL3265A will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS32FL3265A (Figure 6).

READING OPERATION

All of the registers can be read (Table 2).

To read the register, after I2C start condition, the bus master must send the IS32FL3265A device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS32FL3265A device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS32FL3265A to the master (Figure 7).

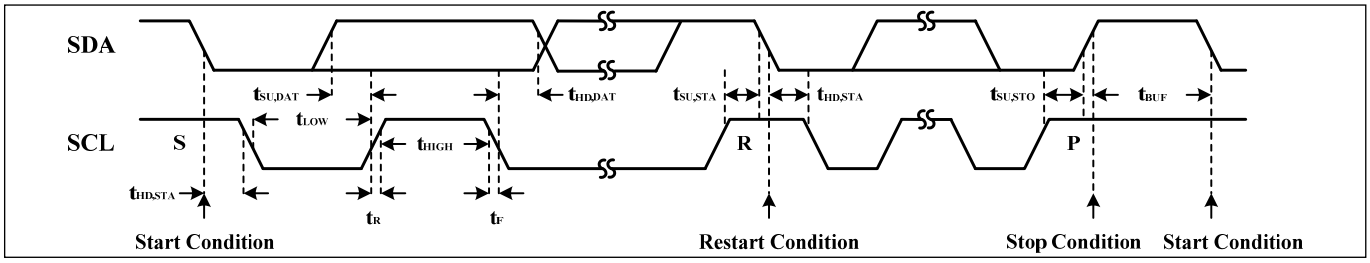


Figure 3 Interface Timing

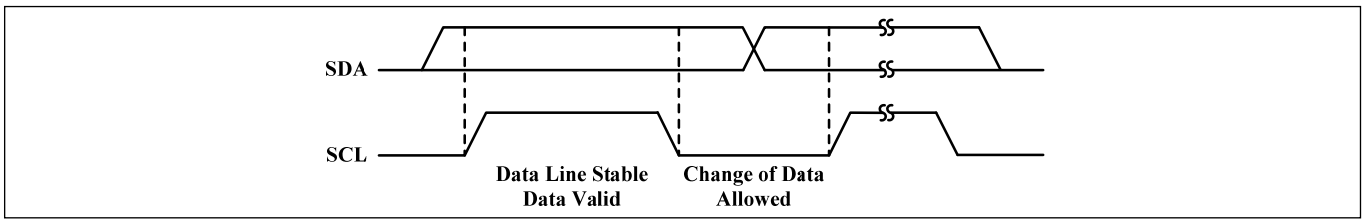


Figure 4 Bit Transfer

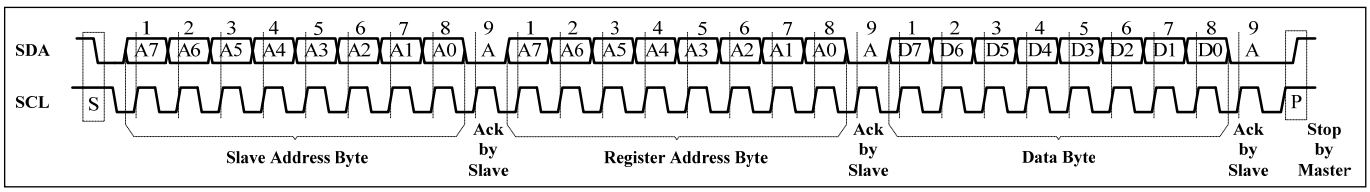


Figure 5 Writing to IS32FL3265A (Typical)

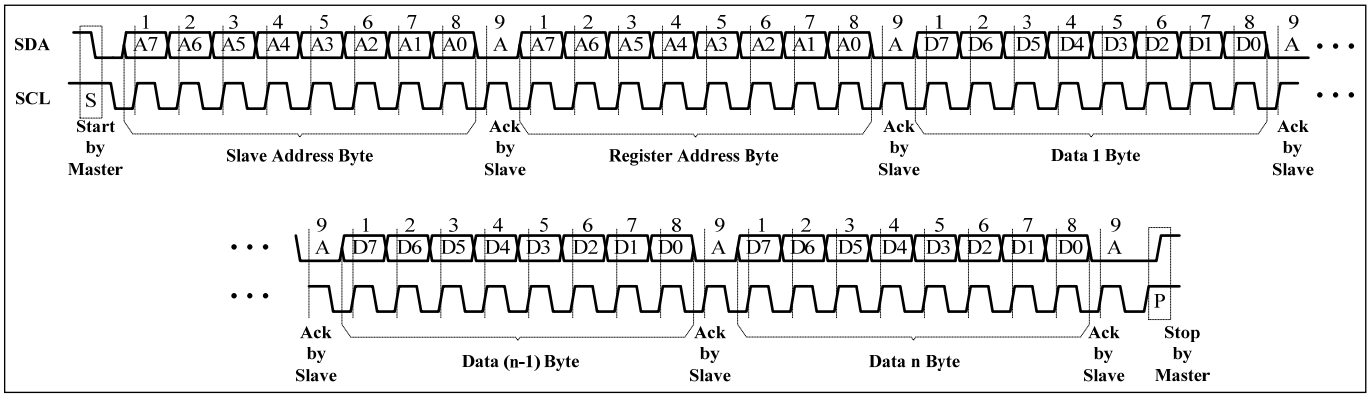


Figure 6 Writing to IS32FL3265A (Automatic Address Increment)

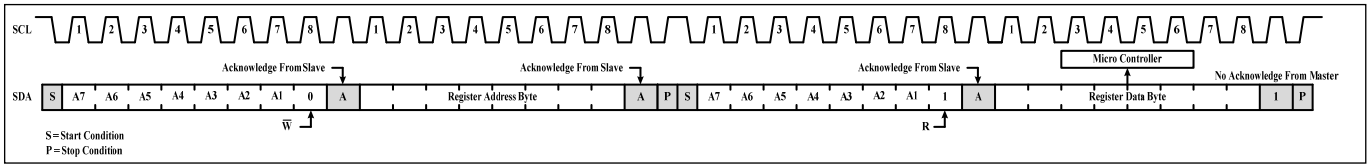


Figure 7 Reading from IS32FL3265A

REGISTER DEFINITIONS

Table 2 Register Function

Address	Name	Function	Table	Default	R/W
00h	Configuration Register	Power control register	3	0000 0000	R/W
01h	Global Current Control Register	Control Global DC current	4	0011 1111	R/W
02h~13h	Scaling Register	Control each channel's DC current	5	1111 1111	R/W
14h	Open Detect Enable Register	Open detect enable	6	0000 0011	R/W
15h~17h	LED Open Status Register (Read Only)	Open information	7	0000 0000	R
18h	Temperature Sensor Register	Temperature information	8	0000 0000	R/W
19h	Spread Spectrum Register	Spread spectrum control register	9	0000 0000	R/W
1Ah~1Ch	DC PWM Register	Disable PWM function	10	0000 0000	R/W
1Dh~1Eh	Phase Delay and Clock Phase Register	Phase Delay and Clock Phase	11	0000 0000	R/W
1Fh~30h	PWM Register	Channel [18:1] PWM register byte	12	0000 0000	R/W
31h~33h	Blinking Enable Register	Enable Blinking state for each LED	13	0000 0000	R/W
34h	Blinking Frequency Register	Blinking frequency setting	14	0000 0000	R/W
35h	Blinking Duty Cycle Register	Blinking duty cycle setting	15	0000 0000	R/W
36h	Scaling Update Register	Update the scaling registers	-	0000 0000	R/W
37h	Update Register	Update the PWM and blinking registers	-	0000 0000	W
3Fh	Reset Register	Reset all registers	-	0000 0000	R/W

Table 3 00h Configuration Register

Bit	D7	D6	D5	D4	D3	D2:D1	D0
Name	-	LGC	CM	PFS	-	SYNC	SSD
Default	0	0	0	0	0	00	0

The Configuration Register sets high/low logic, current multiplier, PWM frequency, synchronization mode and software shutdown mode for the IS32FL3265A.

When SSD bit is "0", the IS32FL3265A is in software shutdown mode. For normal operation the SSD bit should be set to "1".

SYNC bits configure the device into Master or Slave mode. The CLKIO pin has an internal weak pulldown resistor. When the SYNC bits are "10", the CLKIO pin is configured as the master and will output a clock signal for distribution to the slave configured devices. To be configured as a slave device and accept an external clock input the slave device's SYNC bits must be set to "11". The CLKIO clock is only used synchronizing the blink function, and CLKIO frequency is same as blinking setting from 24Hz to 10.66s. There should only be one master and all other CLKIO connected devices should first be configured in slave mode before the master is configured as master mode.

The PFS bit sets the operating PWM frequency, default PWM frequency is 25kHz, when PFS is set to "1", the PWM frequency will change to 200Hz.

CM bit is a current multiplier of all output's current. When CM= "0", $I_{OUT(MAX)}$ follow the formula below or refer to R_{ISET} section in Application Information.

$$I_{OUT\ (MAX)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (1)$$

x = 408, V_{ISET} = 1V.

When CM= "1", the output current will become 1/8 of above setting, which is:

$$I_{OUT\ (MAX)} = \frac{x}{8} \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (1)$$

x = 408, V_{ISET} = 1V.

For applications of $I_{OUT(MAX)}$=6mA~60mA, CM should be set to "0".

For applications of $I_{OUT(MAX)}$=0~7.5mA, recommend to set CM to "1" to ensure good ΔI_{MAT} and ΔI_{OUT}.

When LGC bit is set to "1", the high/low logic will change to 2.4V/0.6V.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

SYNC Master or slave
00/11 no function, CLKIO pull-low
10 Master and CLKIO has square wave output, CLKIO frequency is same as blinking frequency
11 Slave and CLKIO is clock input

PFS PWM frequency setting
0 25kHz
1 200Hz

CM Current multiplier
0 6~60mA
1 1~10mA

LGC H/L logic
0 1.4V/0.4V
1 2.4V/0.6V

Table 4 01h Global Current Control Register

Bit	D7:D6	D5:D0
Name	-	GCC
Default	00	11 1111

GCC and SL control the I_{OUT} as shown in Formula (2).

$$I_{OUT} = I_{OUT\ (MAX)} \times \frac{GCC}{32} \times \frac{SL}{256} \qquad (2)$$

If GCC ≤ 31('01 1111'),

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^{n} \qquad (3)$$

If GCC ≥ 32 ('10 0000'), GCC=32.

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information)

The I_{OUT} of each channel is set by the SL bits of LED Scaling Register (02h~13h). Please refer to the detail information in Table 5.

If GCC=0x05, SL=0xFF, GCC ≤ 31 so GCC=5,

$$I_{OUT} = I_{OUT\ (MAX)} \times \frac{5}{32} \times \frac{255}{256} \qquad (2)$$

If GCC=0x2F, SL=0xFF, GCC ≥ 32 so GCC=32,

$$I_{OUT} = I_{OUT\ (MAX)} \times \frac{255}{256} \qquad (2)$$

Table 5 02h~13h Scaling Register

Bit	D7:D0
Name	SL[7:0]
Default	1111 1111

Each output has 8 bits to modulate DC current in 256 steps.

The value of the SL Registers scales the IOUT current of each output channel.

I_{OUT} computed by Formula (2):

$$I_{OUT} = I_{OUT\ (MAX)} \times \frac{GCC}{32} \times \frac{SL}{256} \qquad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current set by R_{ISET}. GCC (D5~D0) are the global current setting bits. SL D7~D0=0xFF is the default value, resulting in no LED current, for LEDs to function need to program these bits to a value from 0x01 to 0xFF.

Scaling Registers 02h~13h must be updated by writing to the Scaling Update Register 36h. For DC mode (PWM disabled), each register will be updated immediately when it is written. For PWM mode, each register will be updated at the PWM falling edge, except not on the first PWM cycle.

Table 6 14h Open Detect Enable Register

Bit	D7:D2	D1	D0
Name	-	ODF	ODE
Default	00000	0	0

ODE enables Open LED detection and stores this open information in LED Open status registers 15h~17h. The open information will continue updating until detection is disabled by writing "0" to ODE. Writing a "1" to ODF bit enables reporting of the open information on the INTB pin. When ODF is "1", any detected open LED condition on OUT1~OUT18 will cause the INTB pin to go logic low.

ODE Open Detect Enable
0 Detect disable
1 Detect enable

ODF Open Report Enable
0 Report disable
1 Report enable

Table 7-1 15h LED Open Status Register 1

Bit	D7	D6:D4	D3	D2:D0
Name	-	OP[6:4]	-	OP[3:1]
Default	0	000	0	000

Table 7-2 16h LED Open Status Register 2

Bit	D7	D6:D4	D3	D2:D0
Name	-	OP[12:10]	-	OP[9:7]
Default	0	000	0	000

Table 7-2 17h LED Open Status Register 3

Bit	D7	D6:D4	D3	D2:D0
Name	-	OP[18:16]	-	OP[15:13]
Default	0	000	0	000

Open status registers 15h~17h are updated if there is an open LED condition and if bit ODE of register 14h was set to "1". Register 15h~17h will be cleared upon reading the register.

OPx Open Information of OUT18:OUT1
0 No LED open detected
1 LED open detected

Table 8 18h Temperature Status Register

Bit	D7	D6	D5	D4	D3:D2	D1:D0
Name	TSDDE	TRDE	TSDF	TF	TROF	TS
Default	0	0	0	0	00	00

This register stores the temperature point of the IC. When TF=1, the IC die temperature has exceeded the temperature point. When thermal shutdown happens, the TSDF will set to "1" to flag the thermal shutdown has occurred.

Write 18h with C0h to enable read back if die temperature has or has not exceeded the set point.

TROF Percentage of output current before thermal shutdown happens
00 100%
01 75%
10 55%
11 30%

TS Temperature Point, Thermal roll-off start point
00 140°C
01 120°C
10 100°C
11 90°C

TF Temperature Flag
0 Set point not reached
1 Reached the set point

TSDF Thermal Shutdown Flag
0 No thermal shutdown happens
1 Thermal shutdown happens

TRDE Thermal roll off Detect Enable
0 Disable the thermal roll off detect, thermal roll off information will not store in TF
1 Enable the thermal roll off detect, thermal roll off information stored in TF

TSDDE Thermal Shutdown Detect Enable
0 Disable thermal shutdown detect, thermal shutdown information will not be stored in TSDF
1 Enable thermal shutdown detect thermal shutdown information will be stored in TSDF

Table 9 19h Spread Spectrum Register

Bit	D7:D5	D4	D3:D2	D1:D0
Name	-	SSP	RNG	CLT
Default	000	0	00	00

This register enable the spread spectrum function, adjust the cycle time and range.

SSP Spread Spectrum Enable
0 Disable
1 Enable

CLT Spread Spectrum Cycle Time
00 1980μs
01 1200μs
10 820μs
11 660μs

RNG Spread Spectrum Range
00 ±5%
01 ±15%
10 ±24%
11 ±34%

Table 10-1 1Ah DC PWM Register(PWM=256/256)

Bit	D7	D6:D4	D3	D2:D0
Name	-	DP[6:4]	-	DP[3:1]
Default	0	000	0	000

Table 10-2 1Bh DC PWM Register(PWM=256/256)

Bit	D7	D6:D4	D3	D2:D0
Name	-	DP[12:10]	-	DP[9:7]
Default	0	000	0	000

Table 10-3 1Ch DC PWM Register(PWM=256/256)

Bit	D7	D6:D4	D3	D2:D0
Name	-	DP[18:16]	-	DP[15:13]
Default	0	000	0	000

When DPx bit is set to 1, the associated OUTx PWM will become 256/256, the OUTx current is a DC value, not PWM controlled.

DPx	DC PWM command of OUT18:OUT1
0	PWM decided by Registers 1Fh-30h
1	no PWM, DC output

Table 11-1 1Dh Phase Delay and Clock Phase Register

Bit	D7	D6:D4	D3:D1	D0
Name	-	PS[3:1]	-	PDE
Default	0	000	000	0

Table 11-2 1Eh Phase Delay and Clock Phase Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	PS[9:7]	-	PS[6:4]
Default	0	000	0	000

IS32FL3265A features a 9 phase delay function enabled by PDE bit.

PDE	Phase Delay Enable
0	Phase delay disable
1	Phase delay enable

PSx	Phase select
0	OUTx x2 Phase delay 0 degree, PS1 is for OUT1 &OUT2, PS2 is for OUT3 & OUT4…
1	OUTx x2 Phase delay 180 degree, PS1 is for OUT1 &OUT2, PS2 is for OUT3 & OUT4…

Table 12 1Fh-30h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each OUTx has 1 byte to modulate the PWM duty cycle in 256 steps.

The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED}.

I_{LED} computed by Formula (4):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT} \quad (4)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (5)$$

$$I_{OUT} = I_{OUT\ (MAX)} \times \frac{GCC}{32} \times \frac{SL}{256} \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET}, GCC is the global current setting (GCC), and SL is the 8-bit scaling of each output.

For example, if the data in OUT1 PWM register is “0000 0100”, then the associated PWM is the fourth step (4/256).

Table 13-1 31h Blinking Enable Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	BP[6:4]	-	BP[3:1]
Default	0	000	0	000

Table 13-2 32h Blinking Enable Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	BP[12:10]	-	BP[9:7]
Default	0	000	0	000

Table 13-3 33h Blinking Enable Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	BP[18:16]	-	BP[15:13]
Default	0	000	0	000

The Blinking Enable Registers store the Blinking mode enable bit of each OUTx channel. The data sent to the registers will be stored in temporary registers only, a write operation of “0000 0000” value to the Update Blinking Register (37h) is required to update it.

BPx	Blinking Enable Bit
0	PWM Mode
1	Blinking Mode

Table 14 34h Blinking Frequency Register

Bit	D7:D0
Name	BLF
Default	0000 0000

The Blinking Frequency Register stores the blinking frequency of the outputs. The blinking period is controlled through 256 linear steps from 00h (41ms, frequency 24Hz) to FFh (10.66s). Blinking frequency is computed by:

Blinking frequency (Hz) = 24/(BLF[7:0] + 1)

The data sent to the Blinking Frequency Register will be stored in temporary bits, a write operation of "0000 0000" value to the Update Register (37h) is required to update it.

Table 15 35h Blinking Duty Cycle Register

Bit	D7:D0
Name	BLD
Default	0000 0000

The Blinking Duty Cycle Register stores blinking duty cycle information (ON/OFF ratio in %). The blinking duty cycle can be linearly programmed from 0% (BLD=0x00) to 99.6% (BLD=0xFF). Blinking duty cycle computed by:

Blinking duty cycle = BLD[7:0] / 256

The data sent to the Blinking Duty Cycle Register will be stored in temporary bits, a write operation of "0000 0000" value to the Update Register (37h) is required to update it.

36h Scaling Update Register

A Write of 00h to the Scaling Update Register is required to update the Scaling Registers (02h~13h) values.

37h Update Register

A Write of 00h to Update Register is required to update the PWM Registers and Blinking Frequency Register/ Blinking Duty Cycle Register (1Fh~30h, 34h~35h) values.

3Fh Reset Register

A write of 0xAE to the Reset Register will reset all the IS32FL3265A registers to their default values. On initial power-up, the IS32FL3265A registers are reset to their default values for a blank display. A write of "1" to the SSD bit in the Configuration Register 00h is required to enable the IS32FL3265A since the SSD default value is "0" or software shutdown.

APPLICATION INFORMATION

R_{ISET}

The maximum output current $I_{OUT(MAX)}$ of OUT1~OUT18 can be adjusted by external resistor, R_{ISET}, as described in Formula (1).

$$I_{OUT\ (MAX)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (1)$$

x = 408, V_{ISET} = 1V.

The max I_{OUT} result is based on register setting as below (CM is D5 of Configuration Register (00h)):

When CM= “0”, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF

The recommended minimum value of R_{ISET} is 6.8kΩ.

When R_{ISET}=20kΩ, $I_{OUT(MAX)}$=20.4mA.

When R_{ISET}=6.8kΩ, $I_{OUT(MAX)}$=60mA.

When CM= “1”, GCC= 0x20, Scaling= 0xFF, PWM= 0xFF

The output current will become 1/8 of above setting, which is:

$$I_{OUT\ (MAX)} = \frac{x}{8} \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (1)$$

x = 408, V_{ISET} = 1V.

When R_{ISET}=20kΩ, $I_{OUT(MAX)}$=2.55mA.

When R_{ISET}=6.8kΩ, $I_{OUT(MAX)}$=7.5mA.

R_{ISET} should be close to pin 25 and the ground side should connected to a nearby GND plane.

CURRENT SETTING

The maximum output current is set by the external resistor R_{ISET}. The current of each output can be adjusted with the SL 8 bits of LED Scaling Register (02h~13h).

Some applications may require the IOUT of each channel to be adjusted independently. For example, if OUT1 drives 1 LED and OUT2 drives 2 parallel LEDs, and they should have the same average current of 10mA, we can set RISET=20kΩ for IOUT of 20.4mA, and configure the following registers 01h=0x20 (GCC= 32), 02h=0x80 (Scaling OUT1), and 03h=0xFF (Scaling OUT2). The result is OUT1 sinks 10mA and OUT2 sinks 20.4mA which will be shared by the two LEDs in parallel (10mA each).

Another example, for an RGB LED, OUT1 is Red, OUT2 is Green and OUT 3 is Blue, with the same GCC (01h) SL (02h~13h) bits and PWM value, the LED may looks a pinkish, or not so white. In this case, the SL bits can be used to adjust the current of the RGB IOUTx to create a pure white color. These Scaling Registers can also be referred to as white balance registers.

PWM CONTROL

The 18 PWM Registers (1Fh~30h) can modulate the average LED brightness of each 18 channels with 256 steps. For example, if the data in OUT1 PWM register is “0000 0100”, then the associated PWM is the fourth step (4/256).

Continuously updating new values to the PWM registers will modulate the brightness of the LEDs to achieve a breathing effect.

PWM FREQUENCY SELECT

The IS32FL3265A output channels operate with a default 8 bit PWM resolution and a PWM frequency of 200Hz or 25kHz (register selectable). Because all the OUTx channels are synchronized, the DC power supply mau experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the PWM frequency range. To avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS32FL3265A’s output PWM frequency above/below the audible range. The Control Register (00h) can be used to set the switching frequency to 200Hz or 25kHz, to avoid the audible range.

OPEN DETECT FUNCTION

IS32FL3265A has open detect bit for each LED.

By setting the ODE bit of Open Detect Enable Register (14h) from “0” to “1” (store open information), the LED Open Register will store the open LED information so the MCU can read LED status from registers 95h~97h. The open information will continue updating until ODE is set to “0”. The ODF bit can be set to “1” to enable reporting of open LED information on the INTB pin. When ODF is “0”, the open LED information will not be reported on the INTB pin. When ODF is “1”, any OUTx with a detected open LED will cause the INTB pin to go logic LOW.

The Global Current Control Register (01h) needs to set to a value in the range of 0x10~0x48 in order to correctly detect an open LED.

SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome Electromagnetic Interference (EMI) is of concern. To optimize EMI performance, the

IS32FL3265A spread spectrum function can be enabled. By setting the RNG bit of the Spread Spectrum Register (19h), a Spread Spectrum range can be selected from ±5% /±15% /±24% /±34%. Spread spectrum can spread the total electromagnetic emitting energy into a wider frequency range that significantly lowers the peak radiated energy. With spread spectrum enabled and proper PCB layout, it is possible to pass EMI tests which were previously difficult to pass.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to "0", the IS32FL3265A will operate in software shutdown mode. When the IS32FL3265A is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers remain accessible. Typical current consumption is 3μA (VCC=5V). The default SSD value on power up is "0", for normal operation the SSD needs to be written with a "1".

Hardware Shutdown

The IS32FL3265A enters hardware shutdown when the SDB pin is pulled low. All current sources are disabled during hardware shutdown, typical the current consumption is 3μA (V_{CC}=5V).

The IS32FL3265A exits shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but all the register information is retained. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V while the SDB pin is pulled low, all Function Registers must be re-initialized before the SDB pin is pulled high.

LAYOUT

The IS32FL3265A consumes lots of power so proper PCB layout will help improve itsreliability. Below are basic PCB layout factors to consider.

Power Supply Lines

When designing the PCB layout, the first step to consider is the power supply traces and GND connection. High current traces, digital and analog supply traces and GND traces should be separated to avoid noise contamination from the switching digital block from affecting the analog block.

At least one 0.1μF capacitor, if possible in parallel with a 1μF capacitor is recommended to connect from the power supply pin of the chip directly to ground. To be effective, these capacitors must be placed close to the chip and the capacitor ground should be well connected to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip.

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. The maximum power dissipation can be calculated using the following equation:

$$p_{D(MAX)} = \frac{T_{J(\max)} - T_A}{\theta_{JA}}$$

Where $P_{D(MAX)}$ is the maximum allowable power dissipation, $T_{J(MAX)}$ is the maximum allowable junction temperature, T_A is ambient temperature of the device

For example, when T_A=25°C

$$P_{D(MAX)} = \frac{150°C - 25°C}{33.8°C/W} \approx 3.7W$$

Figure 8, shows the power derating of the IS32FL3265A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

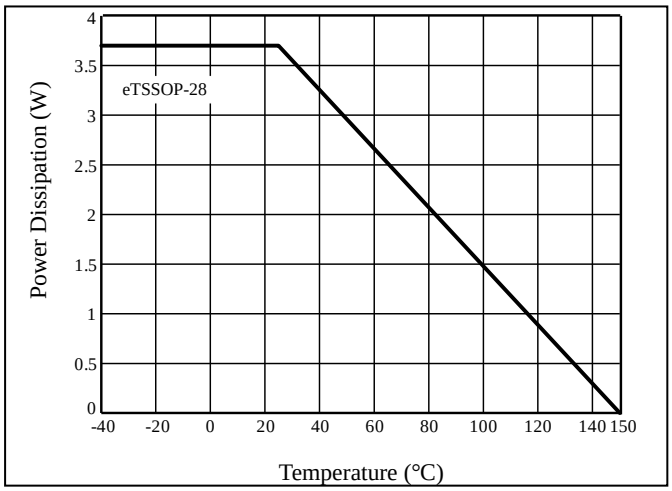


Figure 8 Dissipation Curve

The thermal pad of IS32FL3265A should connect to a large copper GND net (preferably double sided PCB). Use 9 or 16 vias to connect the GND copper area directly under the IC thermal pad with a copper pad on the opposite layer (2 layer PCB). The grounded copper area should be as large area as possible to help distribute the thermal energy from the IS32FL3265A.

Current Rating Example

For R_{ISET}=20kΩ ($I_{OUT(MAX)}$=20.4mA), the current rating for each net is as follows:

• VCC pin maximum current (I_{CC}) is 10mA when V_{CC}=5V, the total OUTx current can as much as 20.4mA×18=367.2mA, the recommended trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.30mm~0.5mm,

• Output pins=20.4mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

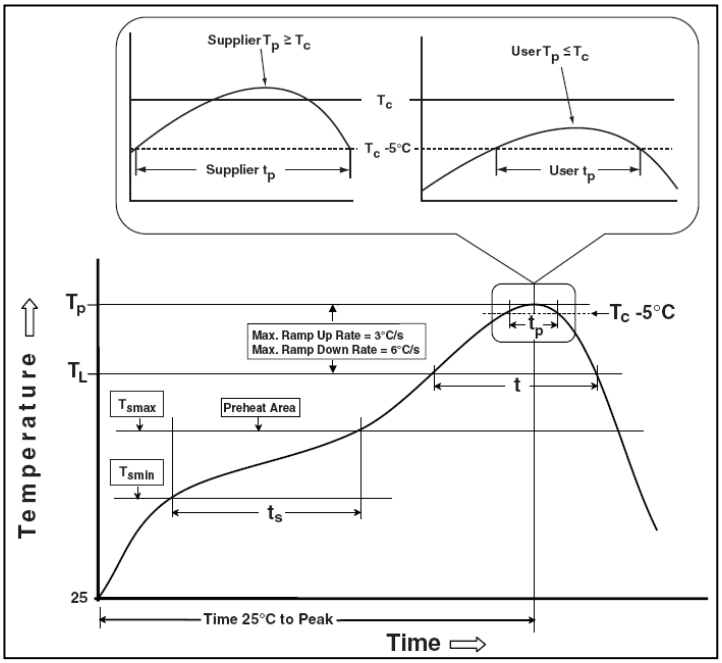
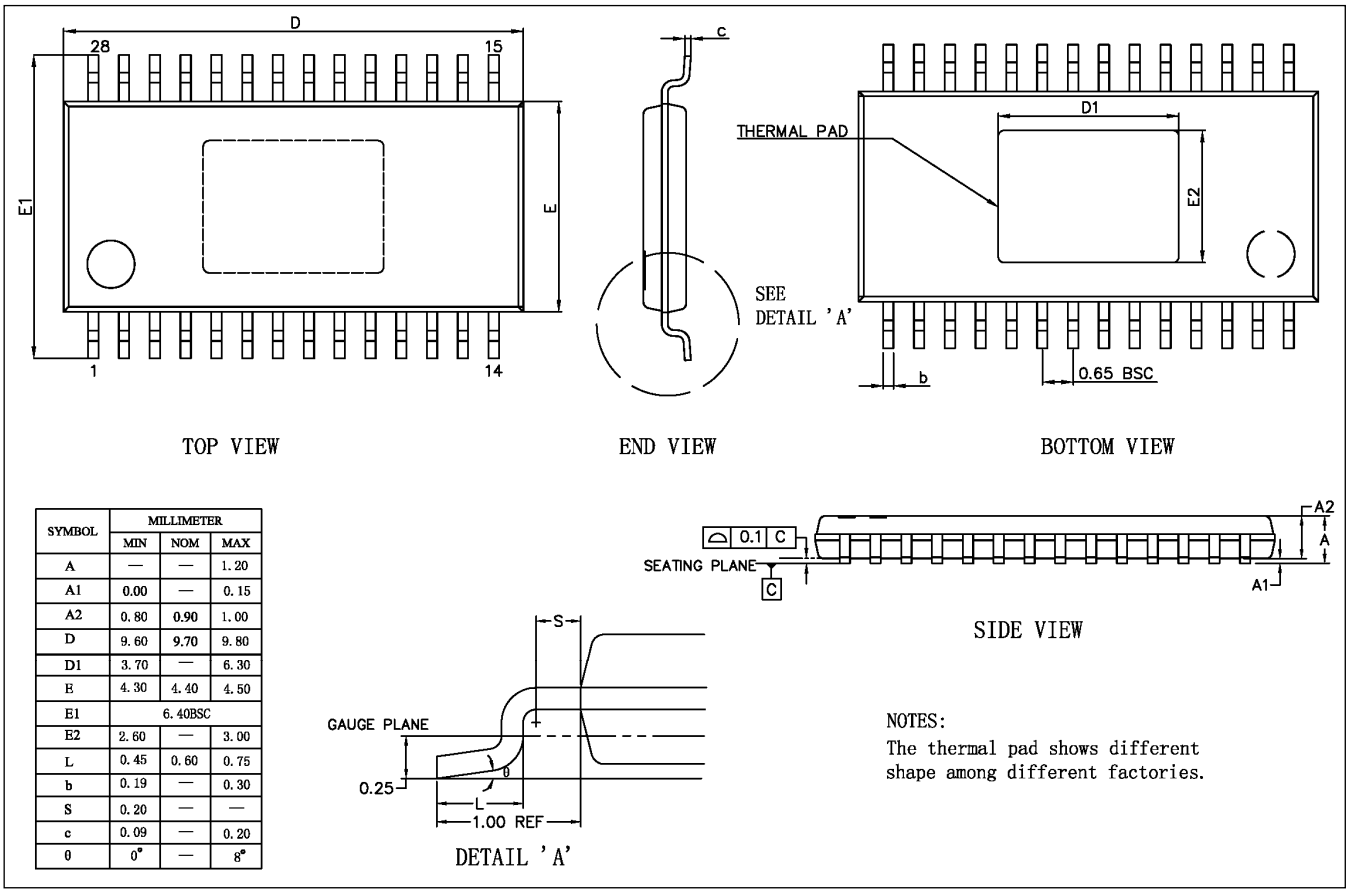


Figure 9 Classification Profile

PACKAGE INFORMATION

eTSSOP-28

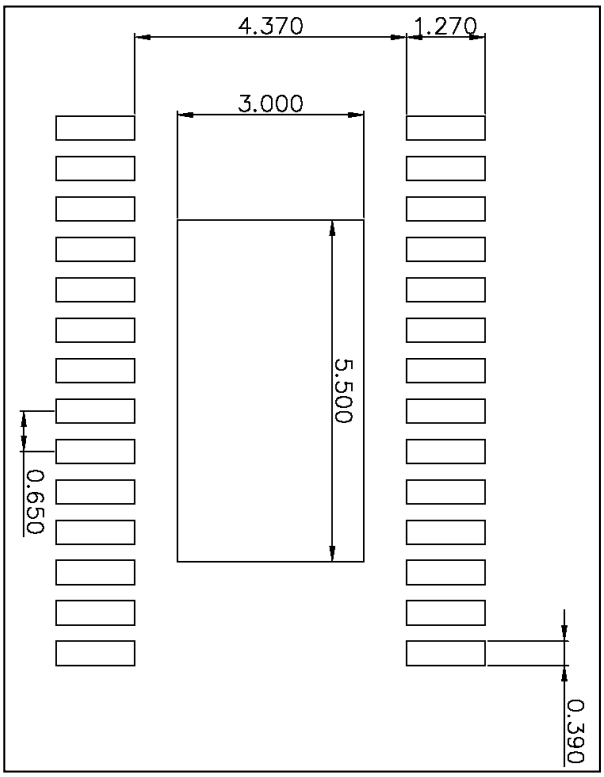


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.00
D	9.60	9.70	9.80
D1	3.70	—	6.30
E	4.30	4.40	4.50
E1	6.40BSC		
E2	2.60	—	3.00
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

eTSSOP-28



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2020.01.02