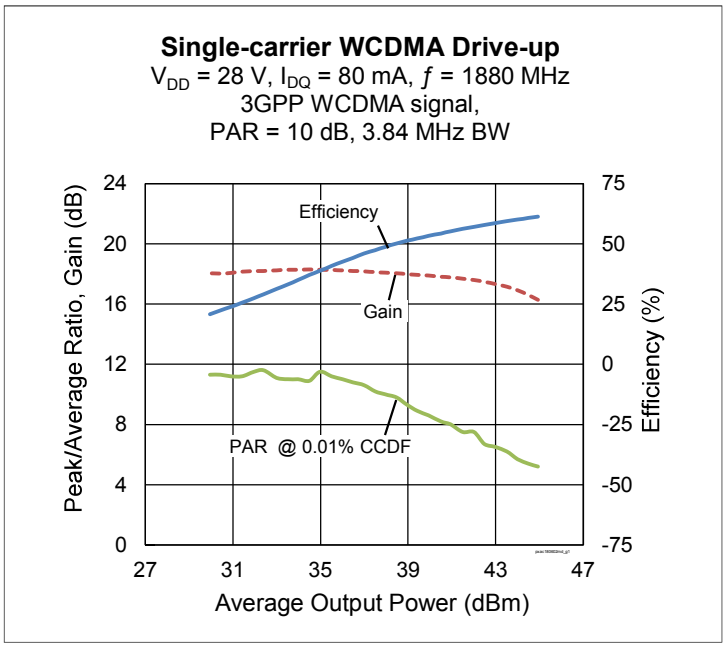
Thermally-Enhanced High Power RF LDMOS FET
60 W, 28 V, 1805 – 1880 MHz

Description

The PXAC180602MD is a 60-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 1805 to 1880 MHz frequency band. Features include dual-path design, input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PXAC180602MD
Package PG-HB1DSO-4-1



Features

- Broadband internal input and output matching
- Asymmetric Doherty design
  - Main : P1dB = 20 W Typ
  - Peak : P1dB = 40 W Typ
- Typical Pulsed CW performance, 1880 MHz, 28 V, 160 µs pulse width, 10% duty cycle, class AB, Doherty Configuration
  - Output power at P_{1dB} = 10 W
  - Efficiency = 58%
  - Gain at P_{3dB} = 19 dB
- Integrated ESD protection
- Human Body Model, Class 1B (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Infineon production Doherty test fixture)
V_{DD} = 28 V, I_{DQ} = 80 mA, P_{OUT} = 8.9 W avg, V_{GSPK} = 160 mA–1.3 V, f_1 = 1840 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16.5	17.7	—	dB
Drain Efficiency	η_D	51.0	54.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–27.6	–25	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
On-State Resistance (main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.76	—	Ω
(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.36	—	Ω
Operating Gate Voltage (main)	V_{DS} = 26 V, I_{DQ} = 80 mA	V_{GS}	2.3	2.6	3.0	V
(peak)	V_{DS} = 26 V, I_{DQ} = 0 mA	V_{GS}	0.8	1.4	1.8	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (Doherty, T_{CASE} = 70°C, 55 W CW)	$R_{\theta JC}$	2.4	°C/W

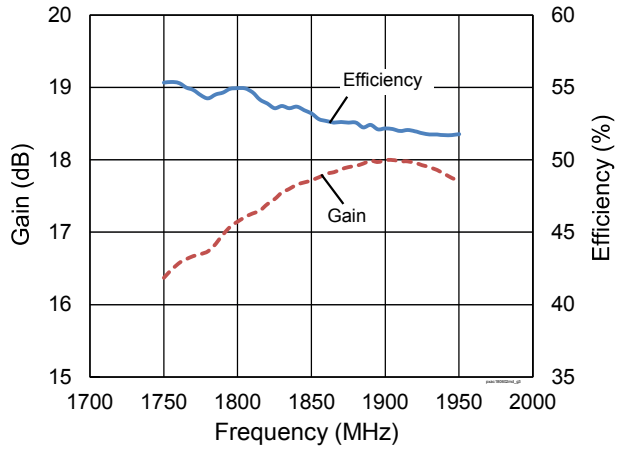
Ordering Information

Type and Version	Order Code	Package Description	Shipping
PXAC180602MD V1 R500	PXAC180602MDV1R500XUMA1	PG-HB1DSO-4-1	Tape & Reel, 500 pcs

Typical Performance (data taken in a production Doherty test fixture)

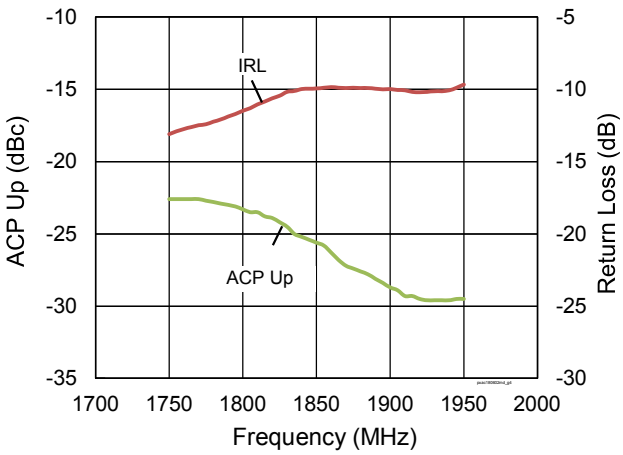
Single-carrier WCDMA Broadband Performance

V_{DD} = 28 V, I_{DQ} = 80 mA, P_{OUT} = 39.5dBm, 3GPP WCDMA signal, PAR = 10 dB



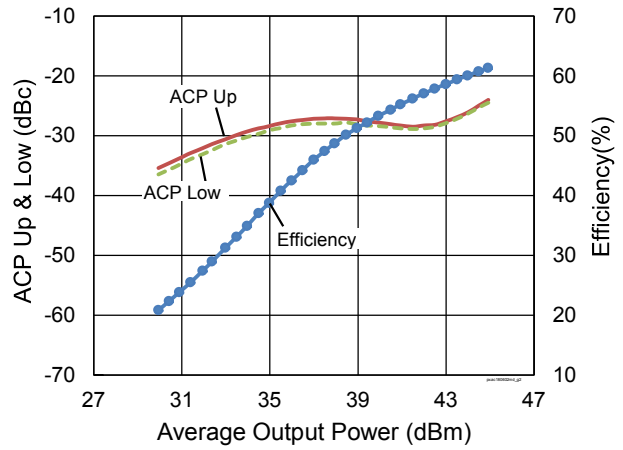
Single-carrier WCDMA Broadband Performance

V_{DD} = 28 V, I_{DQ} = 80 mA, P_{OUT} = 39.5dBm, 3GPP WCDMA signal, PAR = 10 dB



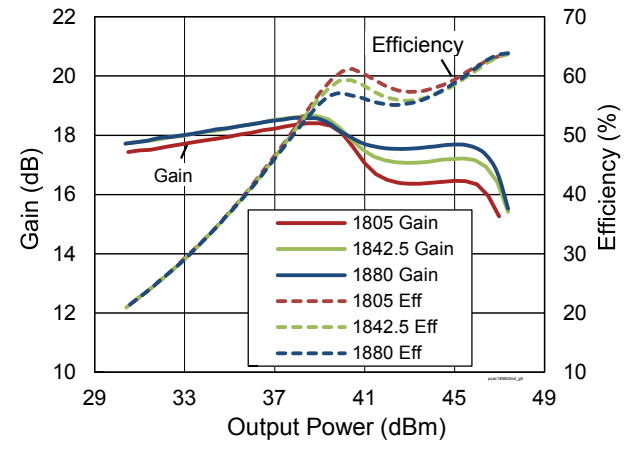
Single-carrier WCDMA Drive-up

V_{DD} = 28 V, I_{DQ} = 80 mA, f = 1880 MHz, 3GPP WCDMA signal, PAR = 10 dB, BW = 3.84 MHz

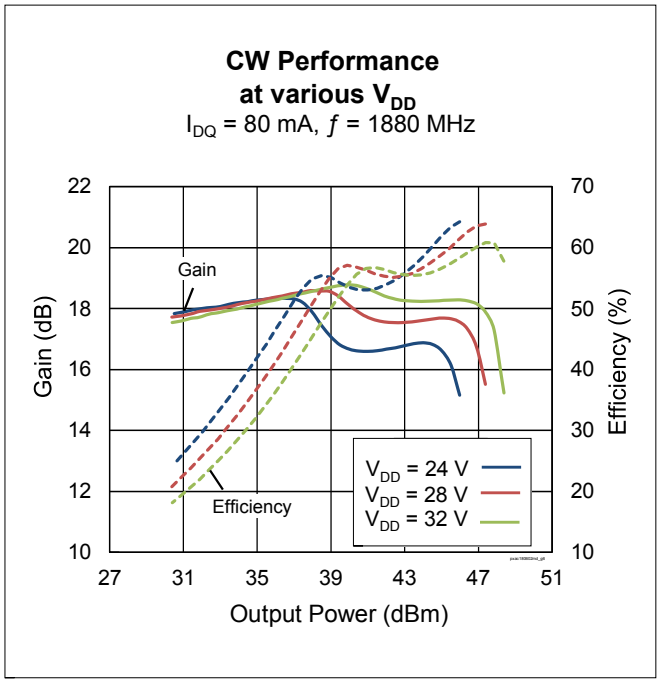


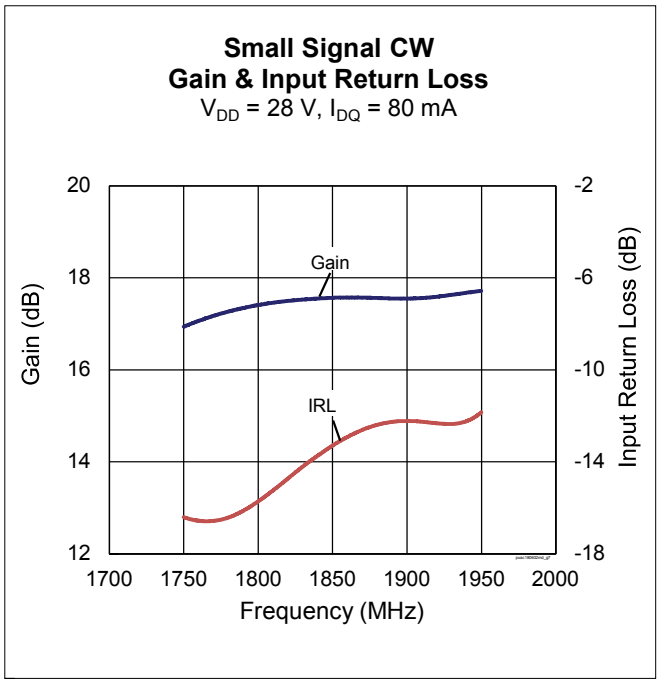
CW Performance

V_{DD} = 28 V, I_{DQ} = 80mA



Typical Performance (cont.)





Load Pull Performance – P_{1dB}

Main Side Load Pull Performance – CW signal: V_{DD} = 28 V, I_{DQ} = 85 mA, Class AB

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1805	7.3-j16.9	8.8-j10.33	20.55	43.62	23	63.4	12.8-j1.9	21.86	41.73	14.89	70.8
1843	6.6-j18.9	8.4-j10.4	20.71	43.29	21.33	60.8	11.8-j4.4	22.12	42.10	16.22	69.6
1880	8.3-j21.5	7.5-j9.3	20.67	43.30	21.38	63.4	9.3-j3.9	21.86	41.87	15.38	69.4

Peak Side Load Pull Performance – CW signal: V_{DD} = 28 V, V_{GSPK} = 1.4 V

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1805	13.5 – j0.7	5.2 – j8.4	16.92	46.35	43.15	63.8	9.9 – j8.0	17.51	45.09	32.28	72.3
1842	7.7 – j0.2	4.7 – j8.4	16.8	46.43	43.95	63.3	9.0 – j7.1	17.47	45.14	32.66	72.7
1880	4.8 – j0.2	4.4 – j8.5	16.7	46.42	43.85	62.8	8.6 – j6.8	17.36	44.99	31.55	72.4

Load Pull Performance – P_{3dB}

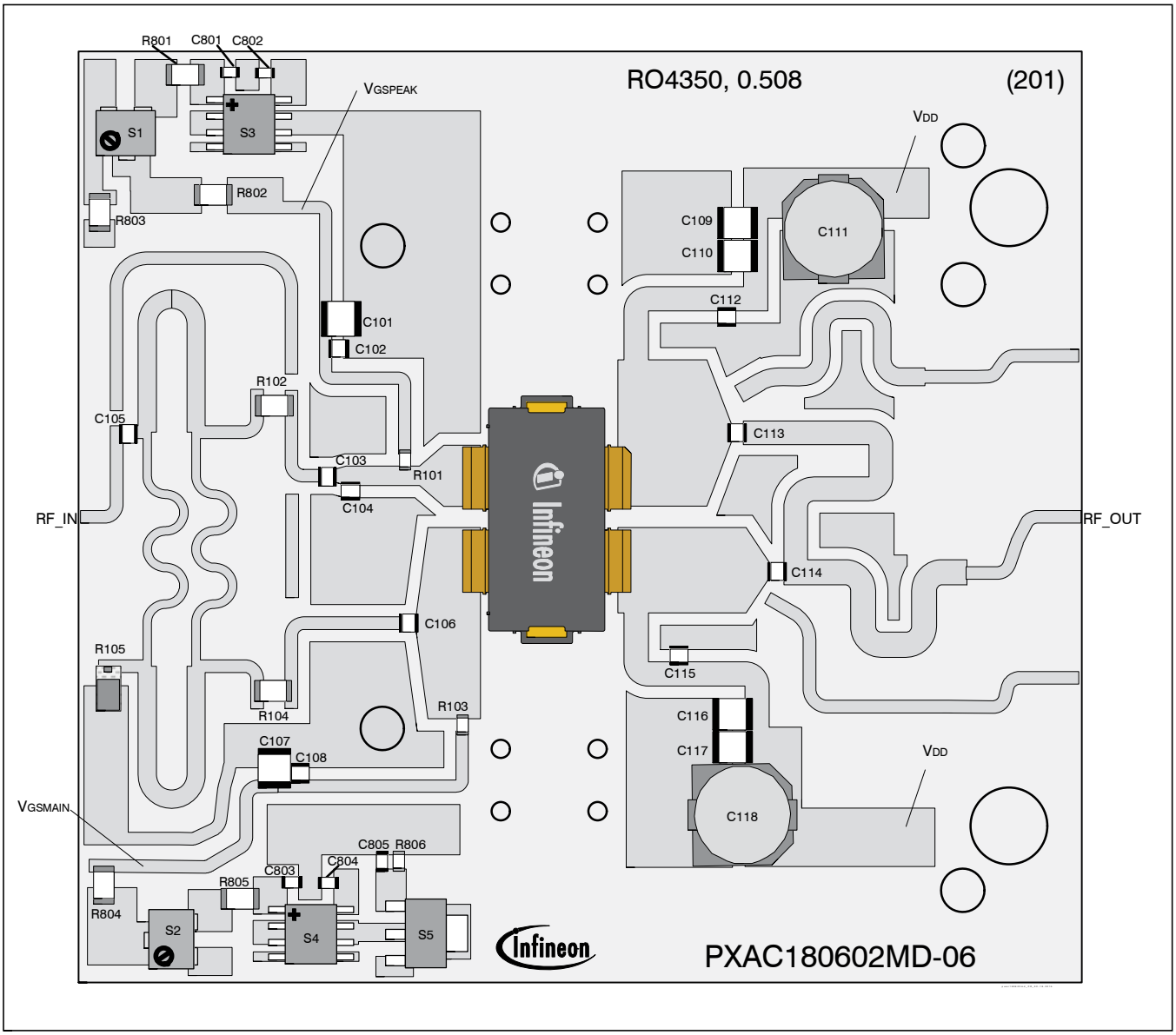
Main Side Load Pull Performance – CW signal: V_{DD} = 28 V, I_{DQ} = 85 mA, Class AB

		P_{3dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1805	7.3-j16.9	9.0-j11.7	18.65	44.30	26.92	63.8	13.1-j7.1	19.78	43.28	21.28	70.8
1843	6.6-j18.9	9.0-j11.7	19	43.98	25	62.0	11.5-j5.9	20	42.94	19.68	69.5
1880	8.3-j21.5	8.9-j11.9	19.26	43.89	24.5	61.7	11.1-j6.4	20.2	42.91	19.54	69.0

Peak Side Load Pull Performance – CW signal: V_{DD} = 28 V, V_{GSPK} = 1.4 V

		P_{3dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
1805	13.5 – j0.7	5.1 – j9.2	14.94	47.00	50.12	64.4	10.0 – j8.3	15.52	45.58	36.14	71.6
1842	7.7 – j0.2	5.0 – j9.2	14.9	47.00	50.1	64.6	9.3 – j7.7	15.45	45.67	36.9	72.0
1880	4.8 – j0.2	4.6 – j9.35	14.72	47.00	50.1	63.3	8.1 – j7.2	15.37	45.74	37.5	71.6

Reference Circuit , 1805 – 1880 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

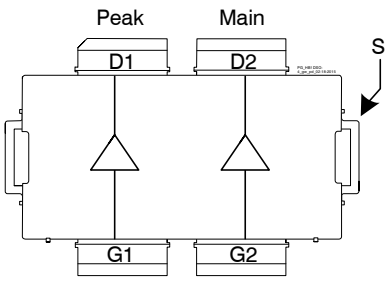
Reference Circuit Assembly

DUT	PXAC180602MD V1
Test Fixture Part No.	LTA/PXAC180602MD V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 1805 – 1880 MHz
Find Gerber files for this test fixture on the Infineon Web site at http://www.infineon.com/rfpower	

Components Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101, C107	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C102, C103, C106, C108	Capacitor, 24 pF	ATC	ATC100A240JW150XB
C104	Capacitor, 2.4 pF	ATC	ATC100A2R4CW150XB
C105	Capacitor, 15 pF	ATC	ATC100A150JW150XB
C801, C802, C803, C804, C805	Capacitor, 1000 pF	Panasonic Electronic Components	ECJ-1VB1H102K
R101, R103	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-3GEYJ100V
R102, R104	Resistor, 0.0 Ω	Panasonic Electronic Components	ERJ-8GEY0R00V
R105	Resistor, 50 Ω	Anaren	C16A50Z4
R801, R805	Resistor, 100 Ω	Panasonic Electronic Components	ERJ-8GEYJ101V
R802, R803, R804	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-8GEYJ100V
R806	Resistor, 1.3k	Panasonic Electronic Components	ERJ-3GEYJ132V
S1, S2	Potentiometer, 2k Ω	Bourns Inc.	3224W-1-202E
S3, S4	Voltage Regulator	Texas Instruments	LM78L05ACM
S5	Transistor	Infineon Technologies	BCP56
Output			
C109, C110, C116, C117	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C112, C113, C114, C115	Capacitor, 24 pF	ATC	ATC100A240JW150XB
C111, C118	Capacitor, 100 µF	Panasonic Electronic Components	EEE-FP1V101AP

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (Peak)
D2	Drain device 2 (Main)
G1	Gate device 1 (Peak)
G2	Gate device 2 (Main)
S	Source (flange)

Lead connections for PXAC180602MD

Package Outline Specifications

Package PG-HB1DSO-4 with Formed Leads

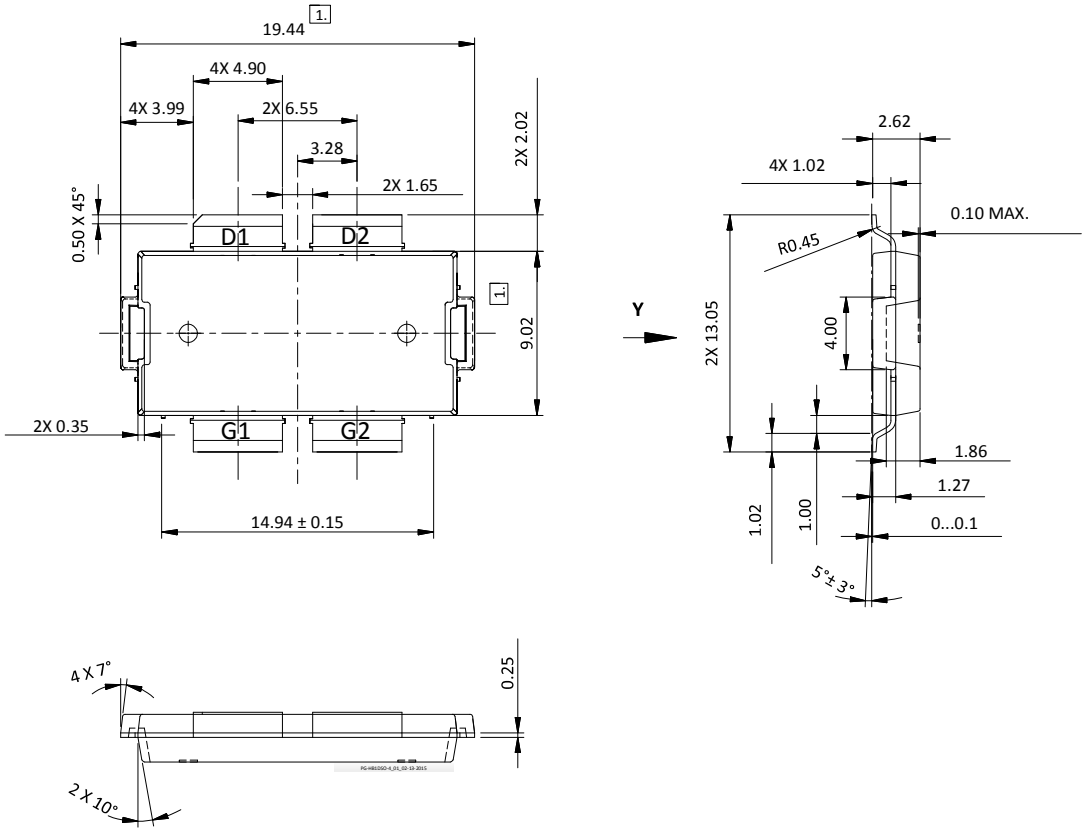


Diagram Notes–unless otherwise specified:

1. Mold/Dam Bar/Metal protusion of 0.30mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Exposed metal surface pre-plated, may not be covered by mold compound.
7. All tolerances ± 0.1mm unless specified otherwise.
8. All metal surfaces pre-plated, except area of cut.
9. Lead thickness: 0.25 mm.
10. Gold plating thickness: 0.25 micron [10 microinch] max.
11. Pins: D1, D2 – drain; G1, G2 – gate; S – source.

Package Outline Specifications (cont.)

Package PG-HB1DSO-4 with Formed Leads (bottom side)

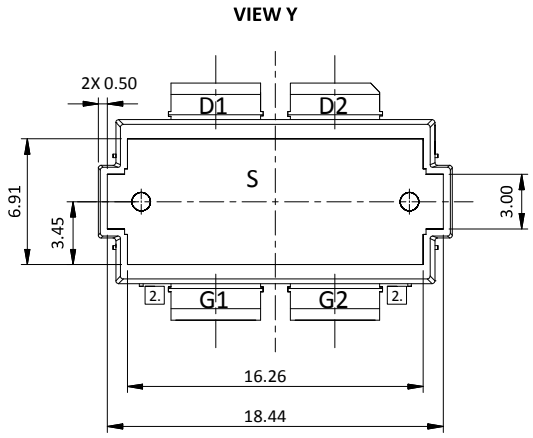


Diagram Notes–unless otherwise specified:

1. Mold/Dam Bar/Metal protusion of 0.30mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Exposed metal surface pre-plated, may not be covered by mold compound.
7. All tolerances ± 0.1mm unless specified otherwise.
8. All metal surfaces pre-plated, except area of cut.
9. Lead thickness: 0.25 mm.
10. Gold plating thickness: 0.25 micron [10 microinch] max.
11. Pins: D1, D2 – drain; G1, G2 – gate; S – source.

Find the latest and most complete information about products and packaging at the Infineon Internet page
http://www.infineon.com/rfpower