HITAG RO64

HTCICC64

Rev. 3.1 — 17 July 2008
152131

Product data sheet
COMPANY PROPRIETARY

1. General description

The HITAG product line is well known and established in the contactless identification market.

Due to the open marketing strategy of NXP Semiconductors there are various manufacturers well established for both the transponders / cards as well as the Read/Write Devices. All of them supporting HITAG transponder IC's.

With the new HITAG RO64, NXP is addressing the low end LF market, by offering a preprogrammed, read-only IC variant.

The advantages of this transponder IC are:

- proven HITAG performance
- easy to assemble because of mega-bumps
- strong RF-modulation
- low cost manufacturing because of preprogrammed TTF code and 210 pF Cres

HITAG RO64 operates in an continuos TTF mode where he modulates the readerfield with it´s preprogrammed 64 bit memory content

2. Features

2.1 Features list

- Integrated Circuit for Contactless Identification Transponders and Cards
- Integrated resonance capacitor of 210 pF with ± 5% tolerance over full production
- Frequency range 100 to 150 kHz.
- 64 bit preprogrammed TTF response
- 10 years data retention
- Delivery form: sawn, gold-megabumped 8” Wafer

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
HTCICC6401EW/C1	Wafer	Au-bumped die on sawn wafer	-

4. Block diagram

The HITAG RO64 Transponder requires no external power supply. The contactless interface generates the power supply and the system clock via the resonant circuitry by inductive coupling to the Read/Write Device (RWD). The interface also demodulates data transmitted from the RWD to the HITAG RO64 Transponder, and modulates the magnetic field for data transmission from the HITAG RO64 Transponder to the RWD.

Data are stored in a non-programmable memory (EEPROM).

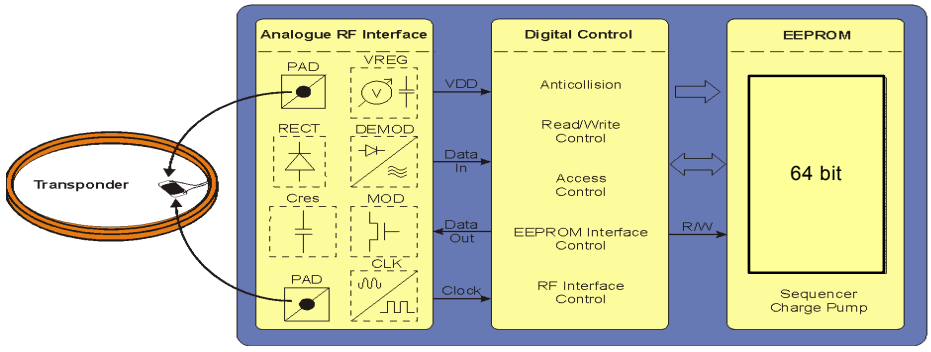


Fig 1. Block diagram

5. Functional description

5.1 Memory organization

TTF ID7:							
MSB							LSB
1	1	1	1	1	1	1	1

TTF ID6:							
MSB							LSB
1	VBit 07	VBit 06	VBit 05	VBit 04	P VBit 07-04	VBit 03	VBit 02

TTF ID5:							
MSB							LSB
VBit 01	VBit 00	P VBit 03-00	DBit 31	DBit 30	DBit 29	DBit 28	P DBit 31-28

TTF ID4:							
MSB							LSB
DBit 27	DBit 26	DBit 25	DBit 24	P DBit 27-24	DBit 23	DBit 22	DBit 21

TTF ID3:							
MSB							LSB
DBit 20	P DBit 23-20	DBit 19	DBit 18	DBit 17	DBit 16	P DBit 19-16	DBit 15

TTF ID2:							
MSB							LSB
DBit 14	DBit 13	DBit 12	P DBit 15-12	DBit 11	DBit 10	DBit 9	DBit 8

TTF ID1:							
MSB							LSB
P DBit 11-8	DBit 7	DBit 6	DBit 5	DBit 4	P DBit 7-4	DBit 3	DBit 2

TTF ID0:							
MSB							LSB
DBit 1	DBit 0	P DBit 3-0	P Colum 0	P Colum 1	P Colum 2	P Colum 3	Stopbit

P Cloum 0:	DBit 31	DBit 27	DBit 23	DBit 19	DBit 15	DBit 11	DBit 7	DBit 3
P Cloum 1:	DBit 30	DBit 26	DBit 22	DBit 18	DBit 14	DBit 10	DBit 6	DBit 2
P Cloum 2:	DBit 29	DBit 25	DBit 21	DBit 17	DBit 13	DBit 9	DBit 5	DBit 1
P Cloum 3:	DBit 28	DBit 24	DBit 20	DBit 16	DBit 12	DBit 8	DBit 4	DBit 0

Fig 2. Memory organization

The memory is preprogrammed as shown in Figure 2. This data gets continuously sent back as soon as the transponder has sufficient energy.

6. Protocol timing

6.1 HITAG RO64 Transponder waiting time before transmitting data in TTF Mode

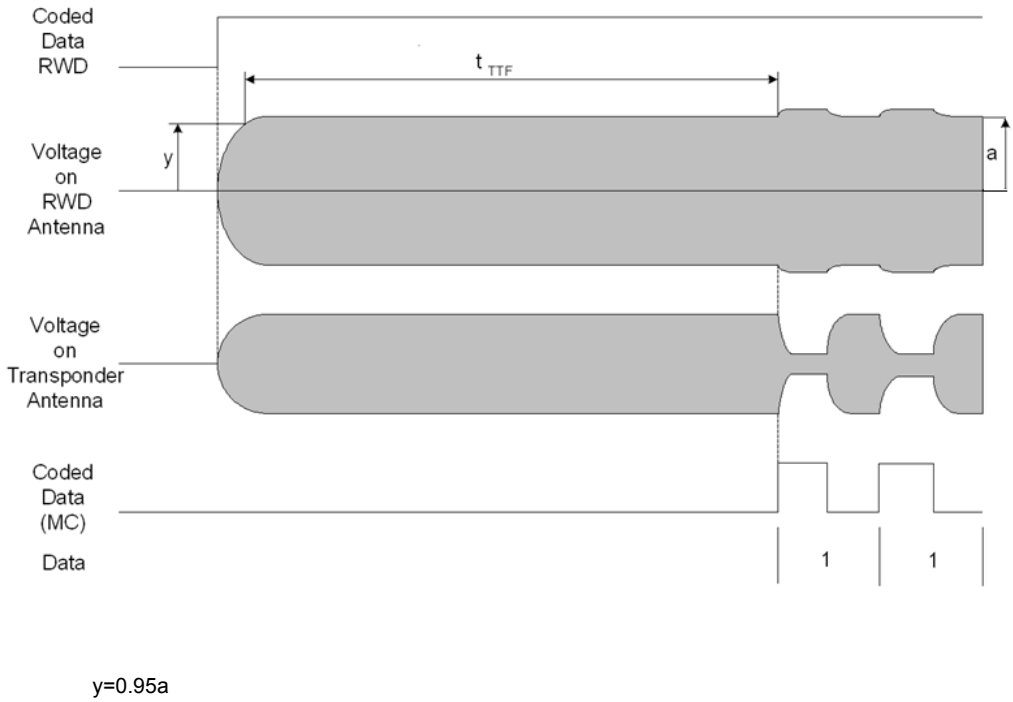


Fig 3. HITAG S Transponder waiting time before transmitting data in TTF Mode

After switching on the powering field, the HITAG RO64 Transponder waits a time t_{TTF} before transmitting data if it is configured in TTF Mode.

Table 2. HITAG RO Transponder programming time

	Min	Typ	Max	Unit
t_{TTF}	565	585	625	T_0

7. State Diagram

7.1 General Description of States

Power Off

The powering magnetic field is switched off or the HITAG RO64 Transponder is out of field.

Transponder Talks First (TTF)

The HITAG RO64 Transponder enters this State after being powered up. Entered this State, the HITAG RO64 Transponder continuously transmits the preprogrammed memory data. This data gets transmitted Manchester coded with 2kbit/s.

8. Mechanical specification

8.1 Wafer

- Diameter: 200 mm
- Thickness: 280 µm ± 15 µm
- PGDW: 25080
- PCM location: reticle area

8.2 Wafer backside

- Material: Si
- Treatment: ground and stress release
- Roughness: R_a max. 0.5 µm, R_t max. 5 µm

8.3 Chip dimensions

- Chip size: x = 1030 µm, y = 990 µm
- Scribe line: x-line: 80 µm
  y-line: 80 µm

8.4 Passivation on front

- Type: Sandwich structure
- Material: PSG / Nitride (on top)
- Thickness: 500 nm / 600 nm

8.5 Au bump

- Bump material: > 99.9 % pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 µm
- Bump height uniformity:
  - within a die: ± 2 µm
  - within a wafer: ± 3 µm
  - wafer to wafer: ± 4 µm
- Bump flatness: ± 1.5 µm
- Bump size:
  - IN1, IN2: 200 x 500 µm
  - VSS, Vdde, TestIO[1]: 60 x 60 µm
- Bump size variation: ± 5 µm
- Under bump metallization: sputtered TW

8.6 Fail die identification

All fail dies are inked according to electrical test results.

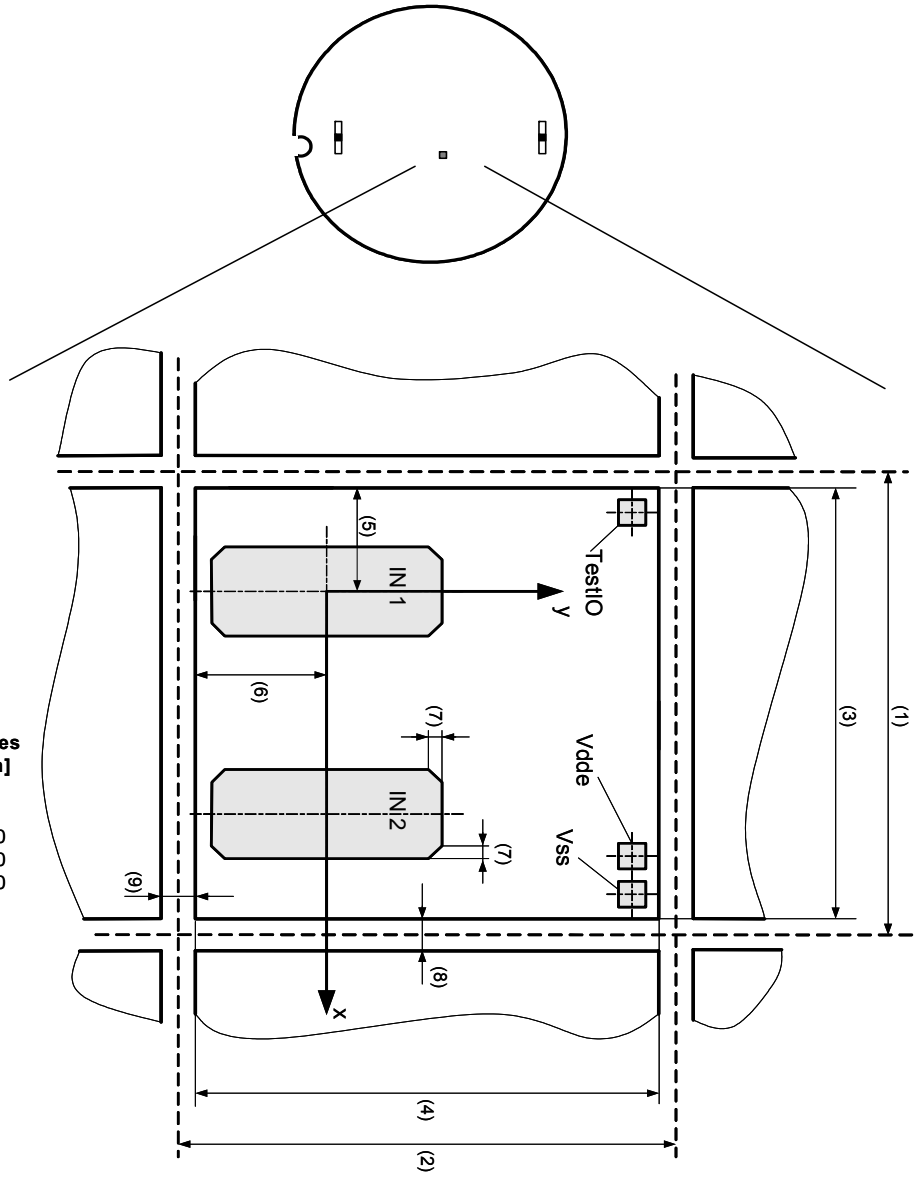
Electronic wafer mapping covers the electrical test results and additionally the results of mechanical / visual inspection.

Remark: Ink dots are not corrected after mechanical/visual inspection.

1. Pads V_{SS}, V_{dde} and TestIO are disconnected for sawn wafers

9. Chip orientation and bondpad locations

9.1 Chip orientation and bondpad locations



PAD	center coordinates x [µm]	y [µm]
IN 1	0.0	0.0
IN 2	526.0	0.0
TestIO	-170.0	689.0
Vdde	606.0	689.0
Vss	696.0	689.0

(1) Chip step on wafer, x-dimension	1070µm	IN 1/IN 2 bump size, x-dimension	200µm
(2) Chip step on wafer, y-dimension	1110µm	IN 1/IN 2 bump size, y-dimension	500µm
(3) IC size, x-dimension	990µm	TestIO/Vdde/Vss bump size, x-dimension	60µm
(4) IC size, y-dimension	1030µm	TestIO/Vdde/Vss bump size, y-dimension	60µm
(5) IN 1 bump center to IC edge, x-dimension	232µm		
(6) IN 1 bump center to IC edge, y-dimension	279µm	*TestIO/Vdde/Vss are disconnected*	
(7) IN 1/IN 2 corner bevelling	30µm		
(8) Sawline with, x-dimension	80µm		
(9) Sawline with, y-dimension	80µm		

Fig 4. Chip orientation and bondpad locations HTCICC64

10. Limiting values

10.1 Absolute maximum ratings

Table 3. Absolute maximum ratings[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{stg}	storage temperature range	-	-55	-	+140	°C
T_j	junction temperature	-	-55	-	+140	°C
V_{ESD}	ESD voltage immunity	JEDEC JESD 22-A114-B Human Body Model	-	±2	–	kV_{peak}
$I_{max\ IN1-IN2}$	maximum input peak current	-	-	±20	–	mA_{peak}

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

11. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{op}	operating temperature	-	-25	-	+85	°C
$I_{IN1-IN2}$	input current	-	-	-	±10	mA_{peak}
$V_{IN1-IN2\ rd}$	minimum operating voltage	-	-	±3.5	±4.5	V_{peak}
f_{op}	operating frequency	-	100	125	150	kHz

[1] Typical ratings are not guaranteed. These values listed are at room temperature.

12. Characteristics

Table 5. Characteristics

T_{op} = -25 to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
C_{res}	input capacitance between IN1 – IN2[2]	$V_{IN1-IN2}$ = 2 V_{rms}	199	210	221	pf
$P_{min\ rd}$	minimum operating supply power [3][4]	$V_{IN1-IN2} = V_{IN1-IN2\ rd}$	-	20	-	µW
V_{clk}	clock recovery sensitivity		-	-	100	mV_{pp}
m_{mod}	response modulation index[5]	$m_{mod} = \frac{V_{high} - V_{mod}}{V_{high} + V_{mod}}$	-	85	-	%
t_{ret}	data retention	$T_{amb} \leq 55$ °C	10	-	-	years

[1] Typical ratings are not guaranteed. These values listed are at room temperature.

[2] Measured with an HP4285A LCR meter at 125 kHz.

[3] Including losses in resonant capacitor and rectifier.

[4] Determined with: Q_{coil} = 20, L_{coil} = 7.5 mH, optimal tuned resonance circuit.

[5] Definition according to Figure 5

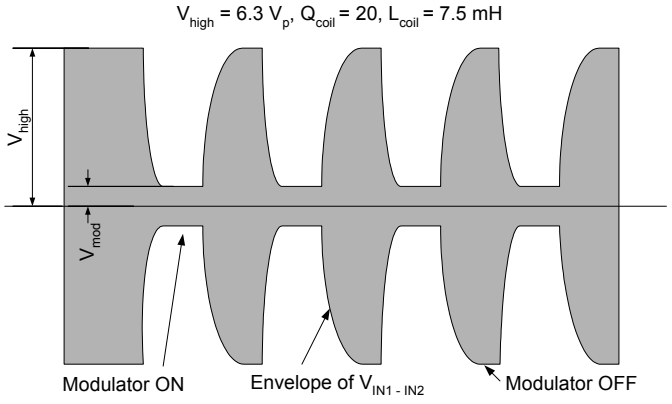


Fig 5. Response modulation index

13. Final wafertest specification

Minimum yield per wafer: 30 % of 25080 potential good dies.

14. References

[1] General quality specification

[2] General specification for 8” wafer

[3] Bumped wafer specification

[4] Application note HITAG S coil design guide

15. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
152131	20080717	Product data sheet		152130
	• Correction of the sentence “Data are stored in a non-programmable memory (EEPROM)” in Section 4 “Block diagram” on page 2			
152130	18 March 2008	Product data sheet addendum		-
	• Initial version			

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Tables

19. Figures

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