CLL3H0914L-700; CLL3H0914LS-700

L-band internally pre-matched GaN-SiC HEMT

AMPLEON

Rev. 2 — 10 January 2023 **Product data sheet**

1. Product profile

1.1 General description

The CLL3H0914L-700 and CLL3H0914LS-700 are 700 W internally pre-matched RF GaN-SiC HEMTs power transistors that are usable in the frequency range from 0.9 GHz to 1.4 GHz. The devices offer excellent efficiency, thermal resistance and ruggedness suitable for short- and long-pulse applications. Further, Section 8.3 highlights performance curves for application reference designs at frequencies from 1.2 GHz to 1.4 GHz, 1030 MHz and 960 MHz to 1215 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 3 ms; δ = 10 %; V_{DS} = 50 V; I_{Dq} = 200 mA; frequencies from 1200 MHz to 1400 MHz, tested on a straight lead device soldered in a class-AB demo circuit.

Test signal	f (MHz)	P_L [1] (W)	G_p (dB)	η_D (%)	RL_{in} (dB)
pulsed CW	1200	850	16.0	62	–12
	1300	750	16.0	71	–16
	1400	750	16.0	68	–15

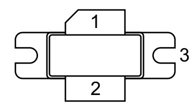
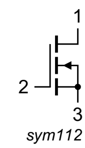
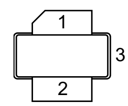
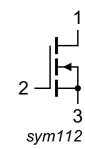
[1] $P_L = P_{L(sat)}$.

1.2 Features and benefits

- 700 W internally pre-matched GaN-SiC HEMT covering a frequency range from 0.9 GHz to 1.4 GHz with internal stability network
- Low thermal resistance
- Excellent ruggedness
- High efficiency, short pulse reference designs at 960 MHz to 1215 MHz and 1030 MHz for avionics applications
- High efficiency, long pulse reference designs at 1.2 GHz to 1.4 GHz
- Typical performance features of all three reference designs summarized in Section 8.3
- For RoHS compliance see the product details on the Ampleon website

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
CLL3H0914L-700 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
CLL3H0914LS-700 (SOT502B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT502A	CLL3H0914L-700U	9349 603 40112	Tray; 20-fold; non-dry pack	20
SOT502B	CLL3H0914LS-700U	9349 603 39112	Tray; 20-fold; non-dry pack	20

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	150	V
V_{GS}	gate-source voltage		–8	+2	V
I_{GF}	forward gate current		-	36	mA
T_{stg}	storage temperature		–65	+150	°C
T_{ch}	active die channel temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(ch-c)}$ [1]	transient thermal impedance from active die channel to case	T_{case} = 85 °C; V_{DS} = 50 V; P_{dis} = 300 W		
		t_p = 100 μs; δ = 10 %	0.12	K/W
		t_p = 200 μs; δ = 10 %	0.14	K/W
		t_p = 300 μs; δ = 10 %	0.15	K/W
		t_p = 100 μs; δ = 20 %	0.15	K/W
		t_p = 500 μs; δ = 20 %	0.19	K/W
		t_p = 2 ms; δ = 20 %	0.24	K/W
		t_p = 1 ms; δ = 10 %	0.19	K/W
		t_p = 3 ms; δ = 10 %	0.24	K/W
		steady state	0.38	K/W

[1] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

6. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = −8 V; I_D = 16 mA	150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 6 V; I_D = 1080 mA	-	−2.9	-	V
I_{DSX}	drain cut-off current	V_{GS} = 2 V; V_{DS} = 6 V	-	75	-	A
g_{fs}	forward transconductance	V_{GS} = 0 V; V_{DS} = 6 V	-	19	-	S
R_{Dson}	drain-source on-state resistance	V_{GS} = 0 V; V_{DS} = 100 mV	-	35	-	mΩ

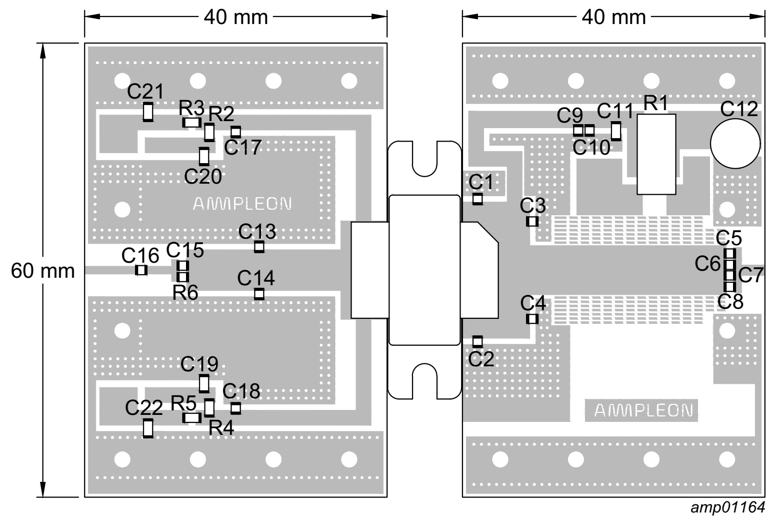
Table 7. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 500 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit, tested at frequencies from 1200 MHz to 1400 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power	$P_{L(3dB)}$	725	800	-	W
G_p	power gain	P_L = 725 W	15	17	-	dB
η_D	drain efficiency	P_L = 725 W	58	65	-	%
RL_{in}	input return loss	P_L = 725 W	-	−10	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 725 W	-	0.1	-	dB

7. Application information

7.1 Circuit information



Printed-Circuit Board (PCB): Rogers 4350B; ε_r = 3.66 F/m; height = 0.762 mm; copper top/bottom metallization; thickness copper plating = 70 μm; 1200 MHz to 1400 MHz demo board.

See Table 8 for list of components.

Fig 1. Component layout for demo board

Table 8. List of components

For test circuit see Figure 1.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	9.1 pF	ATC 100A
C3, C4	multilayer ceramic chip capacitor	5.1 pF	ATC 100A
C5, C6, C7, C8, C9, C10, C16	multilayer ceramic chip capacitor	100 pF	ATC 100A
C11	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata: GRM42256X7S475K100H530
C12	electrolytic capacitor	470 μF, 63 V	
C13, C14	multilayer ceramic chip capacitor	1.2 pF	ATC 100A
C15	multilayer ceramic chip capacitor	24 pF	ATC 100A
C17, C18	multilayer ceramic chip capacitor	72 pF	ATC 100A
C19, C20	multilayer ceramic chip capacitor	10 nF, 50 V	Murata: C1206C104K1RAC
C21, C22	multilayer ceramic chip capacitor	4.7 μF	TDK
R1	shunt resistor	10 mΩ, 5 W	
R2, R3	resistor	8.2 Ω	SMD 1206
R4, R5	resistor	4.7 Ω	SMD 1206
R6	shunt resistor	82 Ω	SMD 0603

7.2 Impedance information

Table 9. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
960	1.419 – j2.007	0.935 – j0.770
1030	1.526 – j2.099	1.053 – j0.613
1090	1.611 – j2.163	1.094 – j0.583
1150	1.638 – j2.186	1.015 – j0.588
1215	1.540 – j2.153	0.813 – j0.518
1200	1.090 – j2.359	1.337 – j0.707
1300	1.842 – j1.747	1.167 – j0.711
1400	2.215 – j1.272	0.722 – j0.604

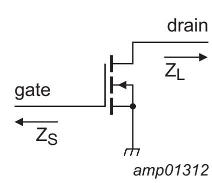


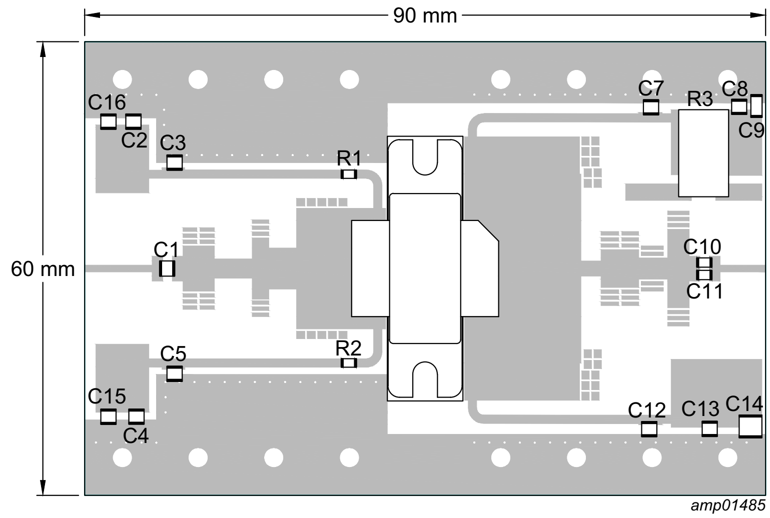
Fig 2. Definition of transistor impedance

8. Test information

8.1 Ruggedness in class-AB operation

The CLL3H0914L-700 and CLL3H0914LS-700 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; f = 1300 MHz at rated load power on RF development board using a pulsed CW RF signal.

8.2 Test circuit information



Printed-Circuit Board (PCB): Rogers 4360G2; ε_r = 6.15 F/m; height = 0.61 mm; copper plating = 35 μm.

See Table 10 for list of components.

Fig 3. Component layout for production RF test circuit

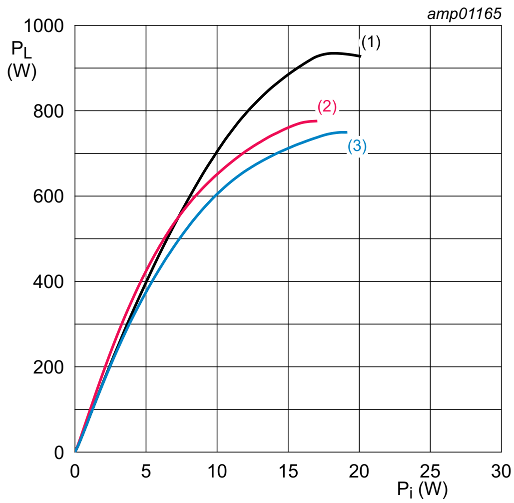
Table 10. List of components

For test circuit see Figure 3.

Component	Description	Value	Remarks
C1, C3, C5, C7, C12	multilayer ceramic chip capacitor	430 pF	ATC 800A
C10, C11	multilayer ceramic chip capacitor	160 pF	ATC 800A
C2, C4, C8, C13	multilayer ceramic chip capacitor	1 nF	ATC 800A
C9, C14, C15, C16	multilayer ceramic chip capacitor	4.7 μF, 100 V	GMR42 258K7S 475K 100 H53
R1, R2	resistor	5.6 Ω	SMD 0603
R3	resistor	10 mΩ	FC4L110R010FER

8.3 Graphical data

8.3.1 1200 MHz to 1400 MHz demo board



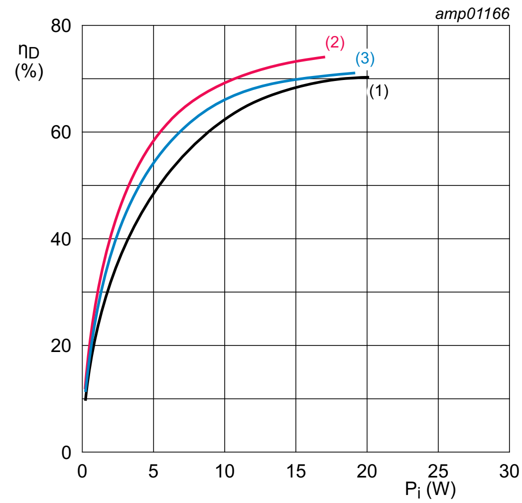
V_{DS} = 50 V; I_{Dq} = 500 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 4. Output power as a function of input power; typical values



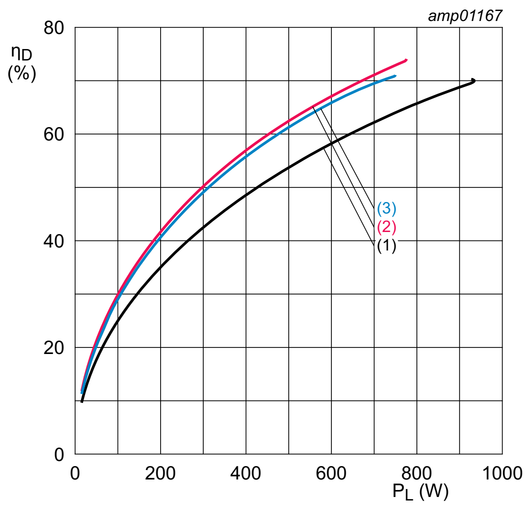
V_{DS} = 50 V; I_{Dq} = 500 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 5. Drain efficiency as a function of input power; typical values



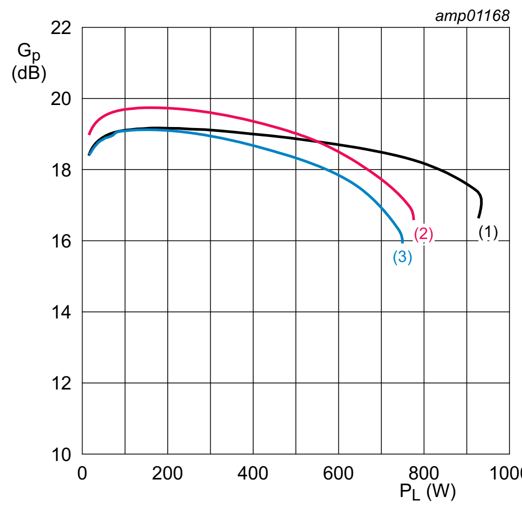
V_{DS} = 50 V; I_{Dq} = 500 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 6. Drain efficiency as a function of output power; typical values



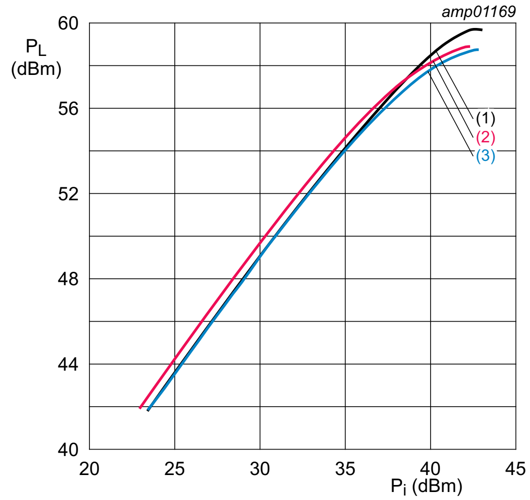
V_{DS} = 50 V; I_{Dq} = 500 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 7. Power gain as a function of output power; typical values



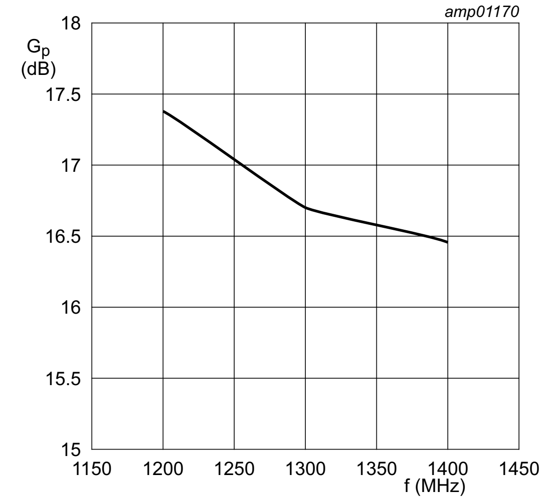
V_{DS} = 50 V; I_{Dq} = 500 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

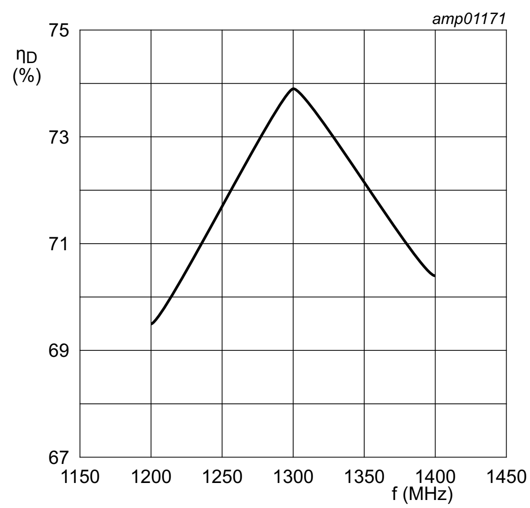
(3) f = 1400 MHz

Fig 8. Output power as a function of input power; typical values



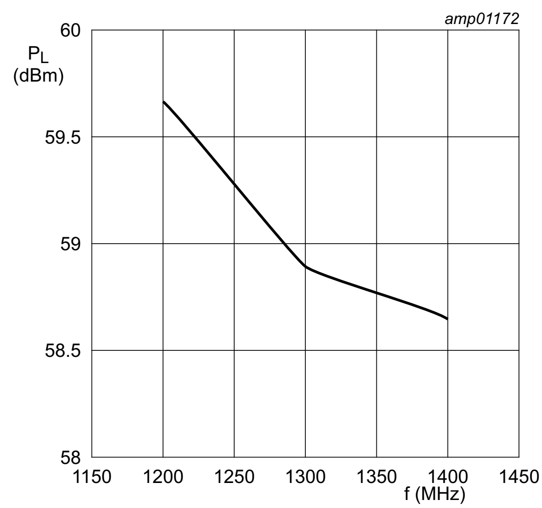
V_{DS} = 50 V; I_{Dq} = 500 mA; P_i = 42.3 dBm; t_p = 100 μs; δ = 10 %.

Fig 9. Power gain as a function of frequency; typical values



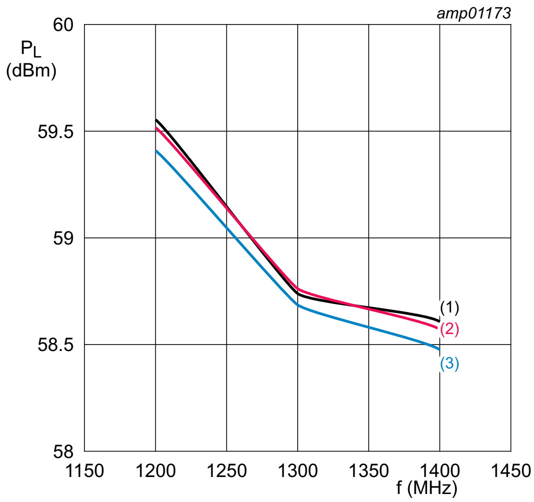
V_{DS} = 50 V; I_{Dq} = 500 mA; P_i = 42.3 dBm; t_p = 100 μs; δ = 10 %.

Fig 10. Drain efficiency as a function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 500 mA; P_i = 42.3 dBm; t_p = 100 μs; δ = 10 %.

Fig 11. Output power as a function of frequency; typical values



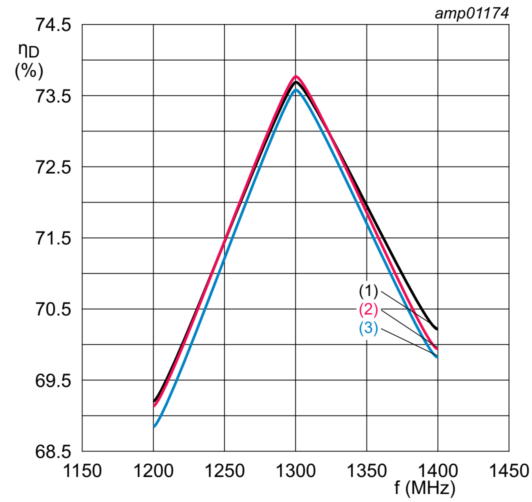
V_{DS} = 50 V; I_{Dq} = 500 mA; P_i = 42.5 dBm; δ = 20 %.

(1) t_p = 500 μs

(2) t_p = 1 ms

(3) t_p = 2 ms

Fig 12. Output power as a function of frequency, typical values



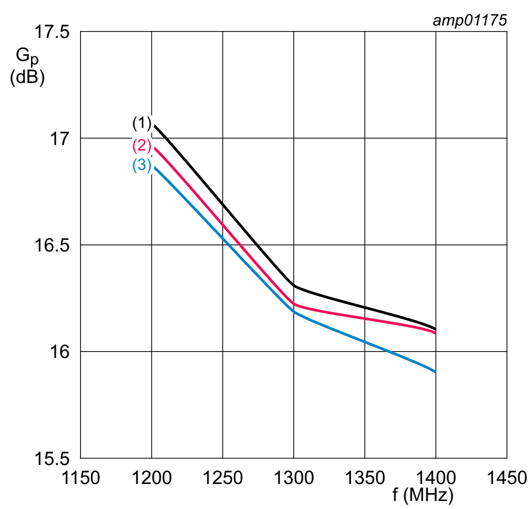
V_{DS} = 50 V; I_{Dq} = 500 mA; P_i = 42.5 dBm; δ = 20 %.

(1) t_p = 500 μs

(2) t_p = 1 ms

(3) t_p = 2 ms

Fig 13. Drain efficiency as a function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 500 mA; P_i = 42.5 dBm; δ = 20 %.

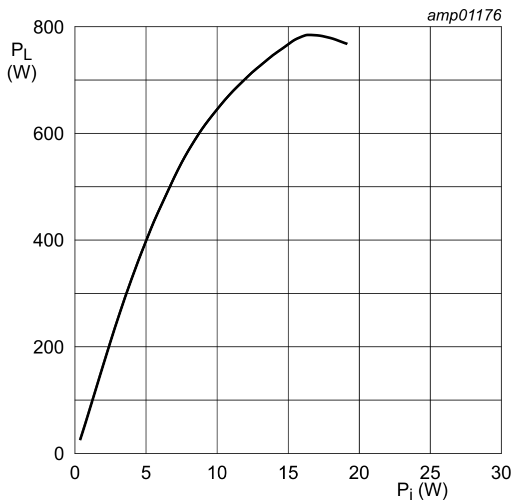
(1) t_p = 500 μs

(2) t_p = 1 ms

(3) t_p = 2 ms

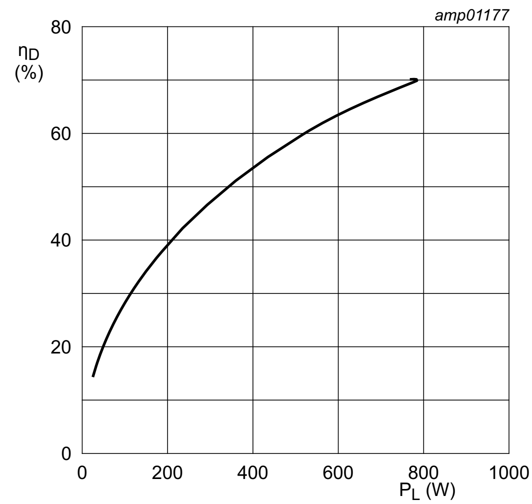
Fig 14. Power gain as a function of frequency, typical values

8.3.2 1030 MHz demo board



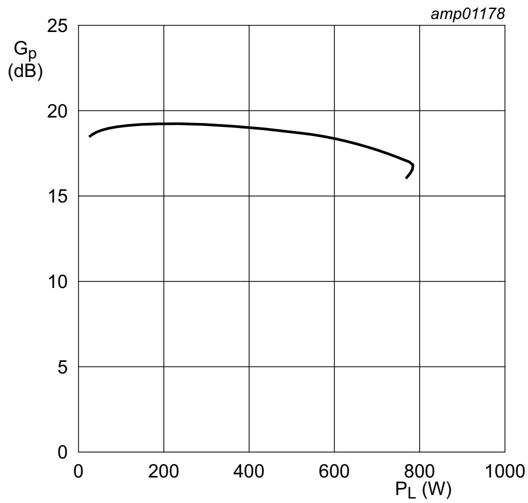
f = 1030 MHz; V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 128 μs; δ = 1 %.

Fig 15. Output power as a function of input power; typical values



f = 1030 MHz; V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 128 μs; δ = 1 %.

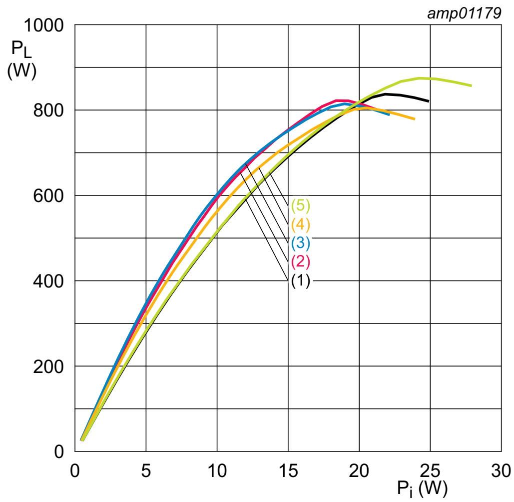
Fig 16. Drain efficiency as a function of output power; typical values



f = 1030 MHz; V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 128 μs; δ = 1 %.

Fig 17. Power gain as a function of output power; typical values

8.3.3 960 MHz to 1215 MHz demo board



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz

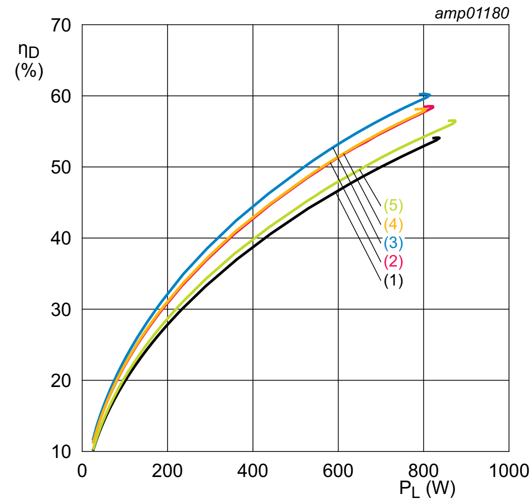
(2) f = 1030 MHz

(3) f = 1090 MHz

(4) f = 1150 MHz

(5) f = 1215 MHz

Fig 18. Output power as a function of input power; typical values



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz

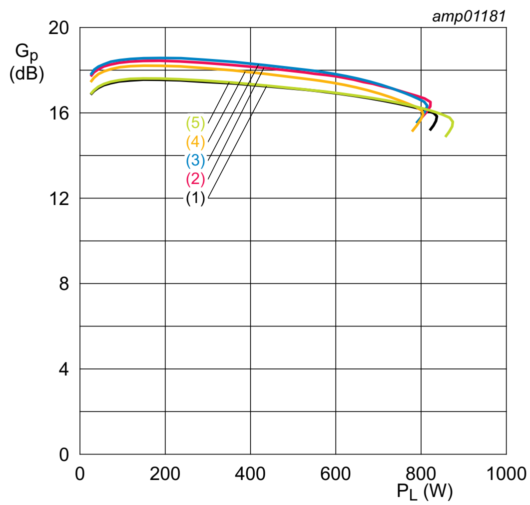
(2) f = 1030 MHz

(3) f = 1090 MHz

(4) f = 1150 MHz

(5) f = 1215 MHz

Fig 19. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz

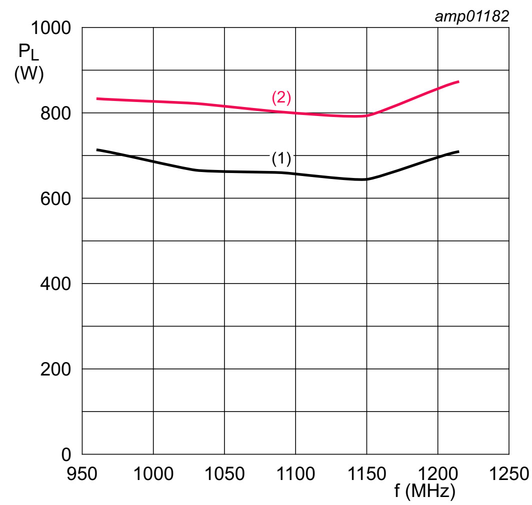
(2) f = 1030 MHz

(3) f = 1090 MHz

(4) f = 1150 MHz

(5) f = 1215 MHz

Fig 20. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 100 μs; δ = 10 %.

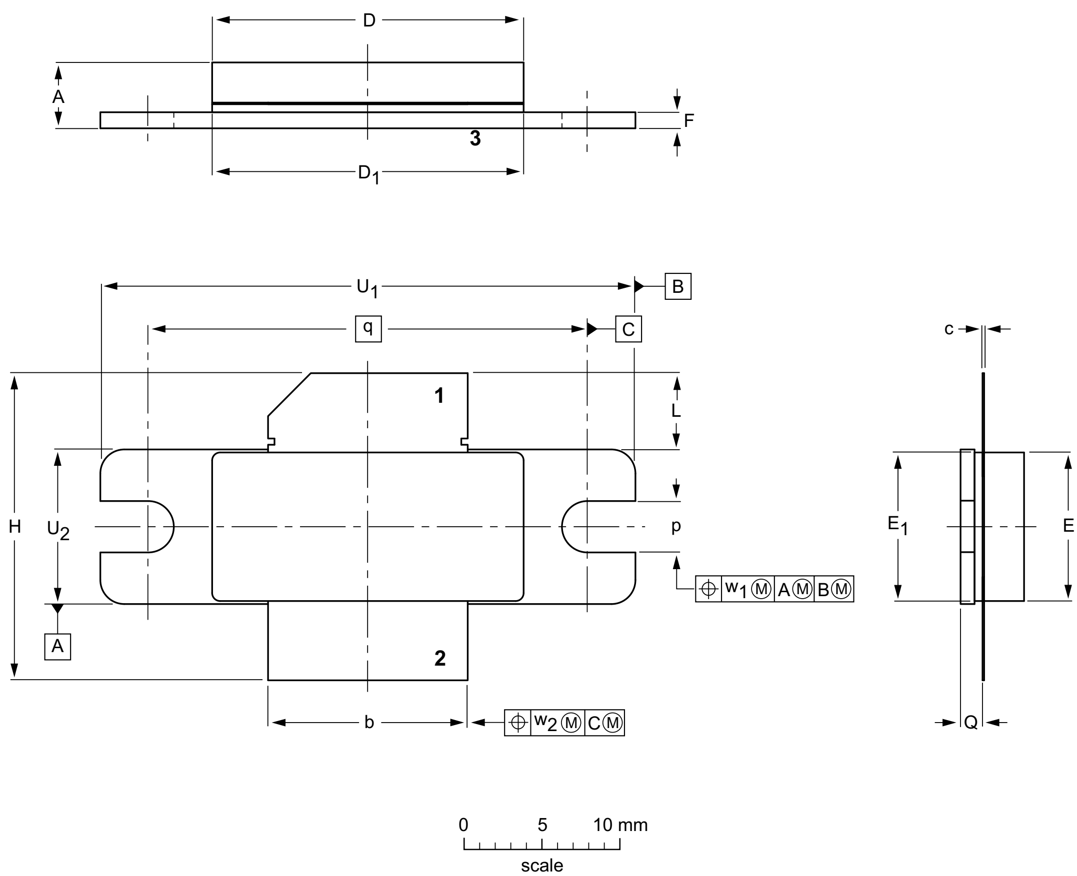
(1) $P_{L(1dB)}$

(2) $P_{L(2dB)}$

Fig 21. Output power as a function of frequency; typical values

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



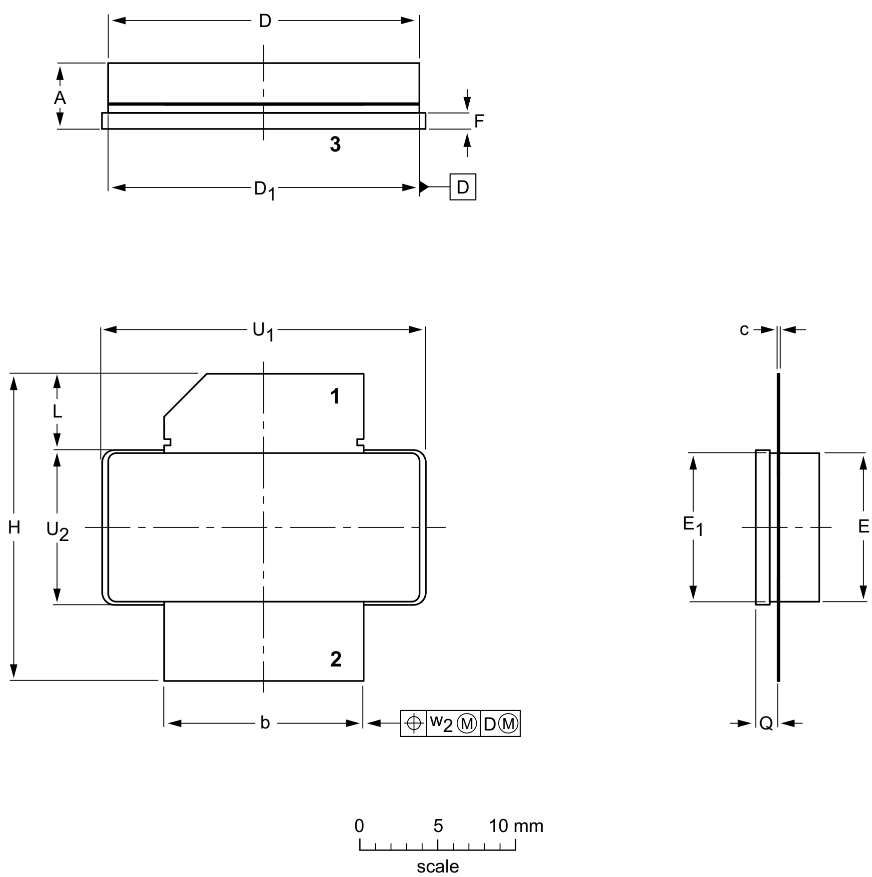
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~12-05-02~~ 21-07-22

Fig 22. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~12-05-02~~ 21-07-22

Fig 23. Package outline SOT502B

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
L-band	Long wave band
MTF	Median Time to Failure
SiC	Silicon Carbide
SMD	Surface Mounted Device
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CLL3H0914L-700_0914LS-700 v.2	20230110	Product data sheet	-	CLL3H0914L-700_ 0914LS-700 v.1
Modifications:	• Table 5 on page 3: table updated			
CLL3H0914L-700_0914LS-700 v.1	20220715	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contact information

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For sales office addresses, please visit: **http://www.ampleon.com/sales**

15. Contents

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