PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 Qualified
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
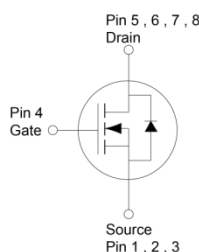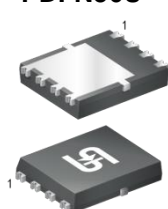- RoHS Compliant
- Halogen-Free

APPLICATIONS

- Automotive Applications
- Solenoid and Motor Drivers
- DC-DC Converters

PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		40	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	5.6	mΩ
	V_{GS} = 7V	6.7	
Q_g	V_{GS} = 10V	27.3	nC

PDFN56U

Pin 5 , 6 , 7 , 8
Drain

Pin 4
Gate

Source
Pin 1 , 2 , 3

Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, Silicon limited	T_C = 25°C	I_D	90	A
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	54	A
	T_C = 100°C		54	
	T_A = 25°C		17	
Pulsed Drain Current		I_{DM}	216	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	21.6	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	69.8	mJ
Total Power Dissipation	T_C = 25°C	P_D	78.9	W
	T_C = 125°C		26.3	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	1.9	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	50	°C/W

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	$V_{GS(TH)}$	2.4	3	3.6	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 40V	I_{DSS}	--	--	1	µA
	V_{GS} = 0V, V_{DS} = 40V T_J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 27A	$R_{DS(on)}$	--	4.3	5.6	mΩ
	V_{GS} = 7V, I_D = 27A		--	5	6.7	
Forward Transconductance (Note 3)	V_{DS} = 10V, I_D = 7A	g_{fs}	--	105	--	S
Dynamic						
Total Gate Charge	V_{GS} = 7V, V_{DS} = 20V, I_D = 17A	Q_g	--	19.4	29.1	nC
Total Gate Charge	V_{GS} = 10V, V_{DS} = 20V, I_D = 17A	Q_g	--	27.3	41	
Gate-Source Charge		Q_{gs}	--	8.4	16.8	
Gate-Drain Charge		Q_{gd}	--	4.8	9.6	
Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	C_{iss}	--	1941	2912	pF
Output Capacitance		C_{oss}	--	348	696	
Reverse Transfer Capacitance		C_{rss}	--	42	84	
Gate Resistance	f = 1.0MHz	R_g	--	1.5	--	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 20V, I_D = 17A, R_G = 1.5Ω	$t_{d(on)}$	--	10.1	--	ns
Rise Time		t_r	--	55.7	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20.3	--	
Fall Time		t_f	--	5.7	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 27A	V_{SD}	--	--	1.1	V
Reverse Recovery Time	I_S = 17A, di/dt = 100A/µs	t_{rr}	--	32	--	ns
Reverse Recovery Charge		Q_{rr}	--	22	--	nC

Notes:

1. Package current limit.
2. L = 0.3mH, V_{GS} = 10V, R_G = 25Ω, Starting T_J = 25°C.
3. Pulse test: Pulse Width ≤ 300µs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM056NH04CR RLG	PDFN56U	2,500pcs / 13" Reel
TQM056NH04CR-V RLG	PDFN56U	2,500pcs / 13" Reel

Notes:
V : HOT test

TAIWAN SEMICONDUCTOR
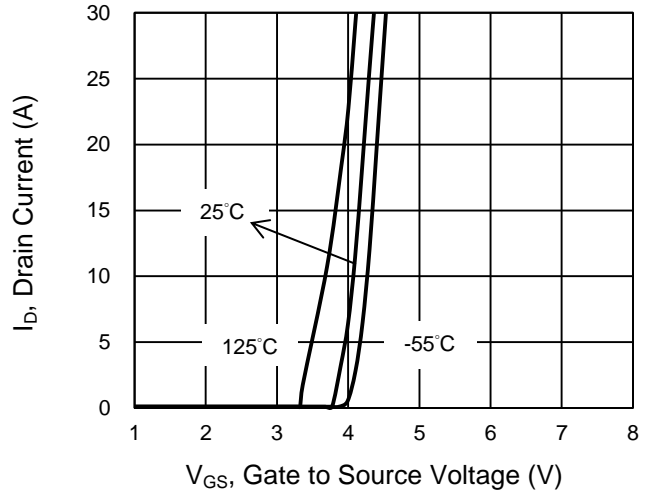
CHARACTERISTICS CURVES
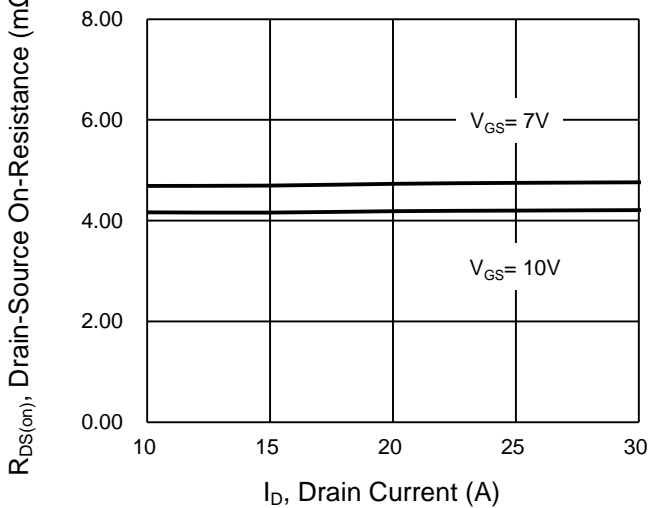
(T_A = 25°C unless otherwise noted)
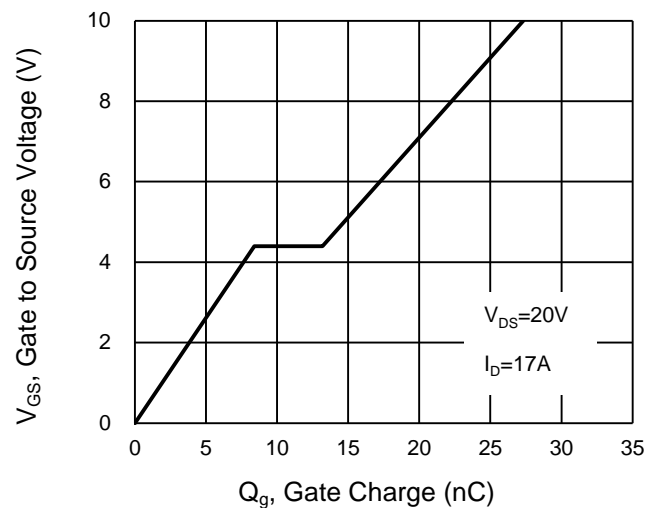
Output Characteristics
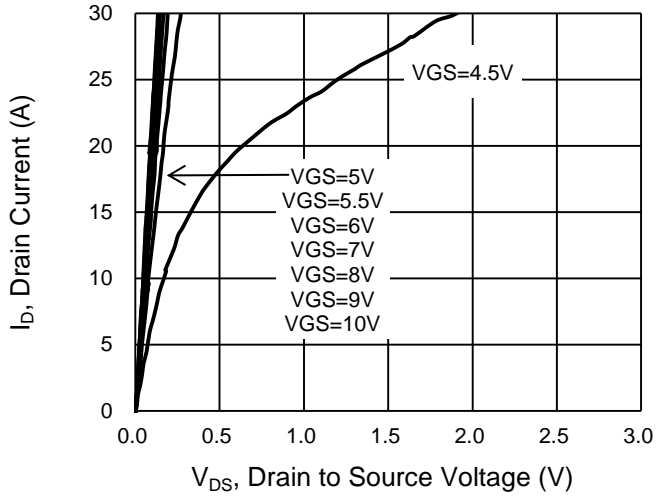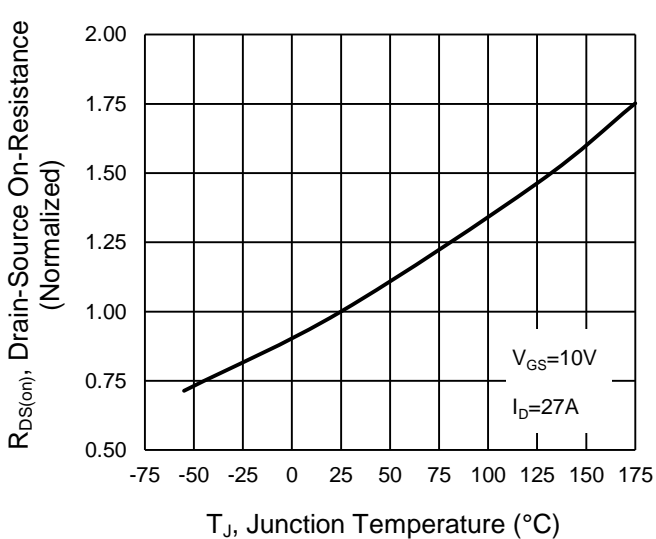

Transfer Characteristics

On-Resistance vs. Drain Current

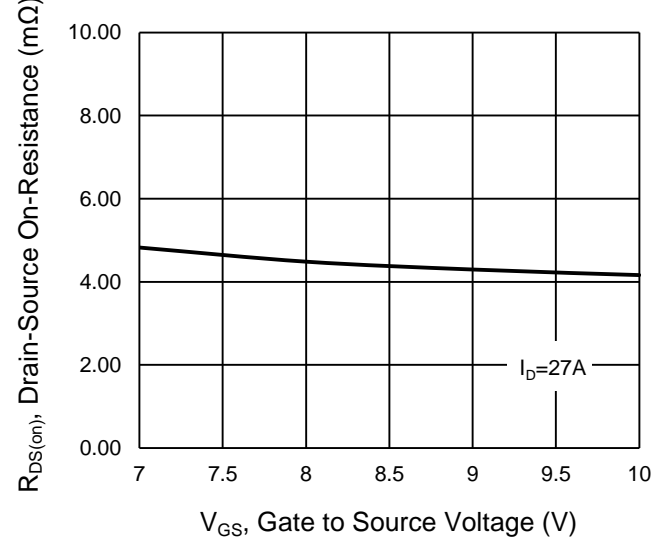**Gate-Source Voltage vs. Gate Charge**
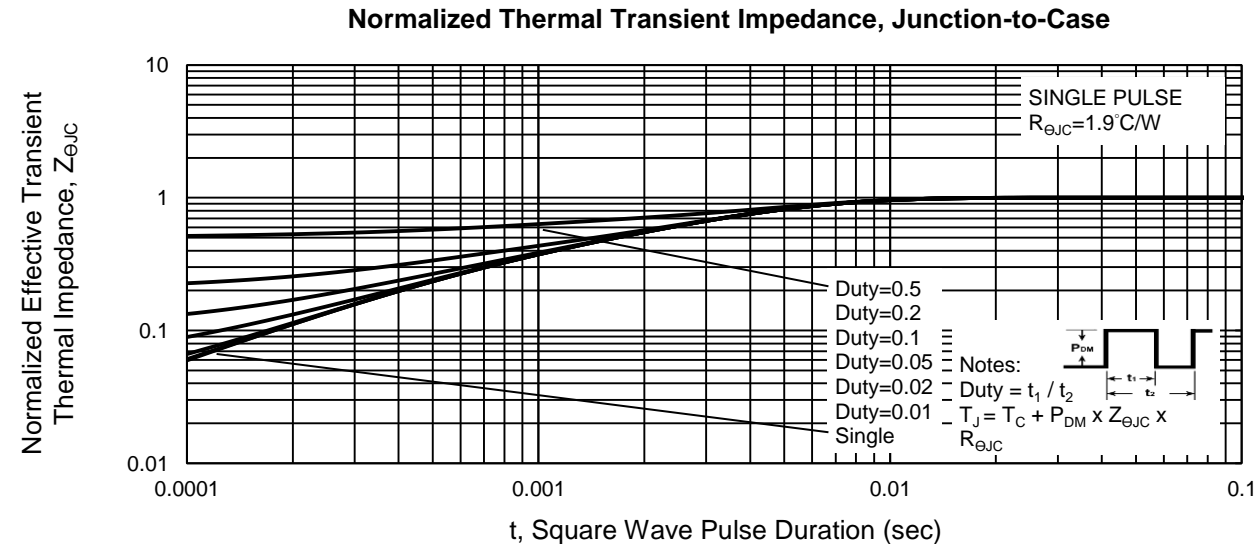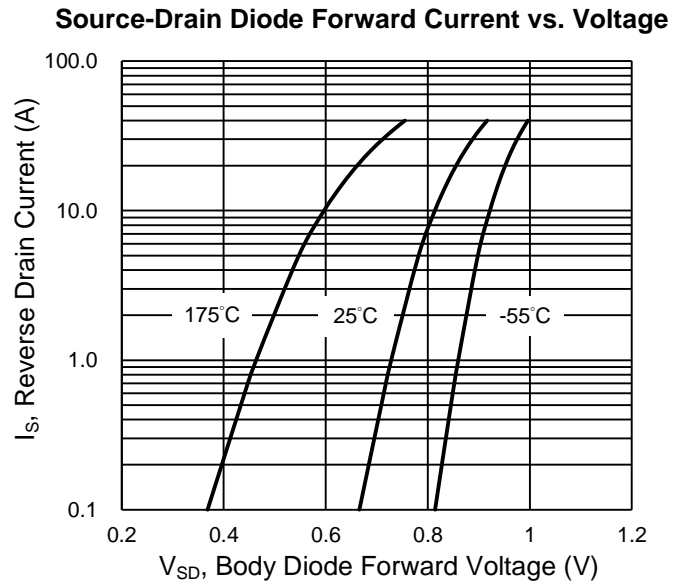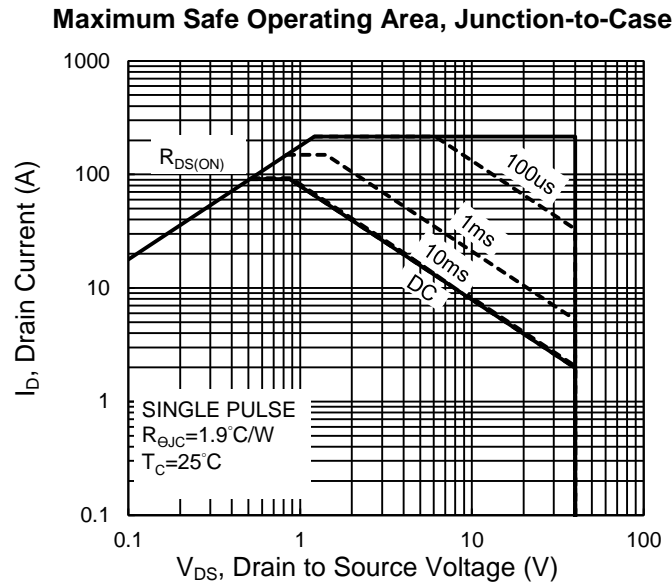

On-Resistance vs. Junction Temperature

On-Resistance vs. Gate-Source Voltage

Version: A2301

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Capacitance vs. Drain-Source Voltage

BV$_{DSS}$ vs. Junction Temperature

Maximum Safe Operating Area, Junction-to-Case

Source-Drain Diode Forward Current vs. Voltage

Normalized Thermal Transient Impedance, Junction-to-Case

Version: A2301

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Power Dissipation

(graph: P_{TOT} – Power (W) vs Junction-to-Case Temperature (°C))

Drain Current
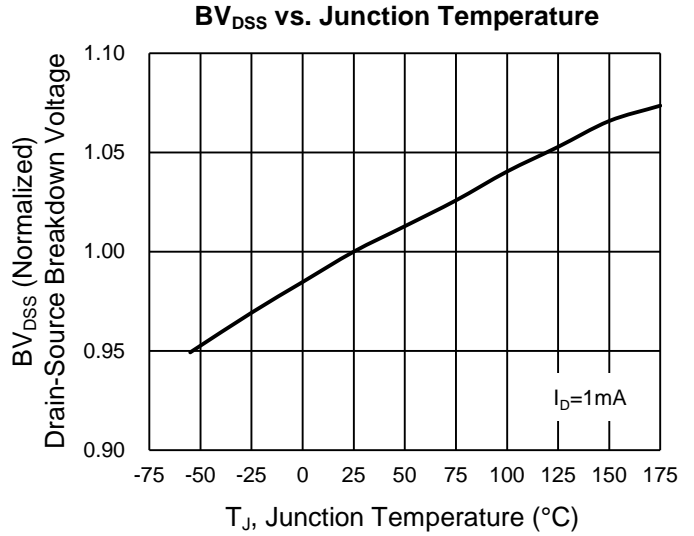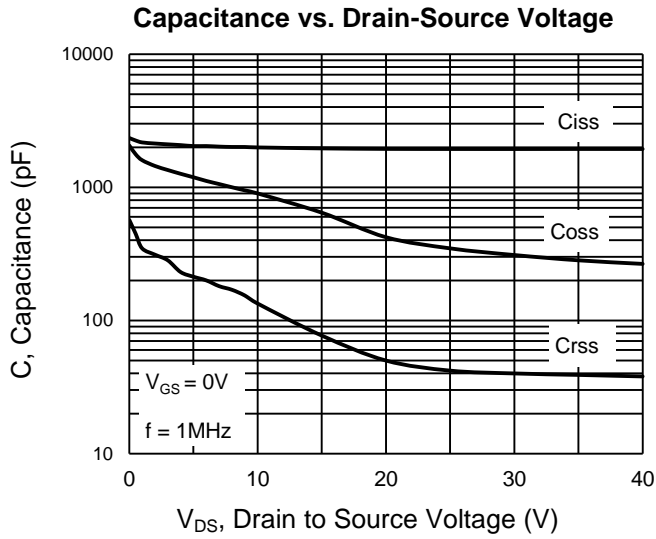
(graph: I_D, Drain Current (A) vs Junction-to-Case Temperature (°C); Silicon limited, V_{GS}=10V, Package limited)

Normalized gate threshold voltage vs Temperature

(graph: Threshold Voltage (Normalized) vs T_J, Junction Temperature (°C); I_D=250µA)
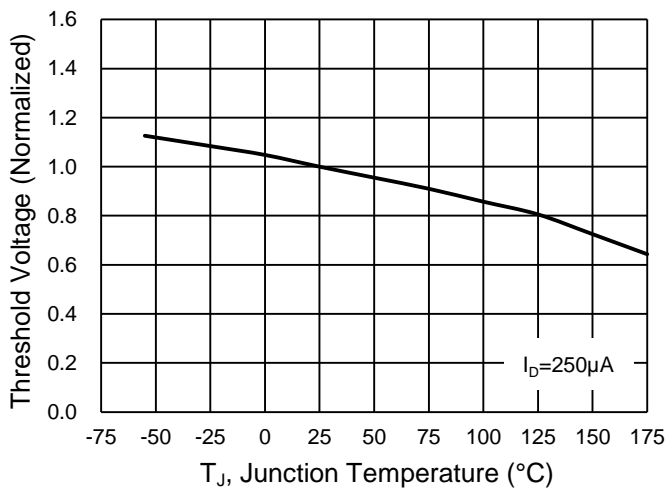
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U

SEE DETAIL A

0.05 C

5.30
4.80

0.90MIN

1.10
0.90

0.05 C

0.30
0.20

0.05
0.00

SEATING PLANE

DETAIL A
(SCALE 2:1)

4.56

3.80
4.60   3.50   3.91
0.92

6.80

1.27

1.27   0.75

3.81

SUGGESTED PAD LAYOUT

8   5

TSC
056NH04
YWWLF

DOT
MARKING,
PIN #1 ID   1   4

MARKING DIAGRAM

P/N	=	MARKING CODE
Y	=	YEAR CODE
WW	=	WEEK CODE (01~52)
L	=	LOT CODE (1~9, A~Z)
F	=	FACTORY CODE
_	=	AEC-Q101 QUALIFIED
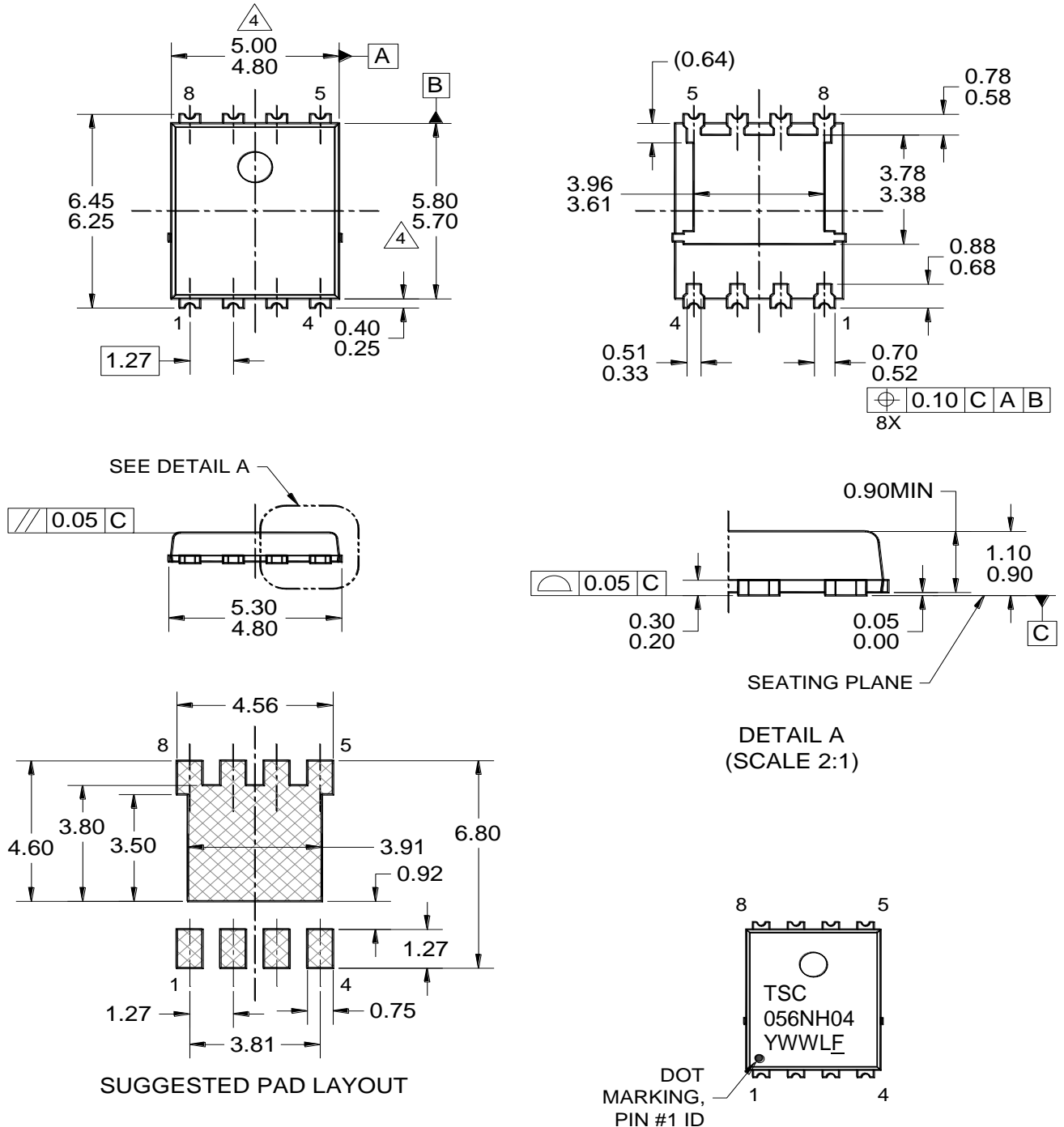
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV A.

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Version: A2301