

# Schmitt Trigger Buffer, Dual, Non-Inverting

## NL27WZ17

The NL27WZ17 is a high performance dual buffer with Schmitt-Trigger inputs operating from a 1.65 to 5.5 V supply.

### Features

- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 3.7 ns  $t_{PD}$  at  $V_{CC} = 5$  V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- $I_{OFF}$  Supports Partial Power Down Protection
- Sink 32 mA at 4.5 V
- Available in SC-88, SC-74, and UDFN6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

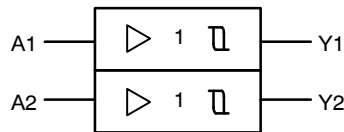

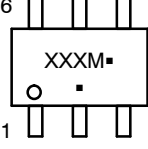

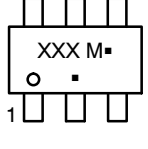






Figure 1. Logic Symbol



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

MARKING DIAGRAMS		
	SC-88 DF SUFFIX CASE 419B-02	
	SC-74 CASE 318F-05	
	UDFN6 1.45x1.0, 0.5P CASE 517AQ	
	UDFN6 1x1, 0.35P CASE 517BX	

X, XXX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# NL27WZ17

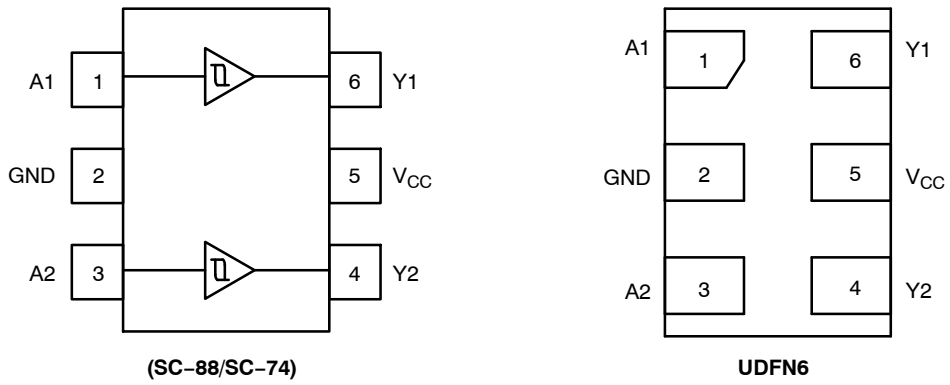


Figure 2. Pinout (Top View)

## PIN ASSIGNMENT

Pin	Function
1	A1
2	GND
3	A2
4	Y2
5	V <sub>CC</sub>
6	Y1

## FUNCTION TABLE

A Input	Y Output
L	L
H	H

# NL27WZ17

## MAXIMUM RATINGS

Symbol	Characteristics	Value	Units
V <sub>CC</sub>	DC Supply Voltage SC-88 (NLV) SC-88, SC-74, UDFN6	-0.5 to +7.0 -0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage SC-88 (NLV) SC-88, SC-74, UDFN6	-0.5 to +7.0 -0.5 to +6.5	V
V <sub>OUT</sub>	DC Output Voltage SC-88 (NLV) Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V <sub>CC</sub> = 0 V)	-0.5 to V <sub>CC</sub> +0.5 -0.5 to +7.0 -0.5 to +7.0	V
	DC Output Voltage SC-88, SC-74, UDFN6 Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V <sub>CC</sub> = 0 V)	-0.5 to V <sub>CC</sub> +0.5 -0.5 to +6.5 -0.5 to +6.5	V
I <sub>IK</sub>	DC Input Diode Current, V <sub>IN</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current, V <sub>OUT</sub> < GND	-50	mA
I <sub>OUT</sub>	DC Output Source/Sink Current	±50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T <sub>J</sub>	Junction Temperature under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2) SC-88 SC-74 UDFN6	377 320 154	°C/W
P <sub>D</sub>	Power Dissipation in Still Air SC-88 SC-74 UDFN6	332 390 812	mW
MSL	Moisture Sensitivity	Level 1	-
F <sub>R</sub>	Flameability Rating Oxygen Index: 28 to 34	UL 94-V-0 @ 0.125 in	-
V <sub>ESD</sub>	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model (NLV) Charged Device Model	2000 1000 N/A	V
I <sub>LATCHUP</sub>	Latchup Performance (Note 4) (NLV)	±100 ±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage	1.65	5.5	V
V <sub>IN</sub>	DC Input Voltage	0	5.5	V
V <sub>OUT</sub>	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V <sub>CC</sub> = 0 V)	0	V <sub>CC</sub>	V
		0	5.5	
		0	5.5	
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Transition Rise or Fall Rate V <sub>CC</sub> = 1.65 V to 1.95 V V <sub>CC</sub> = 2.3 V to 2.7 V V <sub>CC</sub> = 3.0 V to 3.6 V V <sub>CC</sub> = 4.5 V to 5.5 V	0 0 0 0	No Limit No Limit No Limit No Limit	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NL27WZ17

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	Positive Input Threshold Voltage		1.65	-	1.0	1.4	-	1.4	-	1.4	V
			2.3	-	1.5	1.8	-	1.8	-	1.8	
			2.7	-	1.7	2	-	2	-	2	
			3	-	1.9	2.2	-	2.2	-	2.2	
			4.5	-	2.7	3.1	-	3.1	-	3.1	
			5.5	-	3.3	3.6	-	3.6	-	3.6	
V <sub>T-</sub>	Negative Input Threshold Voltage		1.65	0.2	0.5	-	0.2	-	0.2	-	V
			2.3	0.4	0.75	-	0.4	-	0.4	-	
			2.7	0.5	0.87	-	0.5	-	0.5	-	
			3	0.6	1.0	-	0.6	-	0.6	-	
			4.5	1.0	1.5	-	1.0	-	1.0	-	
			5.5	1.2	1.9	-	1.2	-	1.2	-	
V <sub>H</sub>	Input Hysteresis Voltage		1.65	0.1	0.48	0.9	0.1	0.9	0.1	0.9	V
			2.3	0.25	0.75	1.1	0.25	1.1	0.25	1.1	
			2.7	0.3	0.83	1.15	0.3	1.15	0.3	1.15	
			3	0.4	0.93	1.2	0.4	1.2	0.4	1.2	
			4.5	0.6	1.2	1.5	0.6	1.5	0.6	1.5	
			5.5	0.7	1.4	1.7	0.7	1.7	0.7	1.7	
V <sub>OH</sub>	High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.1	-	V <sub>CC</sub> - 0.1	-	V
		I <sub>OH</sub> = -4 mA	1.65	1.29	1.52	-	1.29	-	1.29	-	
		I <sub>OH</sub> = -8 mA	2.3	1.9	2.1	-	1.9	-	1.9	-	
		I <sub>OH</sub> = -12 mA	2.7	2.2	2.4	-	2.2	-	2.2	-	
		I <sub>OH</sub> = -16 mA	3	2.4	2.7	-	2.4	-	2.4	-	
		I <sub>OH</sub> = -24 mA	3	2.3	2.5	-	2.3	-	2.3	-	
		I <sub>OH</sub> = -32 mA	4.5	3.8	4	-	3.8	-	3.8	-	
V <sub>OL</sub>	Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.65 to 5.5	-	-	0.1	-	0.1	-	0.1	V
		I <sub>OL</sub> = 4 mA	1.65	-	0.08	0.24	-	0.24	-	0.24	
		I <sub>OL</sub> = 8 mA	2.3	-	0.2	0.3	-	0.3	-	0.3	
		I <sub>OL</sub> = 12 mA	2.7	-	0.22	0.4	-	0.4	-	0.4	
		I <sub>OL</sub> = 16 mA	3	-	0.28	0.4	-	0.4	-	0.4	
		I <sub>OL</sub> = 24 mA	3	-	0.38	0.55	-	0.55	-	0.55	
		I <sub>OL</sub> = 32 mA	4.5	-	0.42	0.55	-	0.55	-	0.55	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	1.65 to 5.5	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V	0	-	-	1	-	10	-	10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = 5.5 V or GND	5.5	-	-	1	-	10	-	10	μA

# NL27WZ17

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, A to Y (Figures 3 and 4)	R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 15 pF	1.65 to 1.95	-	9.1	15	-	15.6	-	15.6	ns
			2.3 to 2.7	-	5.0	9.0	-	9.5	-	9.5	
		R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 15 pF	3.0 to 3.6	-	3.7	6.3	-	6.5	-	6.5	
			4.5 to 5.5	-	3.1	5.2	-	5.5	-	5.5	
			R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 50 pF	3.0 to 3.6	-	4.4	7.2	-	7.5	-	
		4.5 to 5.5		-	3.7	5.9	-	6.2	-	6.2	

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	2.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	4.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub> 10 MHz, V <sub>CC</sub> = 5.0 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	11 12.5	pF

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} \cdot I_{CC}$ . C<sub>PD</sub> is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} \cdot I_{CC} \cdot V_{CC}$ .

# NL27WZ17



$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1$  MHz

**Figure 3. Test Circuit**

Test	Switch Position	$C_L$ , pF	$R_L$ , $\Omega$	$R_1$ , $\Omega$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table		
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$	-	-	-
		See AC Characteristics Table		
$t_{PHZ} / t_{PZH}$	GND	-	-	-
		See AC Characteristics Table		

X = Don't Care



**Figure 4. Switching Waveforms**

$V_{CC}$ , V	$V_{mi}$ , V	$V_{mo}$ , V		$V_Y$ , V
		$t_{PLH}$ , $t_{PHL}$	$t_{PZL}$ , $t_{PLZ}$ , $t_{PZH}$ , $t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

# NL27WZ17

## ORDERING INFORMATION

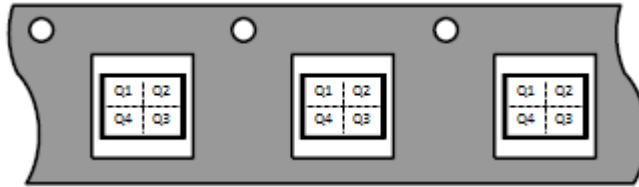
Device	Package	Specific Device Code	Pin1 Orientation (See below)	Shipping <sup>†</sup>
NL27WZ17DFT2G	SC-88	MX	Q4	3000 / Tape & Reel
NLV27WZ17DFT2G*	SC-88	MX	Q4	3000 / Tape & Reel
NL27WZ17DBVT1G	SC-74	AC	Q4	3000 / Tape & Reel
NL27WZ17MU1TCG	UDFN6 1.45 x 1.0, 0.5P	K (Rotated 90° CW)	Q4	3000 / Tape & Reel
NL27WZ17MU3TCG	UDFN6 1.0 x 1.0, 0.35P	D	Q4	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel

Direction of Feed



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



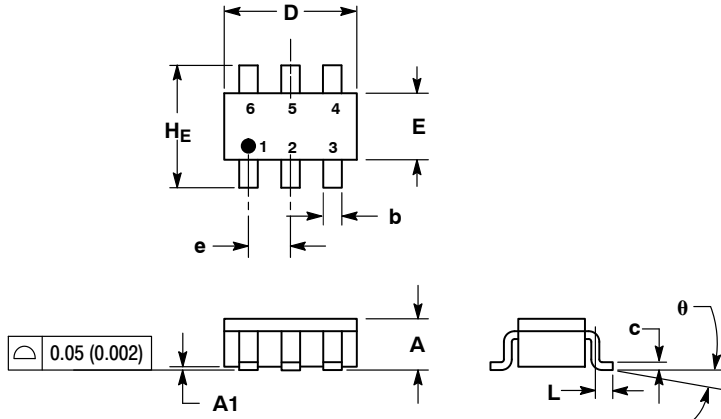
### SC-74

#### CASE 318F-05

#### ISSUE N

DATE 08 JUN 2012

SCALE 2:1

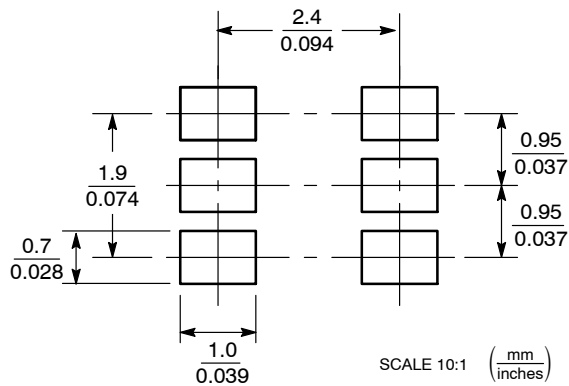


**NOTES:**

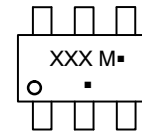
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

#### SOLDERING FOOTPRINT\*



#### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- |  |   |  |   |  |  |
|--|---|--|---|--|--|
| <p><b>STYLE 1:</b></p> <p>PIN 1. CATHODE</p> <p>PIN 2. ANODE</p> <p>PIN 3. CATHODE</p> <p>PIN 4. CATHODE</p> <p>PIN 5. ANODE</p> <p>PIN 6. CATHODE</p>     | <p><b>STYLE 2:</b></p> <p>PIN 1. NO CONNECTION</p> <p>PIN 2. COLLECTOR</p> <p>PIN 3. EMITTER</p> <p>PIN 4. NO CONNECTION</p> <p>PIN 5. COLLECTOR</p> <p>PIN 6. BASE</p> | <p><b>STYLE 3:</b></p> <p>PIN 1. EMITTER 1</p> <p>PIN 2. BASE 1</p> <p>PIN 3. COLLECTOR 2</p> <p>PIN 4. EMITTER 2</p> <p>PIN 5. BASE 2</p> <p>PIN 6. COLLECTOR 1</p> | <p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR 2</p> <p>PIN 2. EMITTER 1/EMITTER 2</p> <p>PIN 3. COLLECTOR 1</p> <p>PIN 4. EMITTER 3</p> <p>PIN 5. BASE 1/BASE 2/COLLECTOR 3</p> <p>PIN 6. BASE 3</p> | <p><b>STYLE 5:</b></p> <p>PIN 1. CHANNEL 1</p> <p>PIN 2. ANODE</p> <p>PIN 3. CHANNEL 2</p> <p>PIN 4. CHANNEL 3</p> <p>PIN 5. CATHODE</p> <p>PIN 6. CHANNEL 4</p> | <p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE</p> <p>PIN 2. ANODE</p> <p>PIN 3. CATHODE</p> <p>PIN 4. CATHODE</p> <p>PIN 5. CATHODE</p> <p>PIN 6. CATHODE</p> |
| <p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE 1</p> <p>PIN 2. GATE 1</p> <p>PIN 3. DRAIN 2</p> <p>PIN 4. SOURCE 2</p> <p>PIN 5. GATE 2</p> <p>PIN 6. DRAIN 1</p> | <p><b>STYLE 8:</b></p> <p>PIN 1. EMITTER 1</p> <p>PIN 2. BASE 2</p> <p>PIN 3. COLLECTOR 2</p> <p>PIN 4. EMITTER 2</p> <p>PIN 5. BASE 1</p> <p>PIN 6. COLLECTOR 1</p>    | <p><b>STYLE 9:</b></p> <p>PIN 1. EMITTER 2</p> <p>PIN 2. BASE 2</p> <p>PIN 3. COLLECTOR 1</p> <p>PIN 4. EMITTER 1</p> <p>PIN 5. BASE 1</p> <p>PIN 6. COLLECTOR 2</p> | <p><b>STYLE 10:</b></p> <p>PIN 1. ANODE/CATHODE</p> <p>PIN 2. BASE</p> <p>PIN 3. EMITTER</p> <p>PIN 4. COLLECTOR</p> <p>PIN 5. ANODE</p> <p>PIN 6. CATHODE</p>                                    | <p><b>STYLE 11:</b></p> <p>PIN 1. EMITTER</p> <p>PIN 2. BASE</p> <p>PIN 3. ANODE/CATHODE</p> <p>PIN 4. ANODE</p> <p>PIN 5. CATHODE</p> <p>PIN 6. COLLECTOR</p>   |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42973B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-74</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.





1  
 SCALE 2:1

SC-88/SC70-6/SOT-363  
 CASE 419B-02  
 ISSUE Y

DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

**GENERIC MARKING DIAGRAM\***



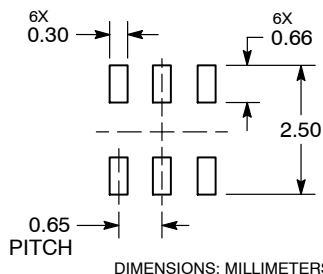
XXX = Specific Device Code  
 M = Date Code\*  
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

<b>DOCUMENT NUMBER:</b>	<b>98ASB42985B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88/SC70-6/SOT-363</b>	<b>PAGE 1 OF 2</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SC-88/SC70-6/SOT-363**  
**CASE 419B-02**  
**ISSUE Y**

DATE 11 DEC 2012

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

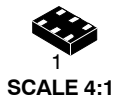
<b>DOCUMENT NUMBER:</b>	<b>98ASB42985B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88/SC70-6/SOT-363</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE

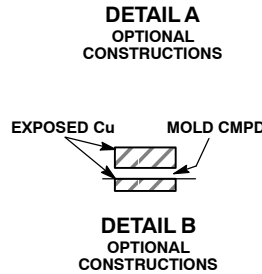
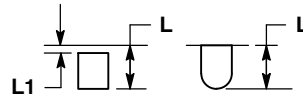
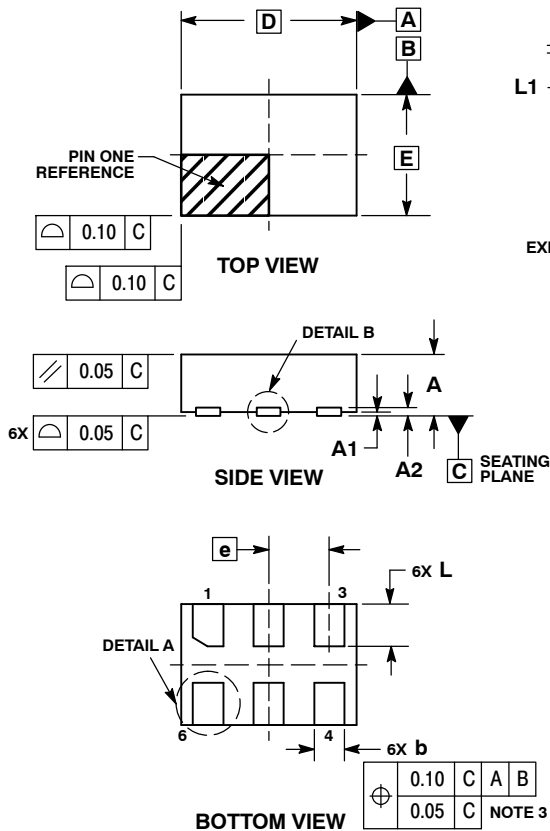
## PACKAGE DIMENSIONS

ON Semiconductor®



UDFN6, 1.45x1.0, 0.5P  
CASE 517AQ-01  
ISSUE O

DATE 15 MAY 2008



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

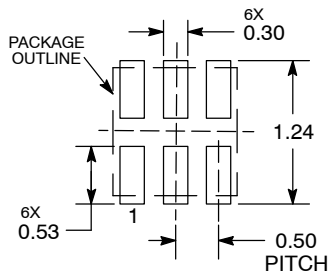
**GENERIC MARKING DIAGRAM\***



- X = Specific Device Code
- M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

**MOUNTING FOOTPRINT**



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	98AON30313E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>STATUS:</b>	ON SEMICONDUCTOR STANDARD	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	UDFN6, 1.45X1.0, 0.5P	<b>PAGE 1 OF 2</b>







ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

### Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative