HCS32MS

Radiation Hardened Quad 2-Input OR Gate

FN3057
Rev 1.00
April 11, 2007

The Intersil HCS32MS is a Radiation Hardened Quad 2-Input OR Gate. A low on both inputs forces the output to a low state.

The HCS32MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

The HCS32MS is supplied in a 14 Ld Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HCS32DMSR	Q 5962R95 78101VCC	-55°C to +125°C	14 Ld SBDIP	D14.3
HCS32KMSR	Q 5962R95 78101VXC	-55°C to +125°C	14 Ld Ceramic Flatpack	K14.A
HCS32D/ Sample		+25°C	14 Ld SBDIP	
HCS32K/ Sample		+25°C	14 Ld Ceramic Flatpack	
HCS32HMSR		+25°C	Die	

Intersil Pb-free hermetic packaged products employ SnAgCu or Au termination finish, which are RoHS compliant termination finishes and compatible with both SnPb and Pb-free soldering operations. Ceramic dual in-line packaged products (CerDIPs) do contain lead (Pb) in the seal glass and die attach glass materials. However, lead in the glass materials of electronic components are currently exempted per the RoHS directive. Therefore, ceramic dual inline packages with Pb-free termination finish are considered to be RoHS compliant.

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200k RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
- V_{IL} = 30% of V_{CC} Max
- V_{IH} = 70% of V_{CC} Min
- Input Current Levels $I_i \leq 5\mu A$ @ VOL, VOH

Functional Diagram

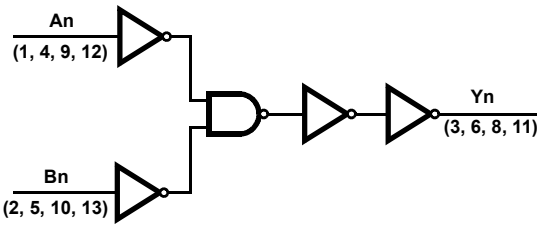


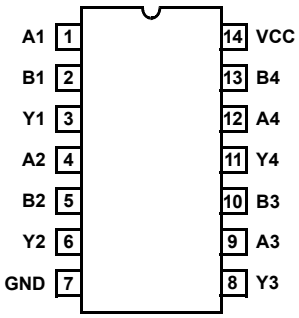
TABLE 1. TRUTH TABLE

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	H

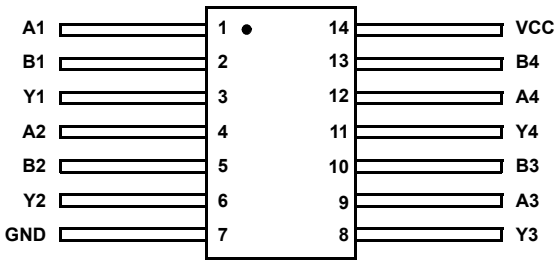
NOTE: L = Logic Level Low, H = Logic level High

Pinouts

HCS32MS
14 LD SBDIP
TOP VIEW



HCS32MS
14 LD CERAMIC FLATPACK
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG). . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec). . . . . +265°C
Junction Temperature (TJ). . . . . +175°C
ESD Classification . . . . . Class 1

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . 100ns/V Max
Operating Temperature Range (TA). . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

Thermal Information

Thermal Resistance (Notes 1, 2)	θJA	θJC
SBDIP Package	74°C/W	24°C/W
Ceramic Flatpack Package	116°C/W	30°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 0.68W
Ceramic Flatpack Package 0.43W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package . . . . . 13.5mW/°C
Ceramic Flatpack Package . . . . . 8.6mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

DC Electrical Electrical Performance Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMP (°C)	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25	-	10	µA
			2, 3	+125, -55	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25	4.8	-	mA
			2, 3	+125, -55	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25	-4.8	-	mA
			2, 3	+125, -55	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25, +125, -55	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25, +125, -55	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25, +125, -55	VCC - 0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25, +125, -55	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25	-	±0.5	µA
			2, 3	+125, -55	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70 (VCC), VIL = 0.30(VCC), (Note 3)	7, 8A, 8B	+25, +125, -55	-	-	-

NOTES:

3. This is just to show continuing notes in the document.
4. This is a row format electrical spec table.

AC Electrical Performance Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS (NOTES 5, 6)	GROUP A SUBGROUPS	TEMP (°C)	LIMITS		UNITS
					MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	9	+25	2	18	ns
			10, 11	+125, -55	2	20	ns
Data to Output	TPLH	VCC = 4.5V	9	+25	2	20	ns
			10, 11	+125, -55	2	22	ns

NOTES:

5. All voltages referenced to device GND.
6. AC measurements assume RL = 500Ω, CL = 50pF, Input tr = tf = 3ns, VIL = GND, VIH = VCC.

Electrical Performance Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	NOTES	TEMP (°C)	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	7	+25	-	6	pF
			7	+125, -55	-	11	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	7	+25	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	7	+25	-	15	ns
			7	+125	-	22	ns

NOTES:

7. The parameters listed in the Electrical Performance Characteristics are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

DC Post Radiation Electrical Performance Characteristics

PARAMETER	SYMBOL	(NOTES 8, 9) TEST CONDITIONS	TEMPERATURE (°C)	200k RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25	-	0.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOL = 50μA	+25	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOH = -50μA	+25	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), (Note 10)	+25	-	-	-

DC Post Radiation Electrical Performance Characteristics (Continued)

Data to Output	TPHL	VCC = 4.5V	+25	2	20	ns
	TPLH	VCC = 4.5V	+25	2	22	ns

NOTES:

8. All voltages referenced to device GND.
9. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
10. For functional tests VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

Operating Specifications

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3µA
IOL/IOH	5	-15% of 0 Hour

Applicable Subgroups

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 11)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11, (Note 12)
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTES:

11. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.
12. Burn-In and Operating Life Test, Delta Parameters (+25°C) only.

Total Dose Irradiation

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	DC Post Radiation Electrical Performance Characteristics on page 4	1, 9	DC Post Radiation Electrical Performance Characteristics on page 4 (Note 13)

NOTES:

13. Except FN test which will be performed 100% Go/No-Go.

Static And Dynamic Burn-In Test Connections

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 14)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 14)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 15)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

14. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in

15. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

Irradiation Test Conditions

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTES:

16. Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 17 and 18)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 18)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 19)

100% External Visual, Method 2009

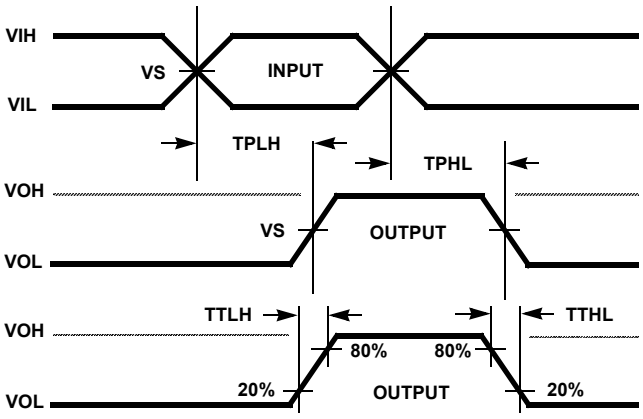
Sample - Group A, Method 5005 (Note 20)

100% Data Package Generation (Note 21)

NOTES:

17. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
18. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
19. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
20. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
21. Data Package Contents:
    - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
    - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
    - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
    - X-Ray report and film. Includes penetrometer measurements.
    - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
    - Lot Serial Number Sheet (Good units serial number and lot number).
    - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
    - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Timing Diagrams



AC Load Circuit

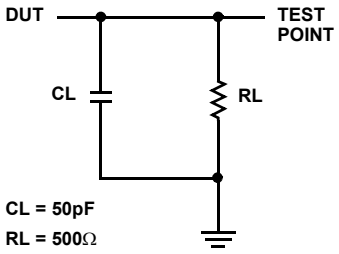


TABLE 1. AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:

87milsx88 mils

2.20mmx2.2mm

METALLIZATION:

Type: SiAl

Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:

Type: SiO_2

Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:

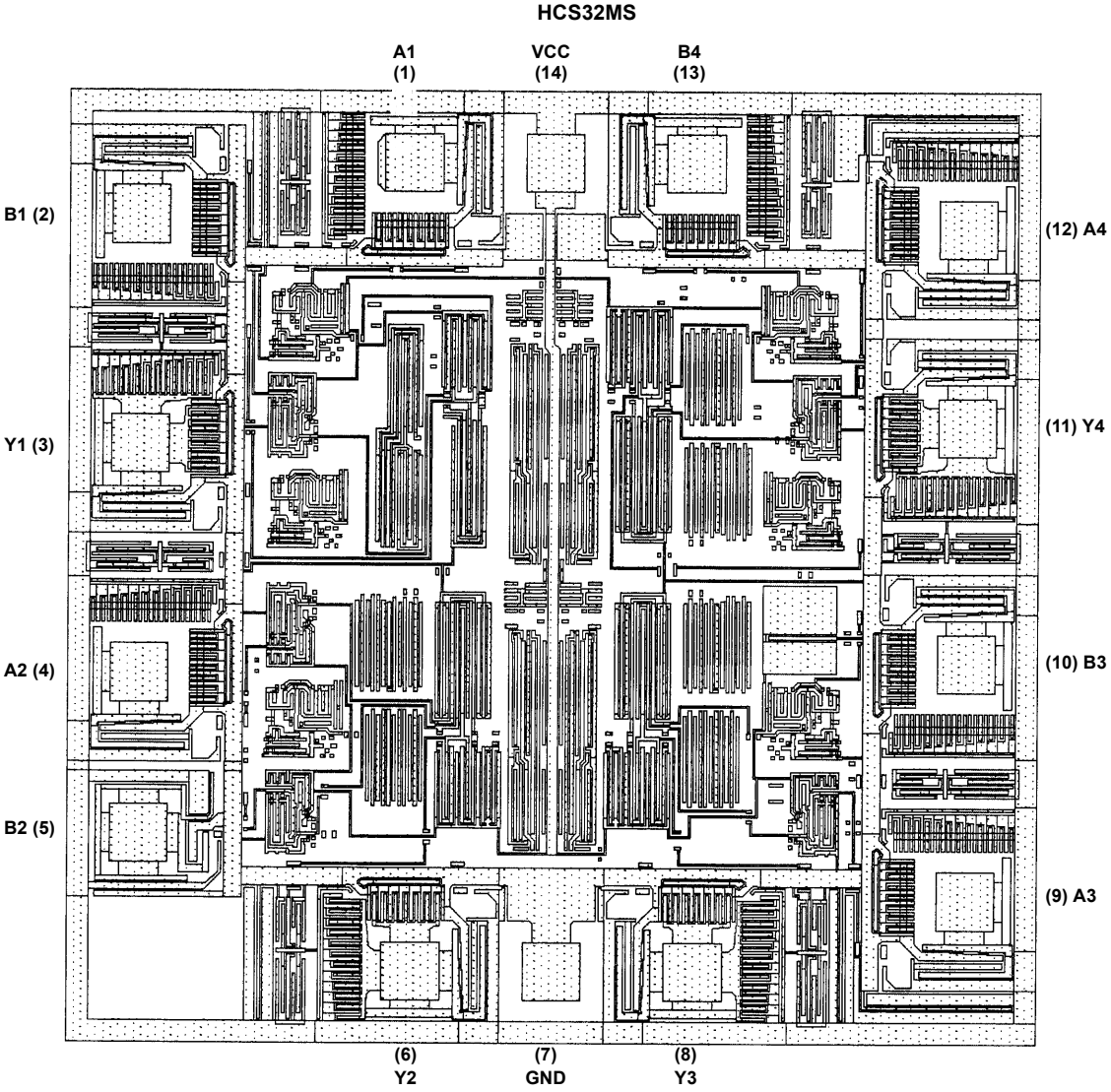
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:

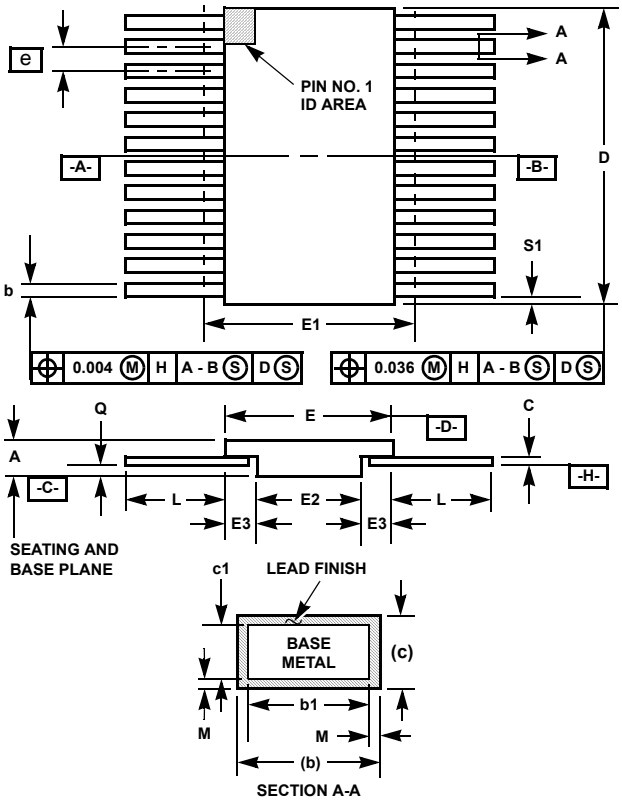
100µm x 100µm

4milsx4mils

Metallization Mask Layout



Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

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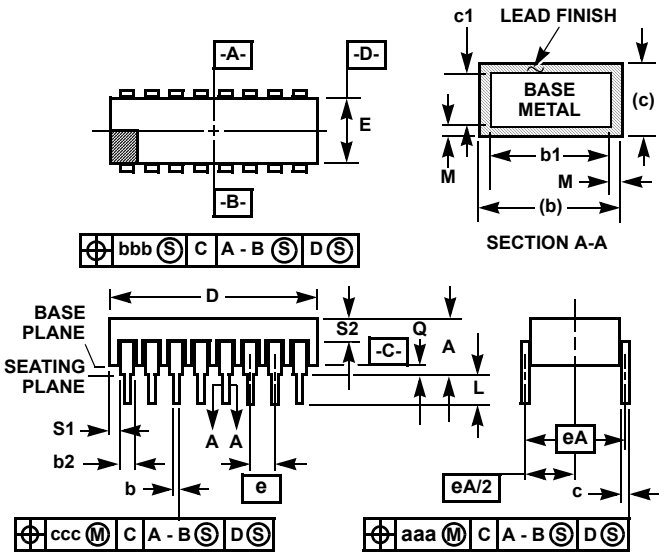
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

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