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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E45RA-MW307-N

Overview:

- 4.5-inch TFT (61.54x110.09 ΥΥ)
- 480È854 LJìÈŜfă
- 2-lane MIPI DSI Interface
- ² ìŘŜ ¢ŜΥLJerature
- Top View
- Transmissive
- No Touch Panel
- 307 nits
- TFT IC: ILI9806E
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit and a backlight unit. The resolution of the 4.5" TFT LCD contains 480(RGB)x854 pixels and can display up to 16.7M colors.

TFT Features

Low Input Voltage: 3.3V
Display Colors: 16.7M
Interface: 2-lane MIPI DSI

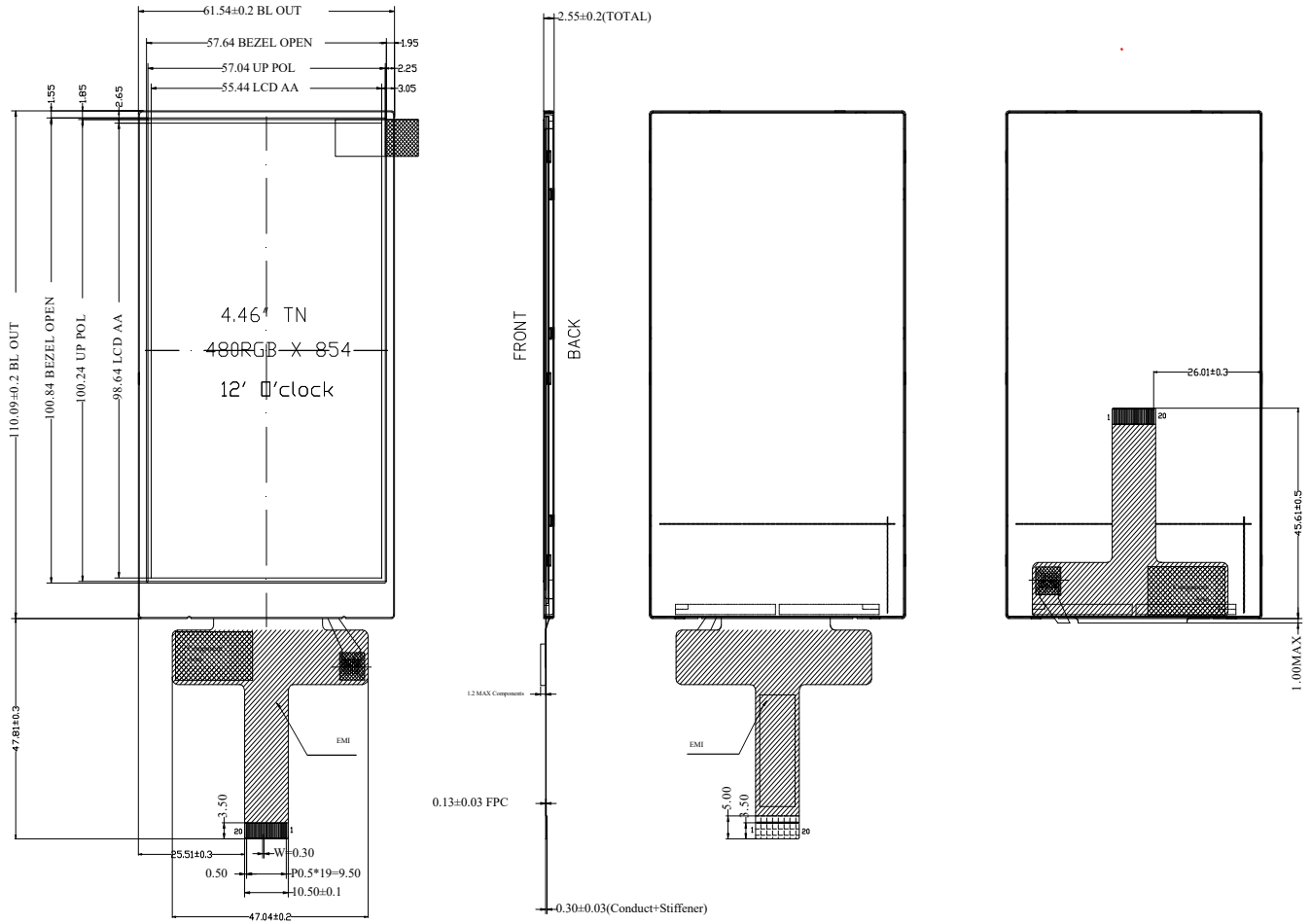
General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	55.44(H) x 98.64(V) (4.5 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Number of pixels	480(RGB)x854	pixels	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.1155(H)x0.1155(V)	mm	-
Viewing angle	12:00	o'clock	-
TFT Controller IC	ILI9806E	-	-
TFT Interface	2-lane MIPI	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20-+70	℃	-
Storage temperature	-30-+80	℃	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		61.54		mm	-
	Vertical (V)		110.09		mm	-
	Depth (D)		2.55		mm	-
	Weight		--		g	

1. Outline Dimensions

ReV.	Revision content description	Date
A	FIRST	2019.06.25



NO.	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	VCI
7	IOVCC
8	TE
9	RESET
10	GND
11	MIPI_D1P
12	MIPI_D1N
13	GND
14	MIPI_CLP
15	MIPI_CLN
16	GND
17	MIPI_D0P
18	MIPI_D0N
19	GND
20	GND

Backlight LED Circuit

1.) Display Type: 4.46" TFT (16:9), 16.7M colors
2.) Display mode: Transmissive, Normally White
3.) 12:00 viewing direction
4.) TFT Driver IC: ILI9806E (COG)
5.) TFT Interface: 2-lane MIPI DSI
6.) VDD/VCI: 3.3V, IOVCC:1.65-3.3V
7.) Operating Tempe: -20-70 C, Storage Temp: -30-80 C
8.) Backlight: LED White, 8 LEDs, 40mA, 12.8+/-0.3V

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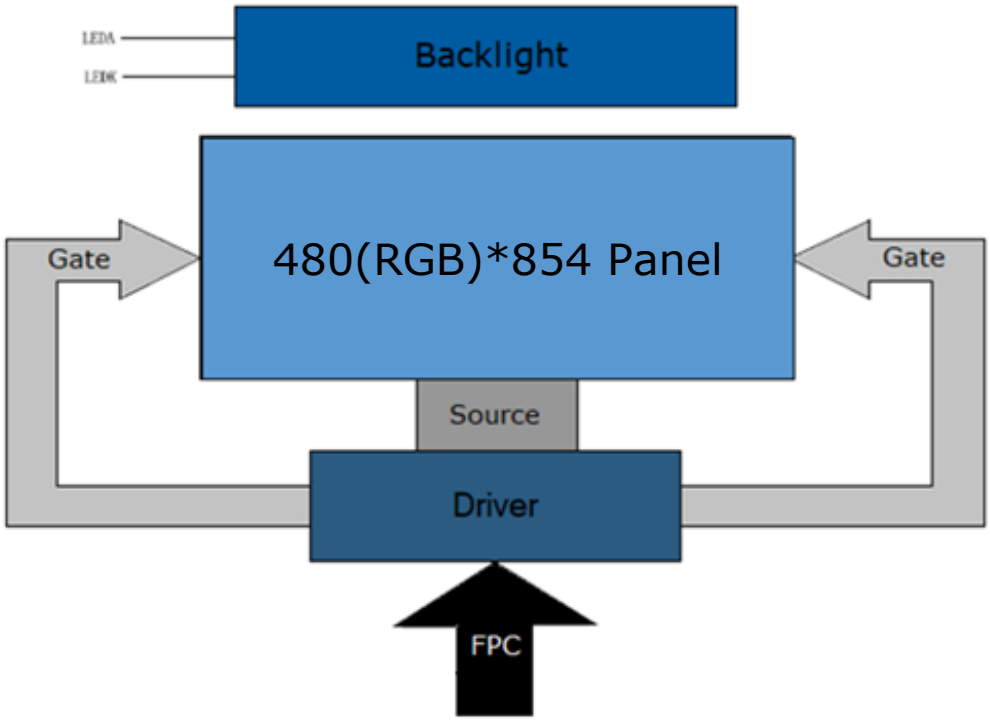
TOLERANCE	DRAWING NAME	
	PARTS NO.	E45RA-MW307-N
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2	Drawn	Unit
	Checked	mm
Scale 1:1	Approve	Page 1/1

2. Block Diagram



3. Input TFT Terminal Pin Assignment

Recommended Connector: FH19C-20S-0.5SH(10)

NO.	Symbol	Description	I/O
1	NC	Not connected	
2	LEDK	Cathode pin of the backlight	P
3	NC	Not connected	
4	LEDA	Anode pin of the backlight	P
5	NC	Not connected	
6	VCI	Supply voltage (3.3V)	P
7	IOVCC	I/O power supply voltage (1.65-3.3V)	P
8	TE	Tearing effect output	O
9	RESET	External reset signal. Initializes the chip at active low.	I
10	GND	Ground	P
11	D1P	MIPI DSI differential data pair lane 1	I/O
12	D1N		
13	GND	Ground	P
14	CLKP	MIPI DSI differential clocking pair	I/O
15	CLKN		
16	GND	Ground	P
17	D0P	MIPI DSI differential data pair lane 0	I/O
18	D0N		
19	GND	Ground	P
20	GND	Ground	P

I: Input, O: Output, P: Power

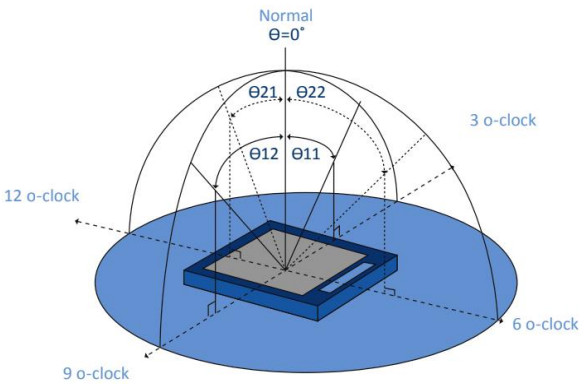
4. LCD Optical Characteristics

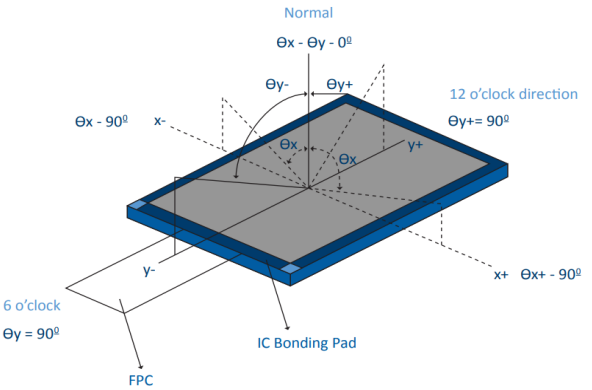
4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S%	θ=0 Normal viewing angle	--	58	--	%	(3)
Contrast Ratio		CR		--	800	--	%	(2)
Response Time	Rising	TR+TF		--	16	32	ms	(4)
	Falling							
Color Filter Chromaticity	White	W_X		0.273	0.313	0.353		(5)(6)
		W_Y		0.290	0.330	0.370		
	Red	R_X		0.604	0.624	0.644		
		R_Y		0.327	0.357	0.377		
	Green	G_X		0.343	0.363	0.383		
		G_Y		0.569	0.589	0.609		
	Blue	B_X		0.128	0.148	0.168		
		B_Y		0.055	0.075	0.095		
Viewing Angle	Hor.	ΘL	CR≥10	60	70	--	degrees	(1)(6)
		ΘR		60	70	--		
	Ver.	ΘT		60	70	--		
		ΘB		60	70	--		
Option View Direction		All						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



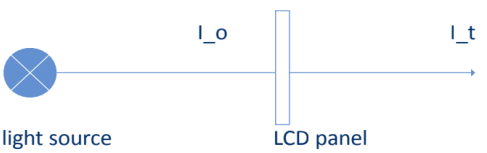


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

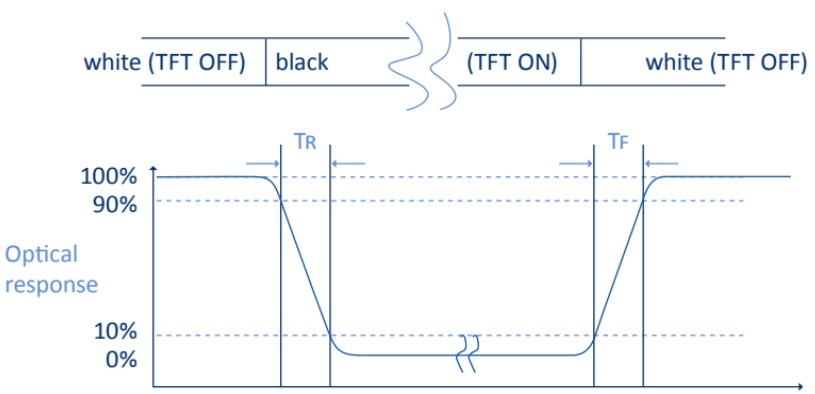
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90%to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

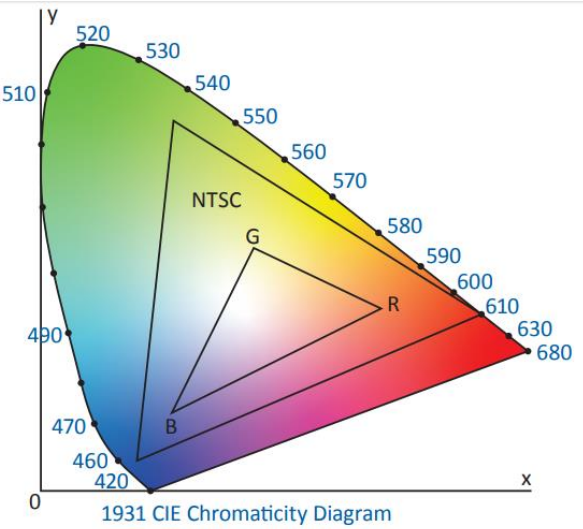
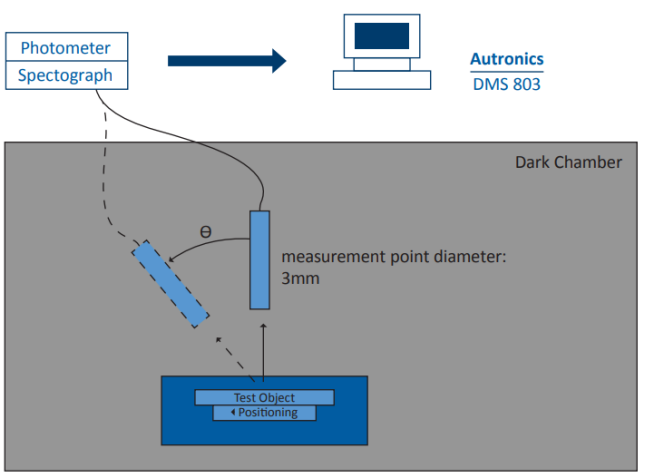


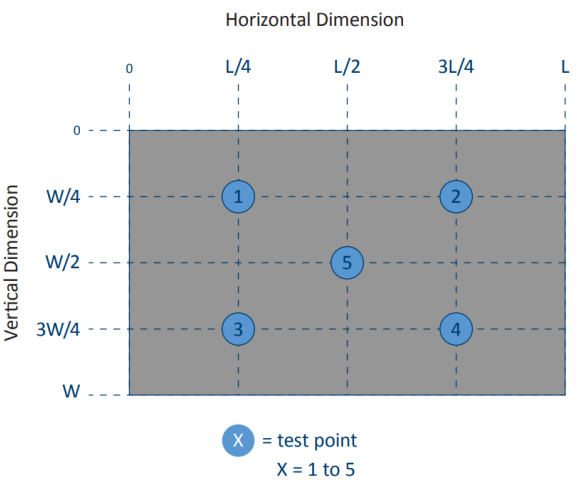
Fig. 1931 CIE chromacity diagram

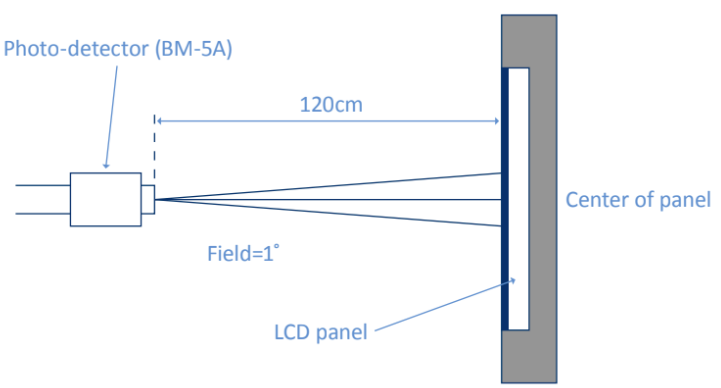
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.2	V
DC/DC Supply Voltage	IOVCC	-0.3	3.3	
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital Supply Voltage	IOVCC	1.65	1.8	3.6	V	
Normal Mode Current	IDD	--	26	--	mA	
Level Input Voltage	VIH	0.7IOVCC	--	IOVCC	V	
	VIL	GND	--	0.3IOVCC	V	
Level Ouput Voltage	VOH	0.8IOVCC	--	IOVCC	V	
	VOL	GND	--	0.2IOVCC	V	

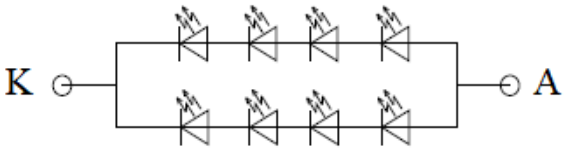
5.4 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	30	40	--	mA	
Forward Voltage	VF	--	12.8	--	V	
LCM Luminance	LV	307	--	--	cd/m2	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 8 white LEDs.

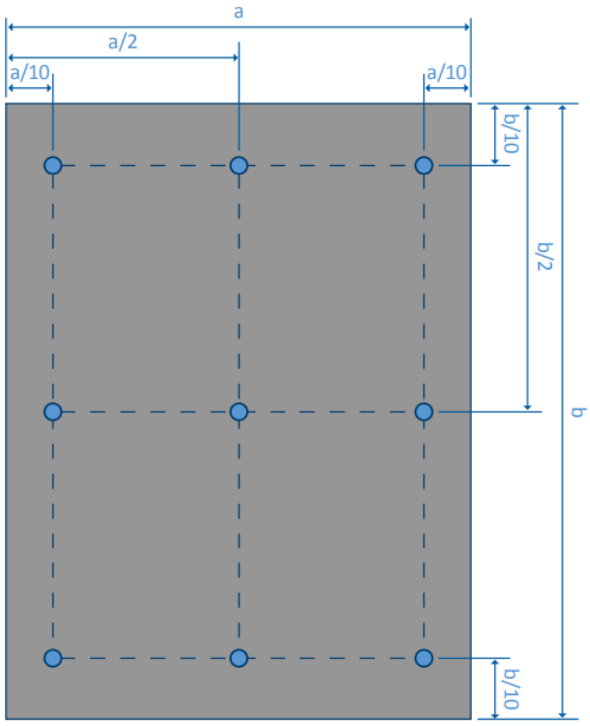
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. MIPI Interface AC Characteristics

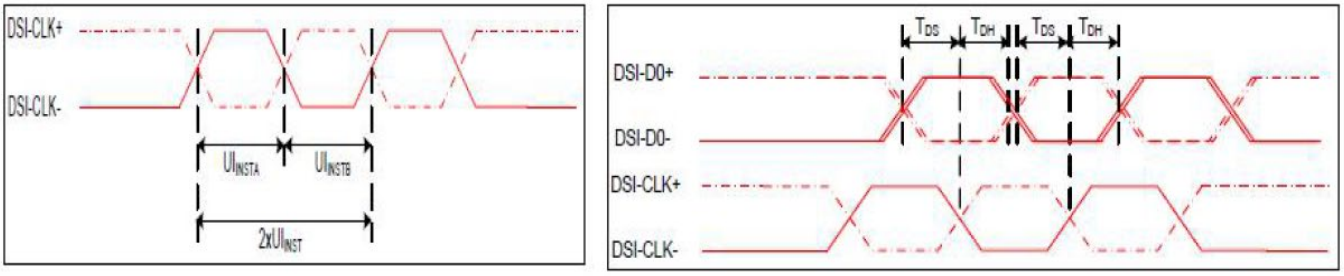


Figure 6.1: DSI Clock Channel Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
DSI-CLK+/-	2xUIINSTA	Double UI Instantaneous	4	25	ns	
DSI-CLK+/-	UIINSTA UIINSTB	UI Instantaneous Halves	2	12.5	ns	UI=UIINSTA=UIINSTB
DSI-Dn+/-	tDS	Data to clock setup time	0.15	--	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	--	UI	

Table 6.1: MIPI Interface High Speed Mode Timing Characteristics

6.2 Low Power Mode

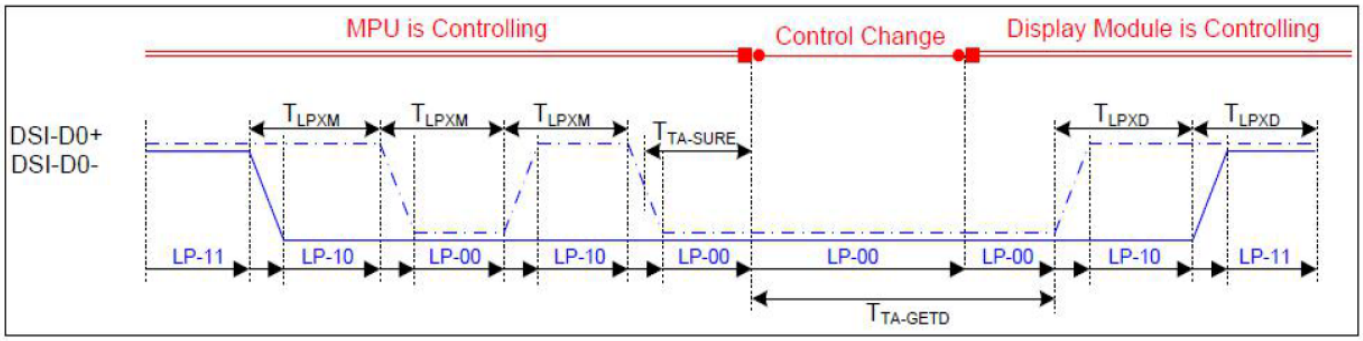


Figure 6.2: Bus Turnaround (BTA) from Display Module to MPU Timing Diagram

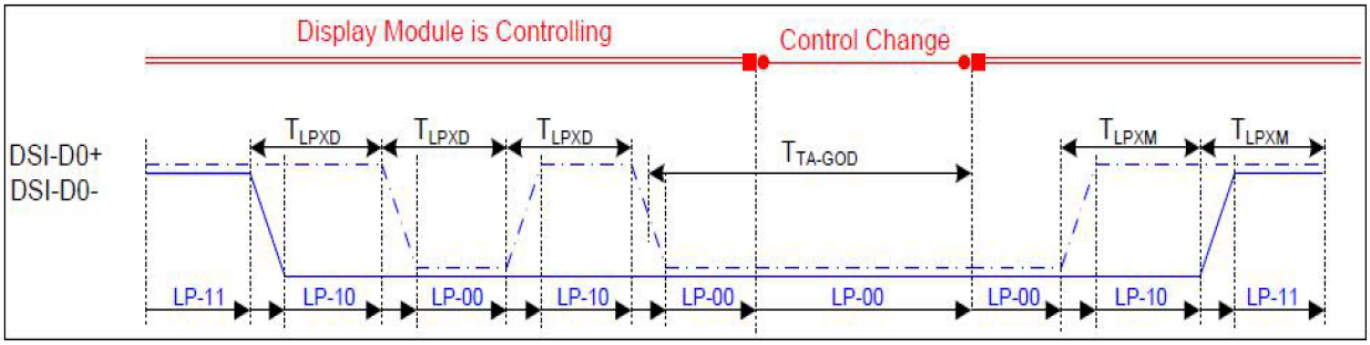


Figure 6.3: Buss Turnaround (BTA) from MPU to Display Module Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
DSI-D0+/-	TLPXM	Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU starts driving	TLPXD	2xTLPXD	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	4xTLPXD		ns	Output

Table 6.2: MIPI Interface Low Power Mode Timing Characteristics

6.3 Bursts Mode

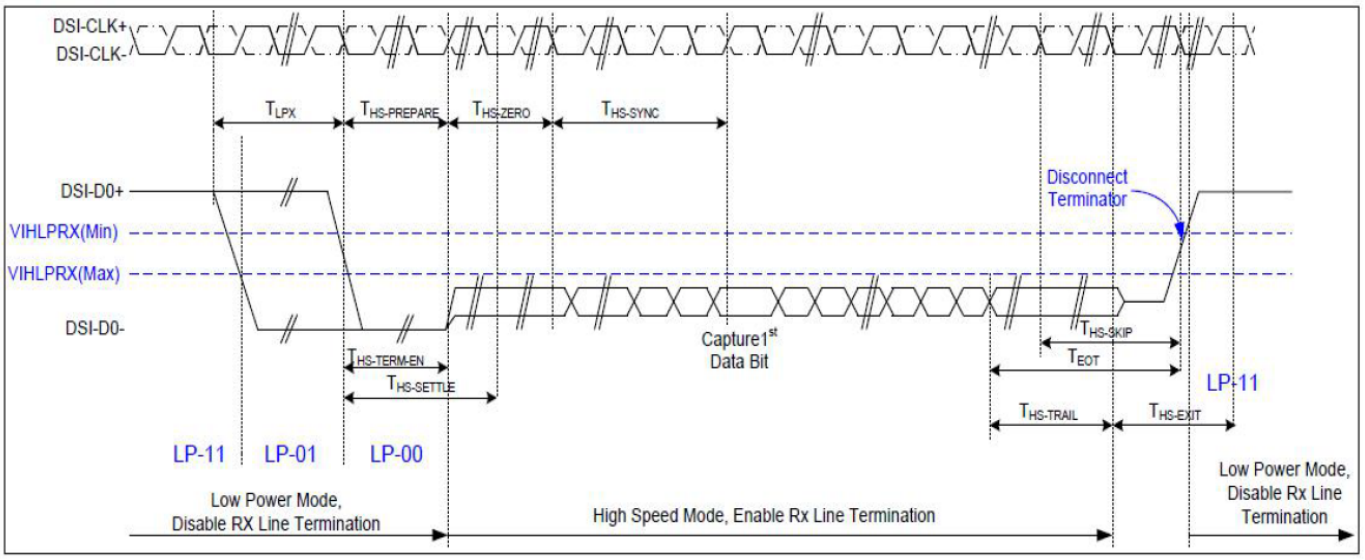


Figure 6.4: Data Lanes Low Power Mode to/from High Speed Mode Timing Diagram

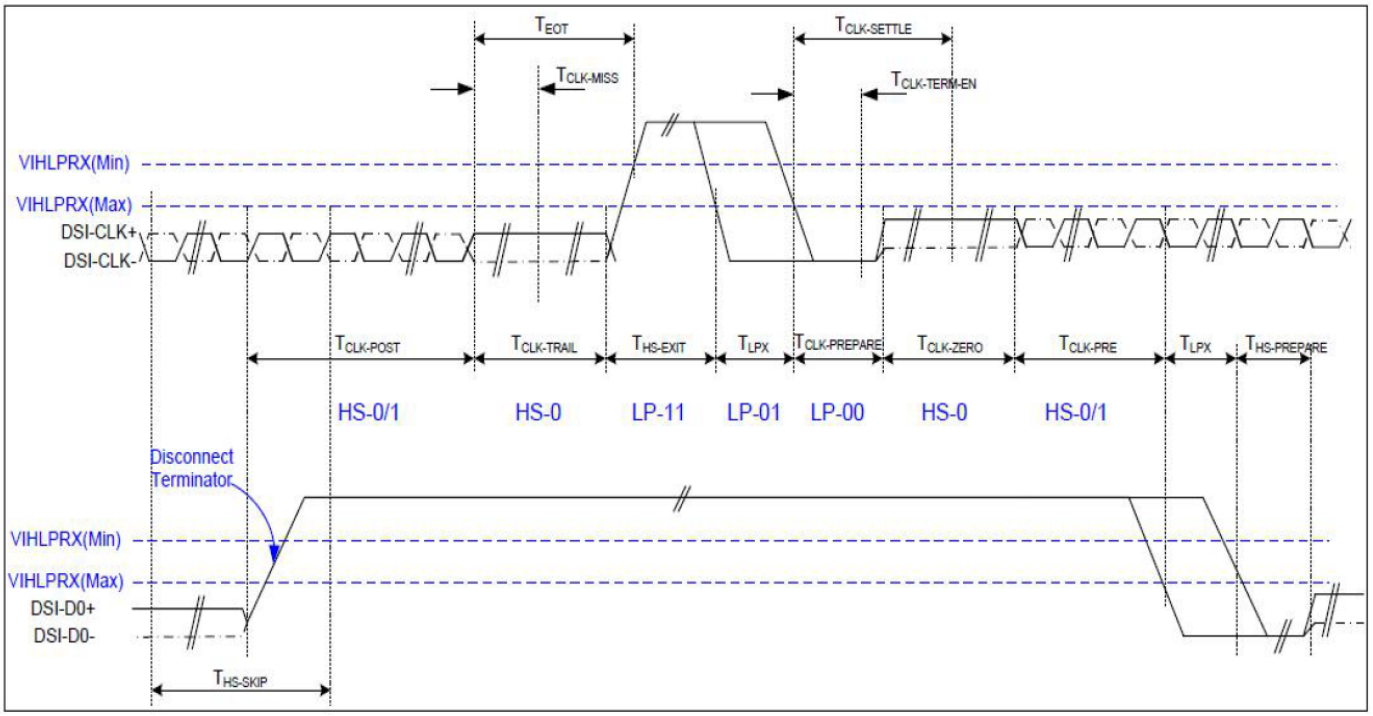


Figure 6.5: Clock Lanes High Speed Mode to/from Low Power Mode Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	--	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4UI	85+6UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	--	35+4UI	ns	Input
DSI-Dn+/-	THS-PREPARE+ THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	140+10UI	--	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	--	ns	Input
DSI-Dn+/-	THS-TRIAL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4UI	--	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transitioned to LP mode	60+52UI	--	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	--	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	--	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for Hs transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time out at clock ands display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+	Minimum lead HS-0 drive period before starting clock	300	--	ns	Input
DSI-CLK+/-	TCLK-ZERO TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	--	ns	Input
DSI-CLK+/-	TEOT	Time from start of TCLK-TRAIL period to start of LP-11 state	--	105+12UI	ns	Input

Table 6.3: Bursts Mode LP to/from HS Mode Timing Characteristics

6.4 Reset Timing

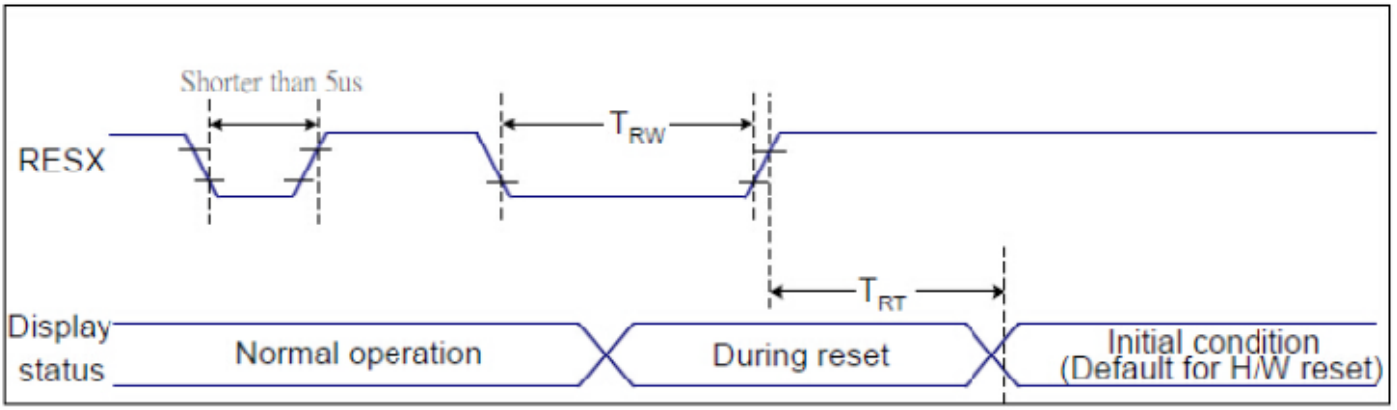


Figure 6.6: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

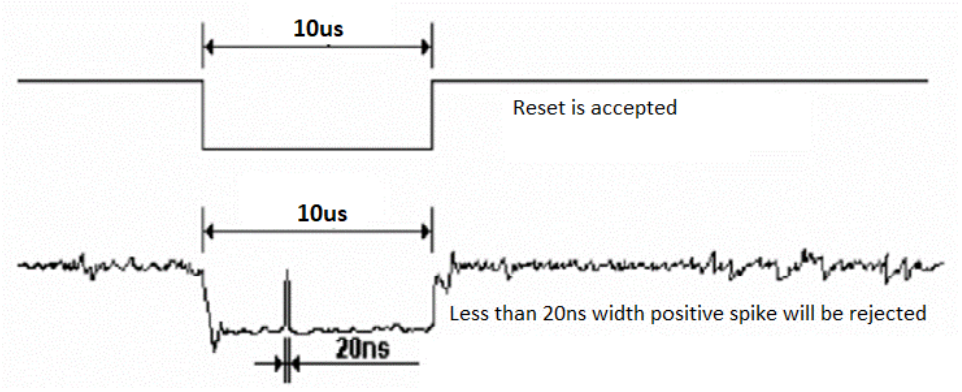
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.