Getting started with the EVALST-ISOSD61T/L board

Introduction

The EVALST-ISOSD61L/61T is a full featured evaluation board designed to allow the user to evaluate all the features of the ISOSD61 and ISOSD61L isolated analog-to-digital converters (ADC).

This document describes how to use the evaluation board of the Isolated Sigma-Delta Converter, how to supply powers and signals, and how to read and filter properly the converted data.

Table 1. Applicable products

Type	Reference products
Isolated Sigma-delta modulator, TTL input and output levels	ISOSD61
Isolated Sigma-delta modulator, LVDS input and output levels	ISOSD61L

Figure 1. EVALST-ISOSD61L board

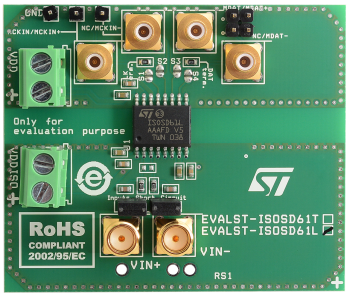
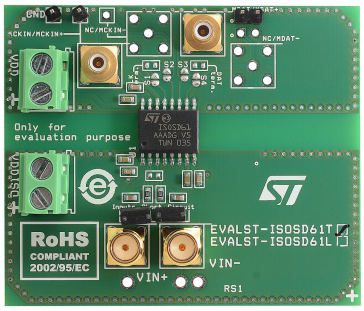


Figure 2. EVALST-ISOSD61T board



1 Getting started

1.1 System requirements

To test the board, the necessary hardware is:

- An isolated power supply with 5 V, 100 mA capability
- A power supply with 3.3 V to 5 V, 50 mA capability
- A clock generator capable of producing a square wave with frequency from 5 MHz to 25 MHz, TTL-level (0 – 3 V) for the ISOSD61 device
- A clock generator capable to produce two complementary square waves with frequency from 5 MHz to 25 MHz, LVDS-level (1.2 V common mode voltage, +-0.3 V differential voltage) for the ISOSD61L device
- An analog signal source (differential or single-ended) to be applied to the analog input(s) or a current to be measured through a current shunt
- A digital equipment (PC, FPGA board, MCU board…) capable of implementing a digital filtering of the sigma-delta modulated output.

1.2 Connecting the board

Follow the steps below to run it:

- Use the two twin-screw green connectors to supply 5 V to the isolated front end (VDDiso, M1) and 3.3 V to 5 V to the digital interface (VDD, M2). Carefully respect the polarity. Reversing the polarity may damage the device.
- Connect the clock source and the data output to the on-board SMB connectors, respectively. Alternatively, header pin connectors can be used. According to the device interface type:
  - ISOSD61 (TTL): connect the clock generator to the MCLKIN connector (BNC2, or J2 and J5) and the data cable to the MDAT connector (BNC4 or P1). Ensure the voltage amplitude is TTL-level compliant.
  - ISOSD61L (LVDS): connect the clock paired cables to the MCLKIN+ and MCLKIN- connectors (BNC2 and BNC3, or J2, J4 and J5) and the data paired cables to the MDAT+ and MDAT- connectors (BNC4 and BNC5, or P1 and P2). Ensure that levels and polarity are LVDS-level compliant and they are adjusted to the on-board 110 ohm differential termination resistors. In the case of MDAT signals terminated to the end of the line to the digital equipment, remove the MDAT termination resistor opening the S3 and S4 soldered short-circuit pads.
  - In case of using the header pin connectors, identify the right GND reference pin (J5 for the clock signals and pin # 2 of P1 and P2 for the data signals)
- About the analog input signal, different options are possible:
  - If a shunt is connected, the current to be sensed will be converted to a voltage signal and fed directly to the analog inputs. No additional connections are required. Ensure not to exceed the current and power ratings of the shunt. (Note: The board is designed to fit a BKW-M-R0003-5.0 shunt made by Isabellenhütte Heusler. It's rated 0.3 milliohm, 100 A max., 3 W max.)
  - In the case of a single-ended analog input signal, place a jumper cap to the J11 2-pin header and connect the signal cable to the VIN+ SMA on-board connector (BNC1). The maximum signal amplitude is 640 mVp-p.
  - In the case of a differential analog input signal, connect the paired cables to the VIN+ and VIN- (BNC1 and BNC6) SMA on-board connectors. Ensure the J10 and J11 pin headers are free from jumper caps.

1.3 Sigma-Delta data processing

The MDAT, 1-bit sigma-delta stream must be converted to an N-bit digital information in order to provide a high resolution accurate digital representation of the sampled analog signal. This conversion process is the so-called digital decimation filtering process. Among the various different decimation techniques, the use of a Sinc3 digital filter is recommended because of its reasonable stopband attenuation combined with its quick step response.

The code below is an example of a generic Sinc3 filter written for GNU Octave that can be easily ported to other languages or systems:

```
function [output, output_dec]=sinc3_generic(in)
    %in is 1xsamples
    %output is 1xsamples
    %output_dec is 1x(samples/dec_fact)
    nbits = 25;
    accbits = 46; %minimum accumulator size
    dutbits = 16;
    stages = 3;
    dec_fact = 256;
    dim = size(in);
    samples = dim(2);
    feed_state = zeros(1,stages);
    fwd_state = zeros(1, stages);
    i = 1;
    out_feed_state = 0;
    for k=1:samples
        if ( i > 1 )
            output(k) = round(out_feed_state * 2^((dutbits-1)));
            else
            output(k) = 0;
            end
        if ( k == dec_fact*i )
            output_dec(i) = round(out_feed_state * 2^((dutbits-1)));
            in_fwd = feed_state(stages);
            fwd_sum = 0;
            for s=1:stages
            fwd_sum += fwd_state(s);
            end
            out_feed_state = in_fwd - fwd_sum;
            si = stages;
            while(si > 1)
            fwd_sum = 0;
            for s=1:(si-1)
            fwd_sum += fwd_state(s);
            end
            fwd_state(si) = in_fwd - fwd_sum;
            si--;
            end
            fwd_state(1) = in_fwd;
            i++;
            end
```

```
        si = stages;
        while(si > 1)
        feed_state(si) = feed_state(si) + feed_state(si-1);
        si--;
        end
        feed_state(1) = feed_state(1) + in(k)* 2^(-(nbits-1));
        end
end
```

Revision history

Table 2. **Document revision history**

Date	Version	Changes
11-Jan-2021	1	Initial release.
15-Jan-2021	2	Title updated.
05-Mar-2021	3	Updated title of Figure 2.

Contents

List of tables

List of figures