MAX38902E

14µV$_{RMS}$ Low Noise 500mA LDO Linear Regulator

General Description

The MAX38902E is low-noise linear regulator that delivers up to 500mA of output current with only 14µV$_{RMS}$ of output noise from 10Hz to 100kHz. This regulator maintains ±1% output accuracy over a wide input voltage range, requiring only 100mV of input-to-output headroom at full load. The 600µA no-load supply current is independent of dropout voltage.

The MAX38902E has a resistor adjustable output voltage in the range of 0.8V to 5.0V and includes an active-low POK output. The device features a programmable output soft-start rate, output over-current and thermal overload protection.

The MAX38902E is offered in an 8-pin TDFN package.

Applications

- Communication Circuitry
- Audio Systems
- High-Resolution Data Acquisition Systems

Benefits and Features

- Delivers Flexible Operating Range
  - 1.7V to 5.5V Input Voltage Range
  - 0.8V to 5.0V Output Voltage Range
  - 500mA Maximum Output Current
  - 100mV Maximum Dropout at 500mA Load (3.6V$_{IN}$)
  - < 0.1µA Shutdown Supply Current
- Reduces Noise and Improved Accuracy
  - 14uV$_{RMS}$ Output Noise, 10Hz to 100kHz
  - 600µA Operating Supply Current
  - 45dB PSRR at 100kHz
  - ±1% DC Accuracy Over Load, Line, and Temperature
- Enables Easy-of-Use and Robust Protection
  - Minimum C$_{OUT}$ 4µF
  - Programmable Soft-Start Rate
  - Overcurrent and Overtemperature Protection
  - Output-to-Input Reversed Current Protection
  - POK Output
- Reduces Size, Improves Reliability
  - 2mm x 2mm 8-pin TDFN Package
  - -40ºC to 125ºC Operating Temperature

Ordering Information appears at end of data sheet.

Typical Operating Circuit

Absolute Maximum Ratings

IN, INS, OUT, EN, $\overline{POK}$, FB, BYP to GND .... -0.3V to +6V
Output Short-Circuit Duration .... Continuous
Continuous Power Dissipation (T$_A$ = +70°C) ....
TDFN (derate 9.8mW/°C above 70°C) 784mW
Operating Temperature Range .... -40°C to +125°C

Maximum Junction Temperature .... +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (Soldering, 10 seconds) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T822+3C
Outline Number	21-0168
Land Pattern Number	90-0065
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ$_{JA}$)	130°C/W
Junction-to-Case Thermal Resistance (θ$_{JC}$)	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ$_{JA}$)	102°C/W
Junction-to-Case Thermal Resistance (θ$_{JC}$)	8°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 10nF, C_{IN} = 10µF, C_{OUT} = 10µF, circuit of *Typical Operating Circuit*, typical values are at T_J = +25°C, unless otherwise specified. (Note 1))
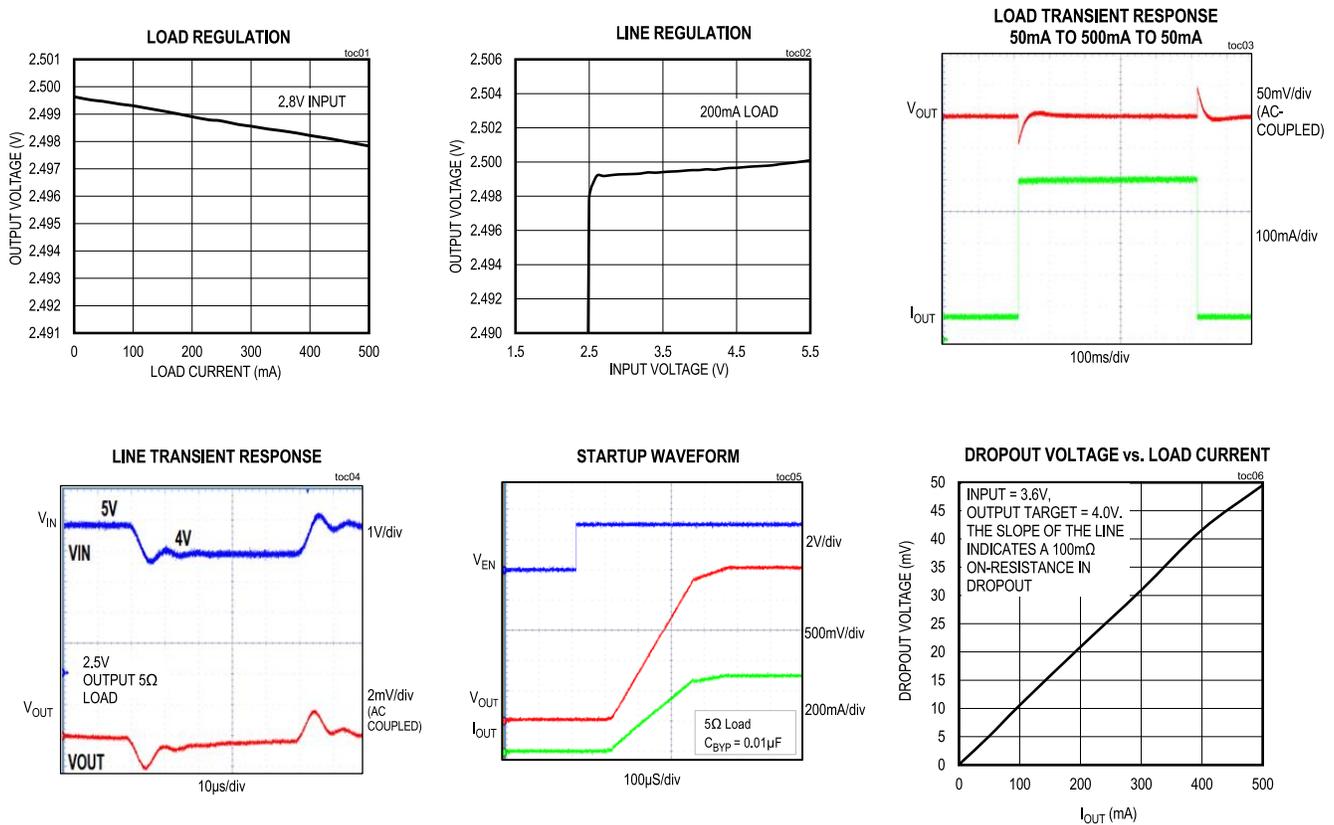
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by Output Accuracy		1.7		5.5	V
Input Undervoltage Lockout	V_{IN_UVLO}	V_{IN} rising, 100mV hysteresis		1.5	1.6	1.7	V
Output Voltage Range	V_{OUT}	V_{IN} > V_{OUT} + 0.1V		0.8		5.0	V
Output Capacitance	C_{OUT}	For stability and proper operation		4	10		µF
Supply Current	I_Q	I_{OUT} = 0mA			600	1500	µA
	$I_{SHUTDOWN}$	V_{EN} = 0V	T_J = +25°C		0.01	0.1	µA
			T_J = +125°C		700		nA
Feedback Accuracy	V_{FB}	I_{OUT} from 0.1mA to 500mA, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V, V_{OUT} from 0.8V to 5.0V		0.594	0.6	0.606	V
Load Regulation		I_{OUT} from 0.1mA to 500mA, V_{IN} = V_{OUT} + 300mV, V_{OUT} = 2.5V			0.07		%
Load Transient		I_{OUT} = 50mA to 500mA to 50mA, t_{RISE} = t_{FALL} = 1µs			50		mV
Line Regulation		V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V, I_{OUT} = 200mA			0.06		%
Line Transient		V_{IN} = 4V to 5V to 4V, I_{OUT} = 500mA, t_{RISE} = t_{FALL} = 5µs			3		mV
Dropout Voltage (Note 2)		I_{OUT} = 500mA	V_{IN} = 3.6V		50	100	mV
Current Limit		V_{FB} = 0V, V_{IN} - V_{OUT} = 500mV		600	700	800	mA
Output Noise		I_{OUT} = 100mA, 10Hz to 100kHz	C_{BYP} = 47nF		14		μV_{RMS}
Power Supply Rejection Ratio	PSRR	I_{OUT} = 100mA	f = 1kHz		60		dB
			f = 10kHz		60		
			f = 100kHz		45		
			f = 1MHz		40		
BYP Capacitor Range	C_{BYP}	Regulator remains stable		0.001		0.1	µF
BYP Soft-Start Current		From BYP to GND during startup			50		µA
EN Input Threshold		V_{IN} from 1.7V to 5.5V	EN rising		0.8	1.2	V
			EN falling	0.4	0.7		
EN Input Leakage Current		V_{EN} from 1.7V to 5.5V	T_J = +25°C	-1	+0.001	+1	µA
			T_J = +125°C		0.01		
$\overline{POK}$ Threshold		V_{OUT} when $\overline{POK}$ switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		
$\overline{POK}$ Voltage, Low		I_{POK} = 1mA			10	100	mV
$\overline{POK}$ Leakage Current		V_{POK} = 5.5V	T_J = +25°C	-0.1	+0.001	+0.1	µA
			T_J = +125°C		0.01		

Electrical Characteristics (continued)

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 10nF, C_{IN} = 10µF, C_{OUT} = 10µF, circuit of *Typical Operating Circuit*, typical values are at T_J = +25°C, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Shutdown Threshold		T_J when output turns on/off	T_J rising		165		°C
			T_J falling		150		

Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at T_J = 25ºC only.

Note 2: Dropout voltage is defined as (V_{IN} - V_{OUT}), when V_{OUT} is 95% of its nominal value.

Typical Operating Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, T_A = 25°C, C_{IN} = 10µF , C_{OUT} = 10µF, unless otherwise noted.)

LOAD REGULATION

LINE REGULATION

LOAD TRANSIENT RESPONSE 50mA TO 500mA TO 50mA

LINE TRANSIENT RESPONSE

STARTUP WAVEFORM

DROPOUT VOLTAGE vs. LOAD CURRENT

Pin Configuration

MAX38902E
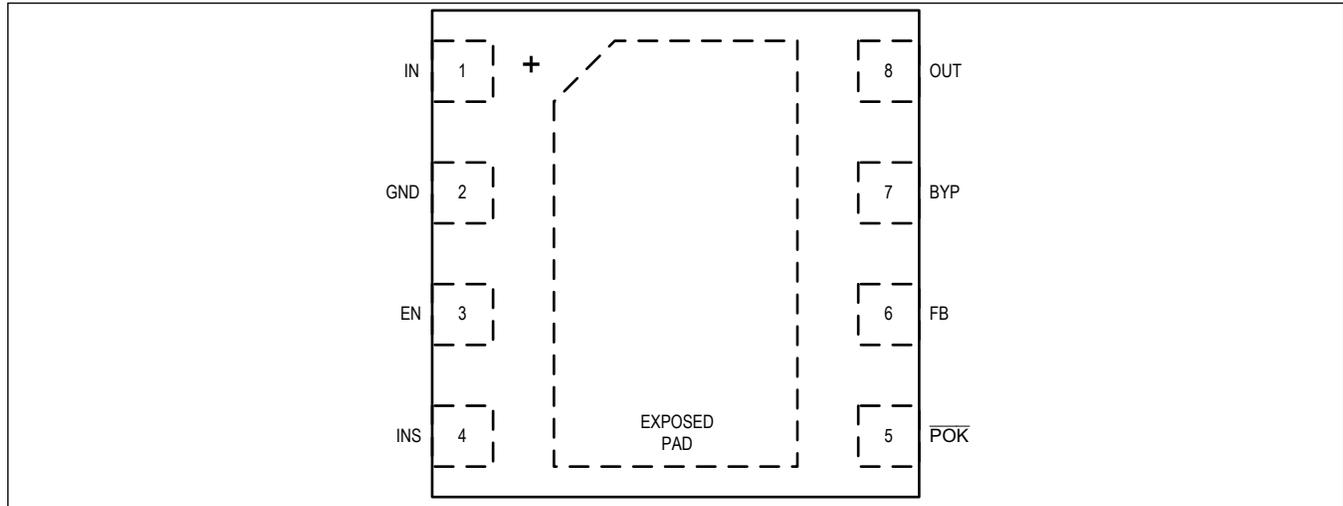
Pin Description

PIN	NAME	FUNCTION
1	IN	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V and bypass with a 10µF capacitor from IN to GND.
2	GND	Regulator Ground. Bring IN and OUT bypass capacitor GND connections to this pin for best performance.
3	EN	Enable Input. Connect this pin to a logic signal to enable (V_{EN} high) or disable (V_{EN} low) the regulator output. Connect to IN to keep the output enabled whenever a valid supply voltage is present.
4	INS	Input Sense Pin. Connect INS to IN.
5	$\overline{POK}$	Power-On Reset Output. Connect a pullup resistor from this pin to a supply to create a reset signal that goes low after the regulator output has reached its regulation voltage.
6	FB	Feedback Divider Input. Connect a resistor divider string from OUT to GND with the mid-point tied to this pin to set the output voltage. In the *Typical Application Circuit*, V_{OUT} = 0.6V x (1 + R3/R2).
7	BYP	Bypass Capacitor Input. Connect a 0.001µF to 0.1µF capacitor between OUT and BYP to reduce output noise and set the regulator soft-start rate.
8	OUT	Regulator Output. Sources up to 500mA at the output regulation voltage. Bypass with a 10µF (4µF minimum including voltage derating) low ESR (< 0.03Ω) capacitor to GND.
EP	EP	Exposed Pad. Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heat sinking.

Functional Diagrams

Detailed Description

The MAX38902E, low noise linear regulator delivers up to 500mA of output current, with only 14µV$_{RMS}$ of output noise in a 10Hz to100kHz bandwidth. This regulator maintains its output voltage over a wide input range, requiring only 100mV of input-to-output headroom at full load.

The MAX38902E maintains a low 600µA typical supply current, independent of the load current and drop-out voltage. The regulator control circuitry includes a programmable soft-start circuit, short-circuit, reverse input current, and thermal overload protection. Other features include an enable input and power-okay ($\overline{POK}$) output (see Typical Operating Circuit).

Enable (EN)

The MAX38902E includes an enable input (EN). Pull EN low to shut down the output, or drive EN high to enable the output. If a separate shutdown signal is not available, connect EN to IN.

Bypass (BYP)

The capacitor connected from BYP to OUT filters the noise of the reference, feedback resistors and regulator input stage, and provides a high-speed feedback path for improved transient response. A 0.01µF capacitor rolls-off input noise at around 32Hz.

The slew rate of the output voltage during startup is also determined by the BYP capacitor. A 0.01µF capacitor sets the slew rate to 5V/ms. This startup rate results in a 50mA slew current drawn from the input at start-up to charge the 10µF output capacitance.

The BYP capacitor value can be adjusted from 0.001µF to 0.1µF to change the startup slew rate according to the following formula:

$$\text{STARTUP SLEW RATE} = \frac{5V}{ms} \text{ x } \frac{0.01\,\mu F}{C_{BYP}}$$

where C$_{BYP}$ is in µF.

Note that this slew rate applies only at startup. That recovery from a short-circuit will occur at a slew rate approximately 500 times slower.

Also note that, being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Protection Features

The MAX38902E is fully protected from an output short-circuit by a current-limiting and thermal overload circuit. If the output is shorted to GND, the output current is limited to 700mA (typ). Under these conditions, the part quickly heats up. When the junction temperature reaches 165°C, a thermal limit circuit shuts off the output device. When the junction cools to 150°C, the output turns back on in an attempt to reestablish regulation. While the fault persists, the output current cycles on and off, as the junction temperature slews between 150°C and 165°C.

The MAX38902E is also protected against reverse current when the output voltage is higher than the input. In the event that extra output capacitance is used at the output, a power-down transient at the input would normally cause a large reverse current through a conventional regulator. The MAX38902E includes a reverse voltage detector that trips when IN drops 10mV below OUT, shutting off the regulator and opening the PMOS body diode connection, preventing any reverse current.

Output Voltage Configuration

The MAX38902E uses external feedback resistors to set the output regulation voltage, as shown in the *Typical Operating Circuit*. The output can be set from 0.8V to 5.0V. Set the lower feedback resistor R2 to 300kΩ or less to minimize FB input bias current error. Then, calculate the value of the upper feedback resistor R3 as follows:

$$R3 \ = \ R2 \ \text{x} \ \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V$_{FB}$ is the feedback regulation voltage of 0.6V. To set the output voltage to 2.5V, for example, R3 should be:

$$R3 \ = \ 300\text{k}\Omega \ \text{x} \ \left(\frac{2.5V}{0.6V} - 1 \right)$$

Power-OK

The MAX38902E includes an additional open-drain output, $\overline{POK}$, that goes low to indicate the output voltage is in regulation. Connect a pullup resistor from this pin to an external supply. During startup, $\overline{POK}$ stays high until the output voltage rises to 91%(typ) of its regulation level. If an overload occurs at the output, or the output is shutdown, $\overline{POK}$ goes high.

Input Capacitor

A 10µF ceramic capacitor is recommended for the input. Select a capacitor that maintains its capacitance over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

Output Capacitor

A minimum of 4µF capacitance is required at OUT to ensure stability. Select a ceramic capacitor that maintains its capacitance (4µF minimum) over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

Thermal Considerations

The MAX38902E is packaged in an 8-pin 2mm x 2mm TDFN package with an exposed paddle. The exposed paddle is the main path for heat to leave the IC, and therefore must be connected to a ground plane with thermal vias to allow heat to dissipate from the device. Thermal properties of the IC package are given in the *Package Information* section.

Ordering Information

Part Number	Temperature Range	Pin-Package	Output Voltage Setting
MAX38902EATA+	-40°C to +125°C	8 TDFN	External Resistor Feedback with $\overline{POK}$ output

+*Denotes a lead(Pb)-free/RoHS-compliant package.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—
1	1/19	Updated *Typical Operating Circuit*, *Absolute Maximum Ratings*, *Electrical Characteristics, Pin Configuration, Pin Description*, and *Functional Diagram*	1–3, 5, 6