LM3528 High Efficiency, Multi Display LED Driver with 128 Exponential Dimming Steps and Integrated OLED Power Supply in a 1.2mm × 1.6mm DSBGA Package

Check for Samples: LM3528

FEATURES

- **128 Exponential Dimming Steps**
- **Programmable Auto-Dimming Function**
- **Up to 90% Efficient**
- **Low Profile 12 Bump DSBGA Package (1.2mm x 1.6mm x 0.6mm)**
- **Integrated OLED Display Power Supply and LED Driver**
- **Programmable Pattern Generator Output for LED Indicator Function**
- **Drives up to 12 LED's at 20mA**
- **Drives up to 5 LED's at 20mA and delivers 18V at 40mA**
- **1% Accurate Current Matching Between Strings**
- **Internal Soft-Start Limits Inrush Current**
- **True Shutdown Isolation for LED's**
- **Wide 2.5V to 5.5V Input Voltage Range**
- **22V Over-Voltage Protection**
- **1.25MHz Fixed Frequency Operation**
- **Dedicated Programmable General Purpose I/O**
- **Active Low Hardware Reset**

APPLICATIONS

- **Dual Display LCD Backlighting for Portable Applications**
- **Large Format LCD Backlighting**
- **OLED Panel Power Supply**
- **Display Backlighting with Indicator Light**

DESCRIPTION

The LM3528 current mode boost converter offers two separate outputs. The first output (MAIN) is a constant current sink for driving series white LED's. The second output (SUB/FB) is configurable as a constant current sink for series white LED bias, or as a feedback pin to set a constant output voltage for powering OLED panels.

As a dual output white LED bias supply, the LM3528 adaptively regulates the supply voltage of the LED strings to maximize efficiency and insure the current sinks remain in regulation. The maximum current per output is set via a single external low power resistor. An I^{2}C compatible interface allows for independent adjustment of the LED current in either output from 0 to max current in 128 exponential steps. When configured as a white LED + OLED bias supply the LM3528 can independently and simultaneously drive a string of up to 6 white LED's and deliver a constant output voltage of up to 21V for OLED panels.

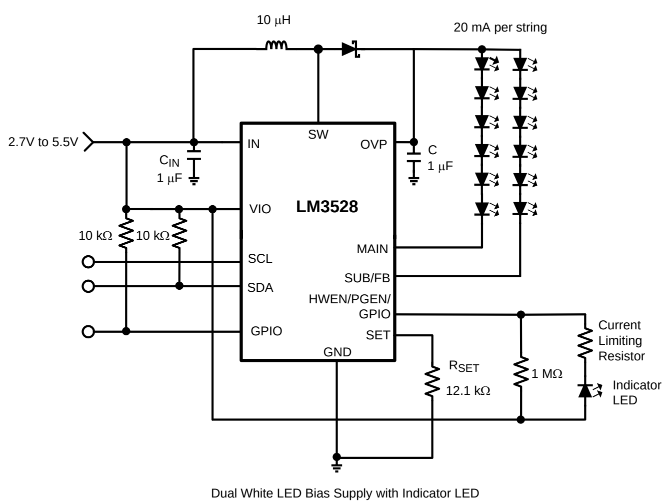


Figure 1. Typical Application Circuit

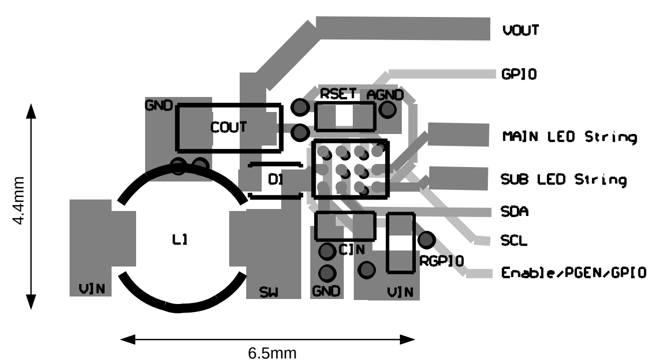


Figure 2. Typical PCB Layout

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Output over-voltage protection shuts down the device if V_{OUT} rises above 22V allowing for the use of small sized low voltage output capacitors. Other features include a dedicated general purpose I/O (GPIO) and a multi-function pin (HWEN/PGEN/GPIO) which can be configured as a 32 bit pattern generator, a hardware enable input, or as a GPIO. When configured as a pattern generator, an arbitrary pattern is programmed via the I^2C compatible interface and output at HWEN/PGEN/GPIO for indicator LED flashing or for external logic control. The LM3528 is offered in a tiny 12-bump DSBGA package and operates over the -40°C to +85°C temperature range.

Connection Diagram

Top View

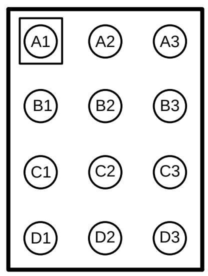


Figure 3. 12-Bump (1.215mm × 1.615mm × 0.6mm) YFQ0012

PIN DESCRIPTIONS

Pin	Name	Function
A1	OVP	Over-Voltage Protection Sense Connection. Connect OVP to the positive terminal of the output capacitor.
A2	MAIN	Main Current Sink Input.
A3	SUB/FB	Secondary Current Sink Input or 1.21V Feedback Connection for Constant Voltage Output.
B1	GPIO1	Programmable General Purpose I/O.
B2	SCL	Serial Clock Input
B3	SET	LED Current Setting Connection. Connect a resistor from SET to GND to set the maximum LED current into MAIN or SUB/FB (when in LED mode), where $I_{LED\_MAX} = 192 \times 1.244V/R_{SET}$.
C1	HWEN/PGEN/GPIO	Active High Hardware Enable Input. Programmable Pattern Generator Output, and Programmable General Purpose I/O.
C2	SDA	Serial Data Input/Output
C3	IN	Input Voltage Connection. Connect IN to the input supply, and bypass to GND with a 1µF ceramic capacitor.
D1	VIO	Logic Voltage Level Input
D2	SW	Drain Connection for Internal NMOS Switch
D3	GND	Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2][3]

V_{IN}	−0.3V to 6V
V_{SW}, V_{OVP},	−0.3V to 25V
$V_{SUB/FB}$, V_{MAIN}	−0.3V to 23V
V_{SCL}, V_{SDA}, $V_{\overline{RESET}\backslash GPIO}$, V_{IO} , V_{SET}	−0.3V to 6V
Continuous Power Dissipation	Internally Limited
Junction Temperature ($T_{J\text{-}MAX}$)	+150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering, 10s) [4]	+300°C
ESD Rating [5] Human Body Model	2.5kV

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin.
(4) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: DSBGA Wafer LEvel Chip Scale Package (SNVA009).
(5) The human body model is a 100pF capacitor discharged through 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7).

Operating Ratings [1][2]

V_{IN}	2.5V to 5.5V
V_{SW}, V_{OVP},	0V to 23V
$V_{SUB/FB}$, V_{MAIN}	0V to 21V
Junction Temperature Range (T_J) [3]	-40°C to +110°C
Ambient Temperature Range (T_A) [4]	-40°C to +85°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=+150°C (typ.) and disengages at T_J=+140°C (typ.).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature (TJ-MAX-OP = +105°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$.

Thermal Properties

Junction to Ambient Thermal Resistance (θ_{JA}) [1]	68°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 114.3mm x 76.2mm x 1.6mm. The ground plane on the board is 113mm x 75mm. Thickness of copper layers are 71.5µm/35µm/35µm/71.5µm (2oz/1oz/1oz/2oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W. For more information on these topics, please refer to Texas Instruments Application Note 1112 SNVA009, and JEDEC Standard JESD51-7.

Electrical Characteristics

Specifications in standard type face are for T_A = 25°C and those in **boldface type** apply over the Operating Temperature Range of T_A = −40°C to +85°C. Unless otherwise specified V_{IN} = 3.6V, V_{IO} = 1.8V, $V_{\overline{RESET}/GPIO} = V_{IN}$, $V_{SUB/FB} = V_{MAIN}$ = 0.5V, R_{SET} = 12.0kΩ, OLED = ‘0’, ENM = ENS = ‘1’, BSUB = BMAIN = Full Scale. [1] [2]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LED}	Output Current Regulation MAIN or SUB/FB Enabled	UNI = ‘0’, or ‘1’, 2.5V < V_{IN} < 5.5V	**18.5**	20	**22**	
	Maximum Current Per Current Sink	R_{SET} = 8.0kΩ		30		mA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but represent the most likely norm.

Electrical Characteristics (continued)

Specifications in standard type face are for T_A = 25°C and those in **boldface type** apply over the Operating Temperature Range of T_A = −40°C to +85°C. Unless otherwise specified V_{IN} = 3.6V, V_{IO} = 1.8V, $V_{\overline{RESET}/GPIO} = V_{IN}$, $V_{SUB/FB} = V_{MAIN}$ = 0.5V, R_{SET} = 12.0kΩ, OLED = '0', ENM = ENS = '1', BSUB = BMAIN = Full Scale.(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{LED\text{-}MATCH}$	I_{MAIN} to $I_{SUB/FB}$ Current Matching	UNI = '1', 2.5V < V_{IN} < 5.5V (3)		0.15	**1**	%
V_{SET}	SET Pin Voltage	3.0V < V_{IN} < 5V		1.244		V
I_{LED}/I_{SET}	I_{LED} Current to I_{SET} Current Ratio			192		
V_{REG_CS}	Regulated Current Sink Headroom Voltage			500		mV
V_{REG_OLED}	$V_{SUB/FB}$ Regulation Voltage in OLED Mode	2.5V < V_{IN} < 5.5V, OLED = '1'	**1.170**	1.21	**1.237**	V
V_{HR}	Current Sink Minimum Headroom Voltage	I_{LED} = 95% of nominal		300		mV
R_{DSON}	NMOS Switch On Resistance	I_{SW} = 100mA		0.43		Ω
I_{CL}	NMOS Switch Current Limit	2.5V < V_{IN} < 5.5V	**645**	770	**900**	mA
V_{OVP}	Output Over-Voltage Protection	ON Threshold, 2.5V < V_{IN} < 5.5V	**20.6**	22	**23**	V
		OFF Threshold, 2.7V < V_{IN} < 5.5V	**19.25**	20.6	**21.5**	
f_{SW}	Switching Frequency		**1.0**	1.27	**1.4**	MHz
D_{MAX}	Maximum Duty Cycle			90		%
D_{MIN}	Minimum Duty Cycle			10		%
I_Q	Quiescent Current, Device Not Switching	V_{MAIN} and $V_{SUB/FB}$ > V_{REG_CS}, BSUB = BMAIN = 0x00, 2.5V < V_{IN} < 5.5V		350	**390**	µA
		$V_{SUB/FB}$ > V_{REG_OLED}, OLED='1', ENM=ENS='0', R_{SET} Open, 2.5V < V_{IN} < 5.5V		250	**260**	
I_{SHDN}	Shutdown Current	ENM = ENS = OLED = '0', 2.5V < V_{IN} < 5.5V		1.8	**3**	µA
HWEN/PGEN/GPIO, GPIO1 Pin Voltage Specifications						
V_{IL}	Input Logic Low	2.5V < V_{IN} <5.5V, MODE bit = 0			**0.5**	V
V_{IH}	Input Logic High	2.5V < V_{IN} < 5.5V, MODE bit = 0	**1.1**			V
V_{OL}	Output Logic Low	I_{LOAD}=3mA, MODE bit = 1			**400**	mV
I^2C Compatible Voltage Specifications (SCL, SDA, VIO)						
V_{IO}	Serial Bus Voltage Level	2.5V < V_{IN} < 5.5V (4)	**1.7**		**V_{IN}**	V
V_{IL}	Input Logic Low	2.5V < V_{IN} < 5.5V			**0.36×V_{IO}**	V
V_{IH}	Input Logic High	2.5V < V_{IN} < 5.5V	**0.7×V_{IO}**			V
V_{OL}	Output Logic Low	I_{LOAD} = 3mA			**400**	mV
I^2C Compatible Timing Specifications (SCL, SDA, VIO, see Figure 4) (5)(4)						
t_1	SCL Clock Period		**2.5**			µs
t_2	Data In Setup Time to SCL High		**100**			ns
t_3	Data Out Stable After SCL Low		**0**			ns

(3) The matching specification between MAIN and SUB is calculated as 100 × ((I_{MAIN} or I_{SUB}) - I_{AVE}) / I_{AVE}. This simplifies out to be 100 × (I_{MAIN} - I_{SUB})/(I_{MAIN} + I_{SUB}).
(4) SCL and SDA signals are referenced to VIO and GND for minimum VIO voltage testing. VIO limits indicate the minimum voltage at VIO at which the part is operational.
(5) SCL and SDA must be glitch-free in order for proper brightness control to be realized.

Electrical Characteristics (continued)

Specifications in standard type face are for T_A = 25°C and those in **boldface type** apply over the Operating Temperature Range of T_A = −40°C to +85°C. Unless otherwise specified V_{IN} = 3.6V, V_{IO} = 1.8V, $V_{\overline{RESET}/GPIO}$ = V_{IN}, $V_{SUB/FB}$ = V_{MAIN} = 0.5V, R_{SET} = 12.0kΩ, OLED = '0', ENM = ENS = '1', BSUB = BMAIN = Full Scale.(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_4	SDA Low Setup Time to SCL Low (Start)		**100**			ns
t_5	SDA High Hold Time After SCL High (Stop)		**100**			ns

Timing Diagram

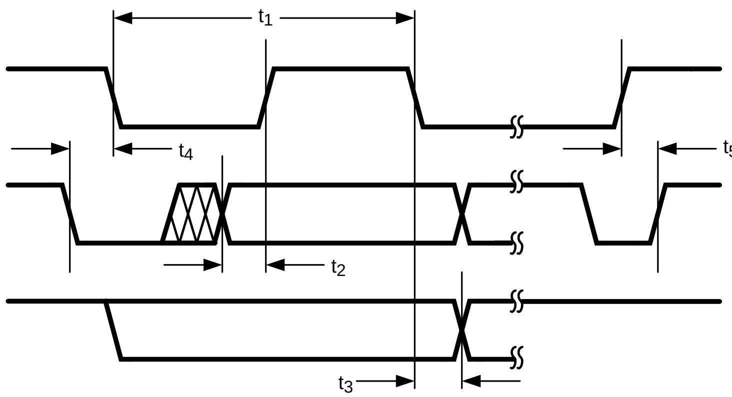


Figure 4. I²C Timing

Typical Performance Characteristics

V_{IN} = 3.6V, LEDs are Nichia (NSSW008C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 12.1kΩ, UNI = '1', $I_{LED} = I_{SUB} + I_{MAIN}$, T_A = +25°C unless otherwise specified.

2x6 LED Efficiency vs I_{LED} (2 Strings of 6LEDs)

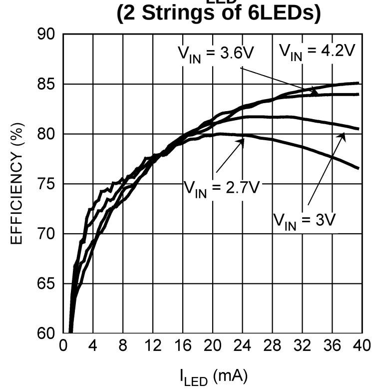


Figure 5.

2x5 LED Efficiency vs I_{LED} (2 Strings of 5LEDs)

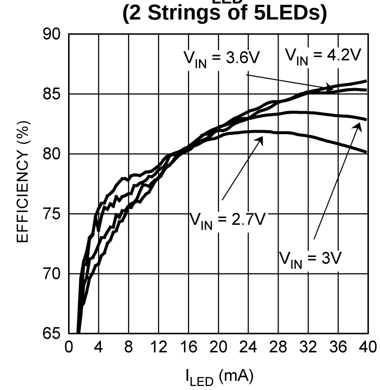


Figure 6.

2x4 LED Efficiency vs I_{LED} (2 Strings of 4LEDs)

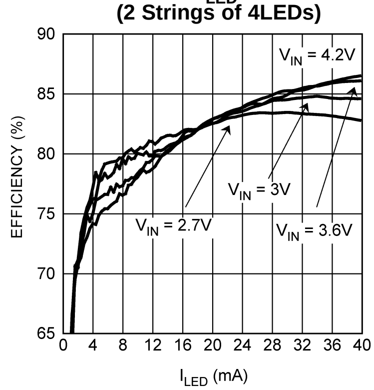


Figure 7.

2x3 LED Efficiency vs I_{LED} (2 Strings of 3LEDs)

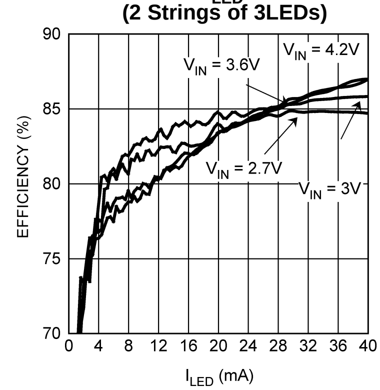


Figure 8.

2x2 LED Efficiency vs I_{LED} (2 Strings of 2LEDs)

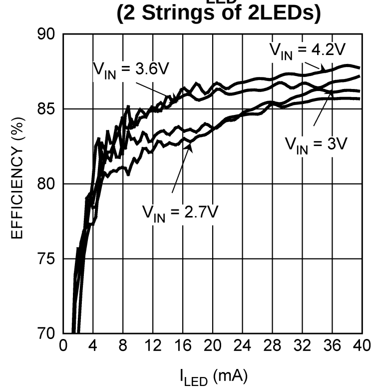


Figure 9.

LED Efficiency vs V_{IN} (L = TDK VLF3012AT-100MR92, R_L = 0.36Ω, $I_{SUB} + I_{MAIN}$ = 40mA)

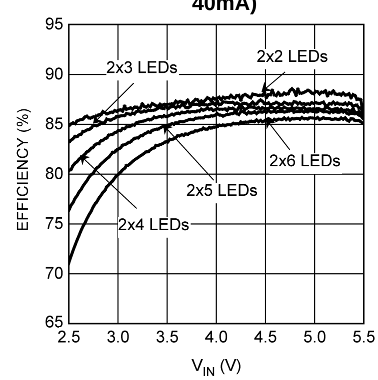


Figure 10.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are Nichia (NSSW008C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 12.1kΩ, UNI = '1', I_{LED} = I_{SUB} + I_{MAIN}, T_A = +25°C unless otherwise specified.

18V OLED Efficiency vs I_{OUT}

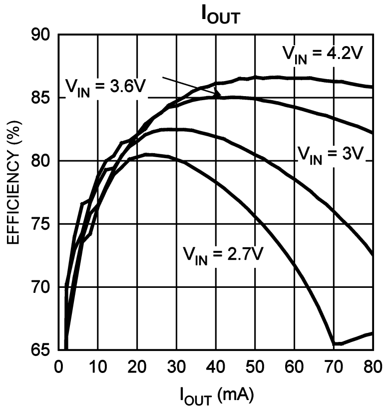


Figure 11.

12V OLED Efficiency vs I_{OUT}

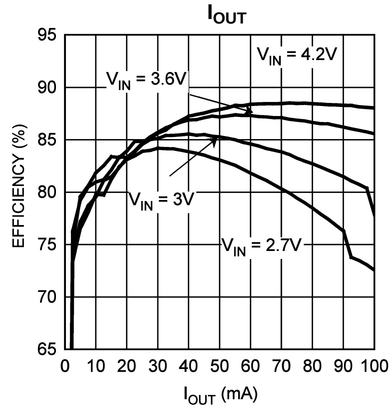


Figure 12.

LED Line Regulation (UNI = '0')

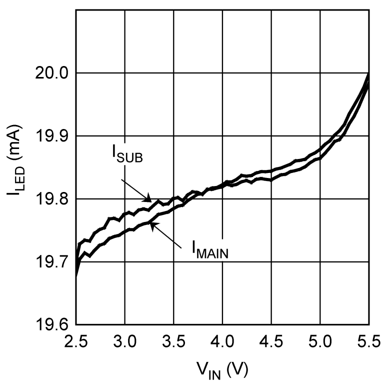


Figure 13.

OLED Line Regulation I_{OLED} = 60mA

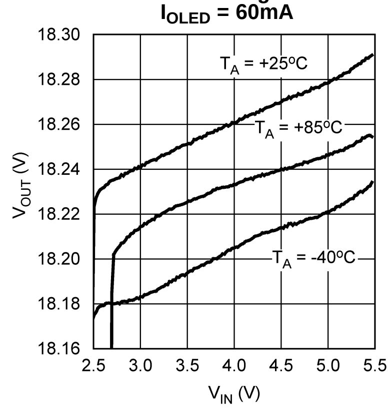


Figure 14.

OLED Line Regulation I_{OLED} = 60mA

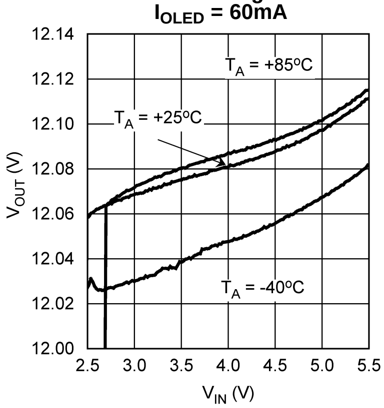


Figure 15.

OLED Load Regulation V_{OLED} = 18V

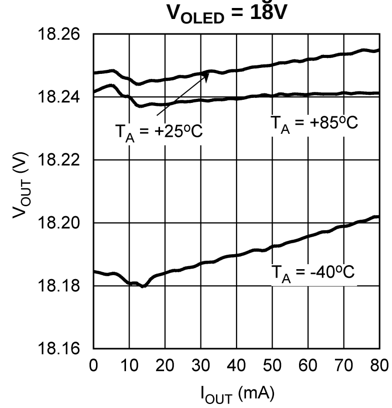


Figure 16.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are Nichia (NSSW008C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 12.1kΩ, UNI = '1', I_{LED} = I_{SUB} + I_{MAIN}, T_A = +25°C unless otherwise specified.

OLED Load Regulation
V_{OLED} = 12V

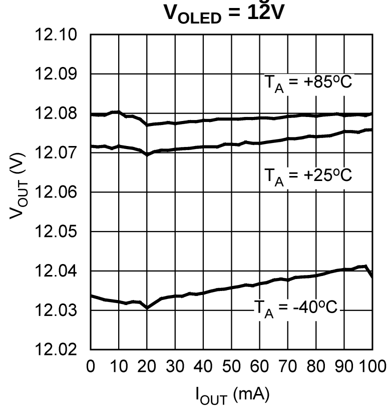


Figure 17.

Peak Current Limit vs. V_{IN}

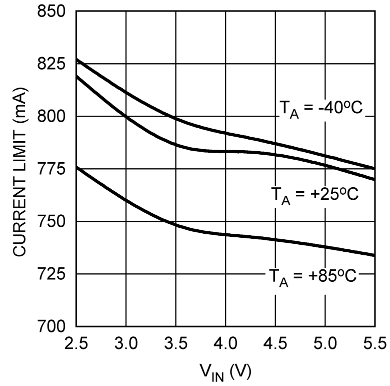


Figure 18.

Over Voltage Limit vs. V_{IN}

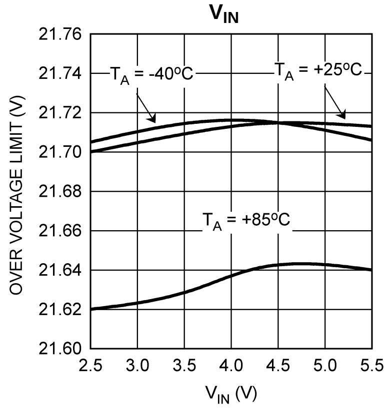


Figure 19.

Switch On-Resistance vs. V_{IN}

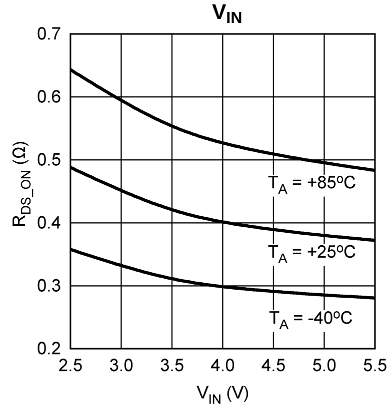


Figure 20.

Switching Frequency vs. V_{IN}

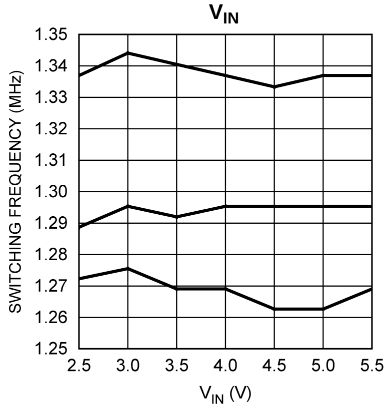


Figure 21.

Maximum Duty Cycle vs. V_{IN}

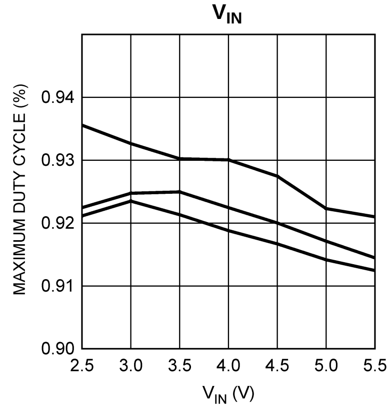


Figure 22.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are Nichia (NSSW008C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 12.1kΩ, UNI = '1', I_{LED} = I_{SUB} + I_{MAIN}, T_A = +25°C unless otherwise specified.

Shutdown Current vs. V_{IN}

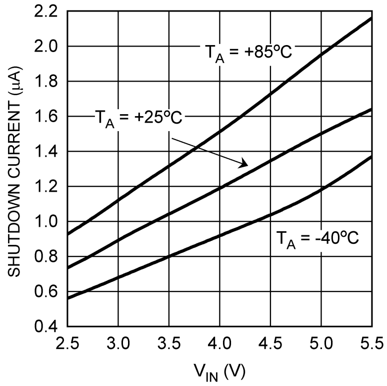


Figure 23.

Switching Supply Current vs. V_{IN}

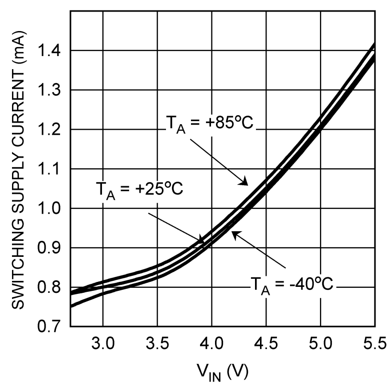


Figure 24.

LED Current Matching vs. CODE[(1)] (UNI = '1', R_{SET} = 12kΩ, T_A = -40°C to +85°C)

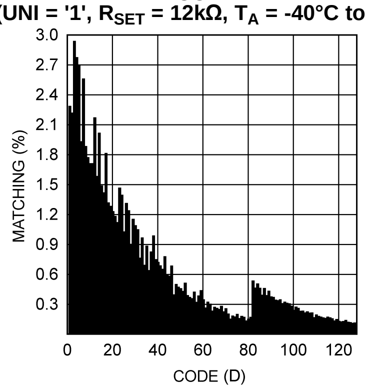


Figure 25.

LED Current Accuracy vs CODE (R_{SET} = 12kΩ±0.05%)

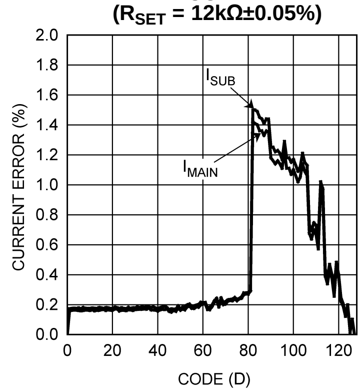


Figure 26.

LED Current vs CODE (I_{MAIN}, I_{SUB}, I_{IDEAL}, R_{SET} = 12kΩ±0.05%)

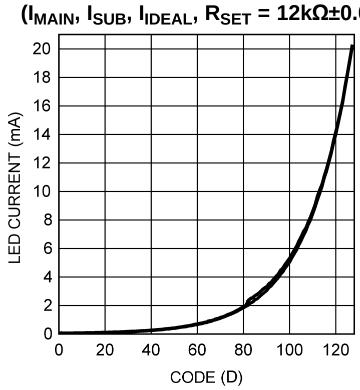


Figure 27.

I_{LED} vs Current Source Headroom Voltage (V_{IN} = 3V, UNI = '0')

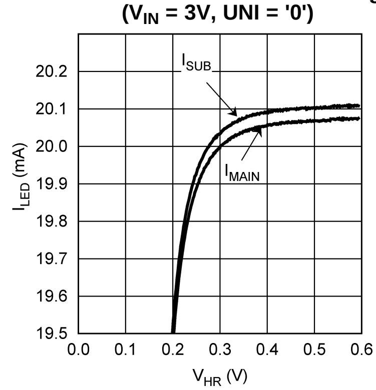


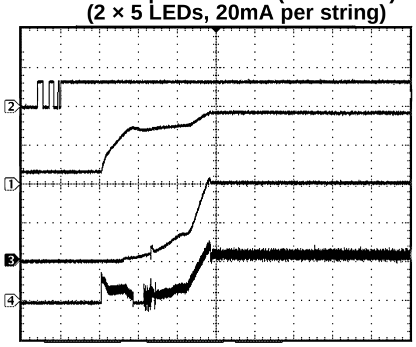
Figure 28.

(1) The matching specification between MAIN and SUB is calculated as 100 × ((I_{MAIN} or I_{SUB}) - I_{AVE}) / I_{AVE}. This simplifies out to be 100 × (I_{MAIN} - I_{SUB})/(I_{MAIN} + I_{SUB}).

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are Nichia (NSSW008C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 12.1kΩ, UNI = '1', I_{LED} = I_{SUB} + I_{MAIN}, T_A = +25°C unless otherwise specified.

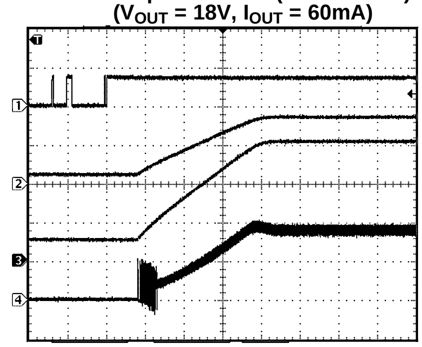
Start-Up Waveform (LED Mode)
(2 × 5 LEDs, 20mA per string)



Channel 2: SDA (5V/div)
Channel 1: V_{OUT} (10V/div)
Channel 3: I_{LED} (20mA/div)
Channel 4: I_{IN} (200mA/div)
Time Base: 400µs/div

Figure 29.

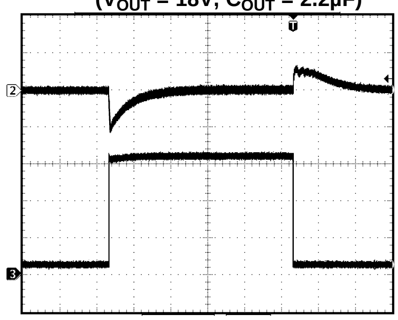
Start-Up Waveform (OLED Mode)
(V_{OUT} = 18V, I_{OUT} = 60mA)



Channel 1: SDA (5V/div)
Channel 2: V_{OUT} (10V/div)
Channel 3: I_{OUT} (20mA/div)
Channel 4: I_{IN} (200mA/div)
Time Base: 400µs/div

Figure 30.

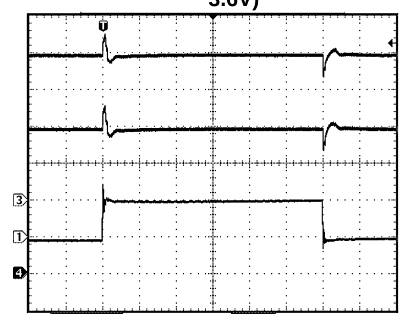
Load Step (OLED Mode)
(V_{OUT} = 18V, C_{OUT} = 2.2µF)



Channel 2: V_{OUT} (AC Coupled, 500mV/div)
Channel 3: I_{OUT} (20mA/div)
Time Base: 200µs/div

Figure 31.

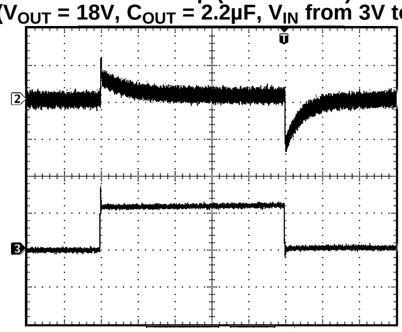
Line Step (LED Mode)
(2 × 5 LEDs, 20mA per String, C_{OUT} = 1µF, V_{IN} from 3V to 3.6V)



Channel 3: ISUB (5mA/div)
Channel 4: IMAIN (5mA/div)
Channel 2: V_{IN} (AC Coupled, 500mV/div)
Time Base: 100µs/div

Figure 32.

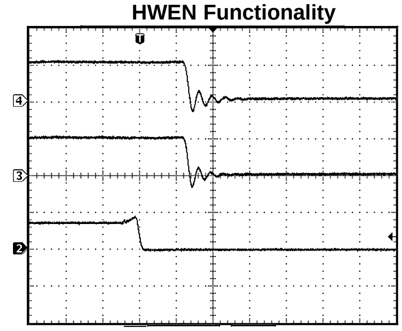
Line Step (OLED Mode)
(V_{OUT} = 18V, C_{OUT} = 2.2µF, V_{IN} from 3V to 3.6V)



Channel 2: VOUT (AC Coupled, 100mV/div)
Channel 3: VIN (AC Coupled, 500mV/div)
Time Base: 200µs/div

Figure 33.

HWEN Functionality



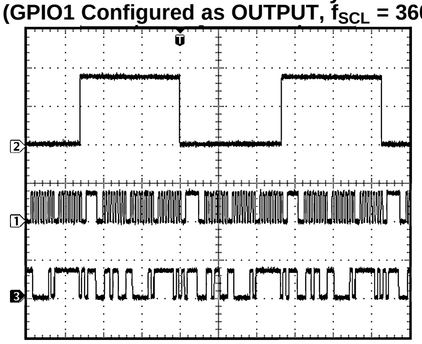
Channel 4: I_{SUB} (20mA/div)
Channel 3: I_{MAIN} (20mA/div)
Channel 2: HWEN (5V/div)
Time Base: 200ns/div

Figure 34.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are Nichia (NSSW008C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 12.1kΩ, UNI = '1', I_{LED} = I_{SUB} + I_{MAIN}, T_A = +25°C unless otherwise specified.

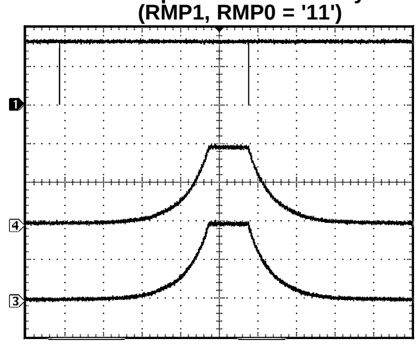
GPIO1 Functionality
(GPIO1 Configured as OUTPUT, f_{SCL} = 360kHz)



Channel 2: GPIO (2V/div)
Channel 1: SCL (5V/div)
Channel 1:SDA (5V/div)
Time Base: 40µs/div

Figure 35.

Ramp Rate Functionality
(RMP1, RMP0 = '11')



Channel 1:SDA (2V/div)
Channel 4: I_{SUB} (10mA/div)
Channel 3: ISUB (10mA/div)
Time Base: 400ms/div

Figure 36.

BLOCK DIAGRAM

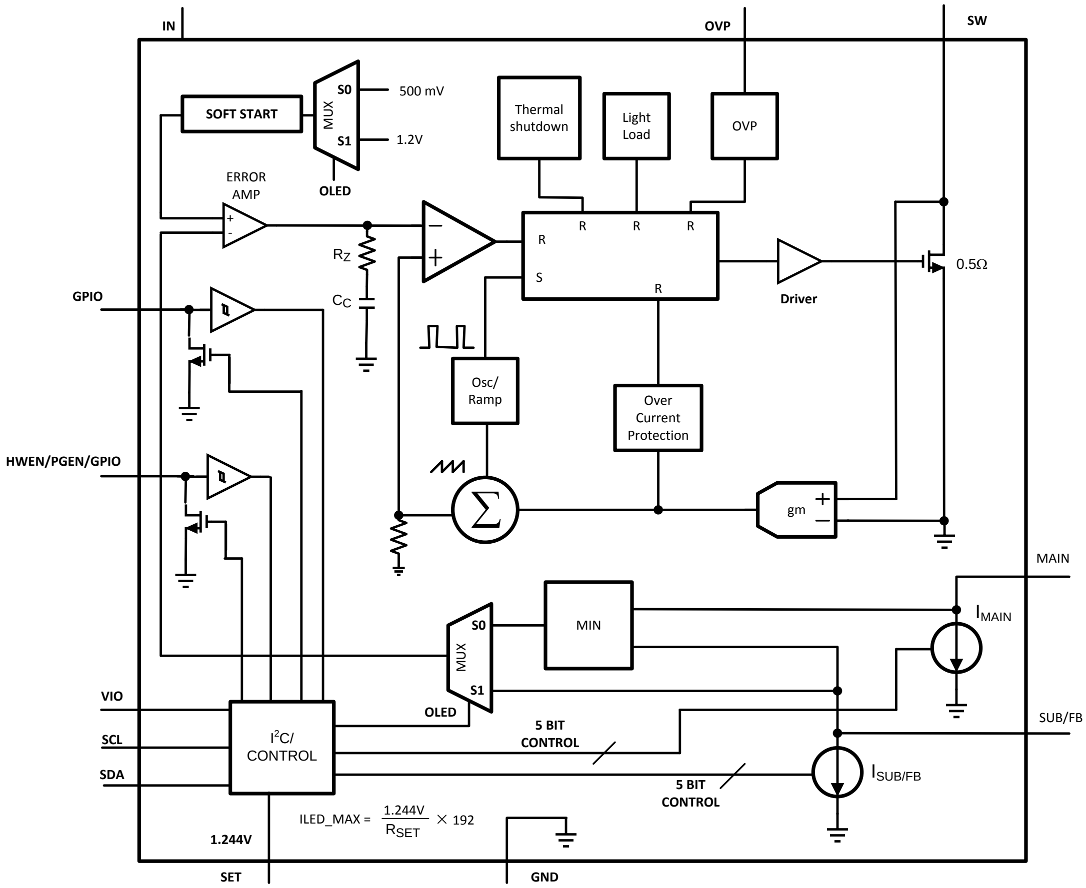


Figure 37. LM3528 Block Diagram

OPERATION DESCRIPTION

The LM3528 Current Mode PWM boost converter operates from a 2.7V to 5.5V input and provides two regulated outputs for White LED and OLED display biasing. The first output, MAIN, provides a constant current of up to 30mA to bias up to 6 series white LED's. The second output, SUB/FB, can be configured as a current source for up to 6 series white LED's at up to 30mA, or as a feedback voltage pin to regulate a constant output voltage of up to 21V. When both MAIN and SUB/FB are configured for white LED bias the current for each LED string is controlled independently or in unison via an I^2C-compatible interface. When MAIN is configured for white LED bias and SUB/FB is configured as a feedback voltage pin, the current into MAIN is controlled via the I^2C-compatible interface and SUB/FB becomes the middle tap of a resistive divider used to regulate the output voltage of the boost converter.

The core of the LM3528 is a Current Mode Boost converter. Operation is as follows. At the start of each switching cycle the internal oscillator sets the PWM converter. The converter turns the NMOS switch on, allowing the inductor current to ramp while the output capacitor supplies power to the white LED's and/or OLED panel. The error signal at the output of the error amplifier is compared against the sensed inductor current. When the sensed inductor current equals the error signal, or when the maximum duty cycle is reached, the NMOS switch turns off causing the external Schottky diode to pick up the inductor current. This allows the inductor current to ramp down causing its stored energy to charge the output capacitor and supply power to the load. At the end of the clock period the PWM controller is again set and the process repeats itself.

Adaptive Regulation

When biasing dual white led strings (White LED mode) the LM3528 maximizes efficiency by adaptively regulating the output voltage. In this configuration the 500mV reference is connected to the non-inverting input of the error amplifier via mux S2 (see Figure 37). The lowest of either V_{MAIN} or $V_{SUB/FB}$ is then applied to the inverting input of the error amplifier via mux S1. This ensures that V_{MAIN} and $V_{SUB/FB}$ are at least 500mV, thus providing enough voltage headroom at the input to the current sinks for proper current regulation.

In the instance when there are unequal numbers of LEDs or unequal currents from string to string, the string with the highest voltage will be the regulation point.

Unison/Non-Unison Mode

Within White LED mode there are two separate modes of operation, Unison and Non-Unison. Non-Unison mode provides for independent current regulation, while Unison mode gives up independent regulation for more accurate matching between LED strings. When in Non-Unison mode the LED currents I_{MAIN} and $I_{SUB/FB}$ are independently controlled via registers BMAIN and BSUB respectively (see Brightness Registers (BMAIN and BSUB) section). When in Unison mode BSUB is disabled and both I_{MAIN} and $I_{SUB/FB}$ are controlled via BMAIN only.

Start-Up

The LM3528 features an internal soft-start, preventing large inrush currents during start-up that can cause excessive voltage ripple on the input. For the typical application circuits when the device is brought out of shutdown the average input current ramps from zero to 450mA in approximately 1.2ms. See Start Up Plots in the Typical Performance Characteristics.

OLED Mode

When the LM3528 is configured for a single White LED bias + OLED display bias (OLED mode), the non-inverting input of the error amplifier is connected to the internal 1.21V reference via MUX S2. MUX S1 switches SUB/FB to the inverting input of the error amplifier while disconnecting the internal current sink at SUB/FB. The voltage at MAIN is not regulated in OLED mode so when the application requires white LED + OLED panel biasing, ensure that at least 300mV of headroom is maintained at MAIN to ensure proper regulation of I_{MAIN}. (see the Typical Performance Characteristics for a plot of I_{LED} vs Current Source Headroom Voltage)

Peak Current Limit

The LM3528's boost converter has a peak current limit for the internal power switch of 770mA typical (650mA minimum). When the peak switch current reaches the current limit the duty cycle is terminated resulting in a limit on the maximum output current and thus the maximum output power the LM3528 can deliver. Calculate the maximum LED current as a function of V_{IN}, V_{OUT}, L and I_{PEAK} as:

$$I_{OUT\_MAX} = \frac{(I_{PEAK} - \Delta I_L) \times \eta \times V_{IN}}{V_{OUT}}$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{1}$$

f_{SW} = 1.27MHz. Typical values for efficiency and I_{PEAK} can be found in the efficiency and I_{PEAK} curves in the Typical Performance Characteristics.

Over Voltage Protection

The LM3528's output voltage (V_{OUT}) is limited on the high end by the Output Over-Voltage Protection Threshold (V_{OVP}) of 21.2V (min). In White LED mode during output open circuit conditions the output voltage will rise to the over voltage protection threshold. When this happens the controller will stop switching causing V_{OUT} to droop. When the output voltage drops below 19.7V (min) the device will resume switching. If the device remains in an over voltage condition the LM3528 will repeat the cycle causing the output to cycle between the high and low OVP thresholds. See waveform for OVP condition in the Typical Performance Characteristics.

Output Current Accuracy and Current Matching

The LM3528 provides both precise current accuracy (% error from ideal value) and accurate current matching between the MAIN and SUB/FB current sinks. Two modes of operation affect the current matching between I_{MAIN} and $I_{SUB/FB}$. The first mode (Non-Unison mode) is set by writing a 0 to bit 2 of the General Purpose register (UNI bit). Non-Unison mode allows for independent programming of I_{MAIN} and $I_{SUB/FB}$ via registers BMAIN and BSUB respectively. In this mode typical matching between current sinks is 1%.

Writing a 1 to UNI configures the device for Unison mode. In Unison mode, BSUB is disabled and I_{MAIN} and $I_{SUB/FB}$ are both controlled via register BMAIN. In this mode typical matching is 0.15%.

Light Load Operation

The LM3528 boost converter operates in three modes; continuous conduction, discontinuous conduction, and skip mode operation. Under heavy loads when the inductor current does not reach zero before the end of the switching period the device switches at a constant frequency. As the output current decreases and the inductor current reaches zero before the end of the switching cycle, the device operates in discontinuous conduction. At very light loads the LM3528 will enter skip mode operation causing the switching period to lengthen and the device to only switch as required to maintain regulation at the output.

Hardware Enable/Pattern Generator/General Purpose I/O (HWEN/PGEN/GPIO)

HWEN/PGEN/GPIO can be configured for three different modes of operation; Hardware Enable, Pattern Generation, and General Purpose I/O. Register HPG at address 0x80 controls the functionality of this pin (see Table 6).

Hardware Enable (HWEN)

On initial power-up HWEN/PGEN/GPIO defaults to the Hardware Enable (HWEN) state. In this mode HWEN/PGEN/GPIO is an active high open-drain input enable to the device. When in HWEN mode HWEN/PGEN/GPIO must be pulled up to at least 0.7 × VIO to enable the device. In HWEN mode pulling HWEN/PGEN/GPIO below 0.36 × VIO will shutdown the LM3528, resetting all registers, and forcing MAIN, SUB/FB, and SW high impedance. Bit 0 of the HPG register controls the HWEN function. Writing a ‘0’ to this bit enables the HWEN mode. Writing a ‘1’ to this bit disables the HWEN mode and allows selection between the other two modes.

Pattern Generator (PGEN)

With bit 0 of the HPG register set to 1, HWEN/PGEN/GPIO can be programmed as an open drain Pattern Generator Output (PGEN). In PGEN mode a 32 bit pattern is output at HWEN/PGEN/GPIO. This pattern can be programmed to repeat itself at 4 different frequencies and 6 different duty cycles. The arbitrary pattern is programmed into four 8 bit registers; PGEN0 (address 0x90), PGEN1 (address 0x91), PGEN2 (address 0x92), and PGEN3 (address 0x93) (see Figure 47 - Figure 50). Figure 51 details an example of a 32 bit pattern at a specific programmed duty cycle and frequency. A ‘1’ written to the PGEN_ registers forces HWEN/PGEN/GPIO low. A ‘0’ causes HWEN/PGEN/GPIO to go open drain.

Bits <5:3> in the HPG register have three functions; GPIO enable, duty cycle select, and pattern latch. Any combination of these bits other than ‘000’ or ’111’ puts HWEN/PGEN/GPIO into PGEN mode at the specified duty cycle shown in Table 6. Writing a ‘111’ to bits <5:3> latches the 32 bit pattern programmed into the 4 pattern generator registers PGEN0, PGEN1, PGEN2, PGEN3 into the internal shift register. When bits <5:3> = ‘000’ the PGEN mode is off and HWEN/PGEN/GPIO is configured as a GPIO.

Bits <7:6> of the HPG register control the pattern frequency. See Table 6 for the detailed breakdown of each available frequency. Figure 51 details the pattern programming and Figure 52 shows the pattern output at HWEN/PGEN/GPIO.

General Purpose I/O (GPIO1)

With bits <5:3> and bit 0 of the HPG register all set to ‘0’ HWEN/PGEN/GPIO functions as an open drain General Purpose I/O. In this mode, bit 1 of the HPG register controls the logic direction (Input or Output) and bit 2 holds the logic data. With bit 1 set to ‘0’ HWEN/PGEN/GPIO is configured as an output. In this mode a ‘0’ written to bit 2 forces HWEN/PGEN/GPIO to logic low. Likewise, a ‘1’ written to bit 2 will force HWEN/PGEN/GPIO open drain. When bit 1 is set to ‘1’ HWEN/PGEN/GPIO is configured as a logic input. In this mode when HWEN/PGEN/GPIO is externally pulled low a ‘0’ is written to bit 2 of the HPG register. Likewise, when HWEN/PGEN/GPIO is externally pulled high a ‘1’ is written to bit 2 of the HPG register. Table 6 and Figure 45 detail the bit functions of the HPG register and their power-on-reset values. Note that the logic output levels for the GPIO function of this pin are inverted compared to the PGEN functions. For example, a 1 written to the PGEN registers cause the HWEN/PGEN/GPIO pin to pull low while a 1 written to bit 2 of the HPG register causes the pin to go open drain.

General Purpose I/O (GPIO0)

The GPIO pin is a dedicated General Purpose I/O (open drain) and is controlled via the GPIO register at address 0x81. Bit 1 holds the logic data while bit 0 controls the logic direction (Input or Output). Bits <7:2> are un-used and will always read back as logic '1'. With bit 0 set to ‘0’ GPIO is configured as an output. In this mode a ‘0’ written to bit 1 forces GPIO to a logic low. Likewise, a ‘1’ written to bit 1 will force GPIO to logic high. When bit 0 is set to ‘1’ GPIO is configured as a logic input. In this mode when GPIO is externally pulled low a ‘0’ is written to bit 1 of the GPIO register. Likewise, when GPIO is externally pulled high a ‘1’ is written to bit 2 of the HPG register. Table 8 and Figure 46 detail the bit functions and power-on-reset values of GPIO.

During an initial GPIO write two I2C sequences (Slave I.D, Register Address, Register Data) are required to change the state of the GPIO pin. The first write configures the GPIO pin as an output. The second write will change the state of the GPIO output to the desired logic '1' or '0'.

Thermal Shutdown

The LM3528 offers a thermal shutdown protection. When the die temperature reaches +140°C the device will shutdown and not turn on again until the die temperature falls below +120°C.

I²C Compatible Interface

The LM3528 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. A START and a repeated START conditions are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

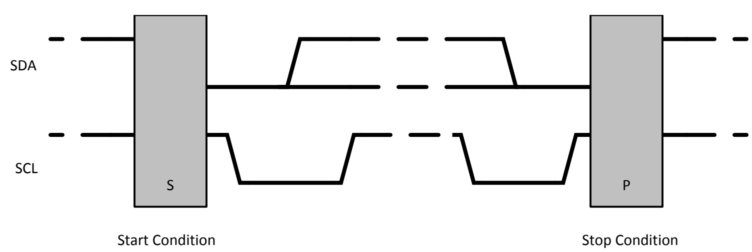


Figure 38. Start and Stop Sequences

I²C Compatible Address

The chip address for the LM3528 is 0110110 (36h). After the START condition, the I²C master sends the 7-bit chip address followed by a read or write bit (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data will be written. The third byte contains the data for the selected register.

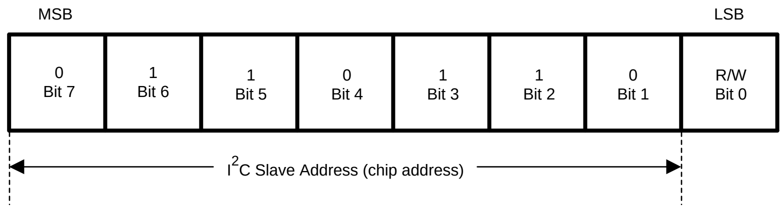


Figure 39. Chip Address

Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3528 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received. Figure 40 is an example of a write sequence to the General Purpose register of the LM3528.

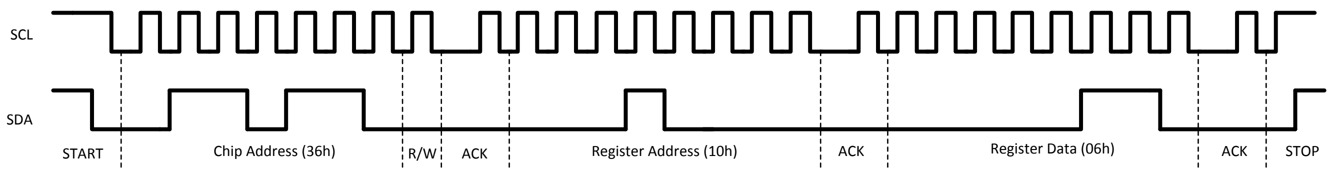


Figure 40. Write Sequence to the LM3528

Register Descriptions

There are 4, 8 bit registers within the LM3528 as detailed in Table 1.

Table 1. LM3528 Register Descriptions

Register Name	Hex Address	Power -On-Value
General Purpose (GP)	0x10	0xC0
Brightness Main (BMAIN)	0xA0	0x80
Brightness Sub (BSUB)	0xB0	0x80
HWEN/PGEN/GPIO Control (HPG)	0x80	0XF8
General Purpose I/O Control (GPIO)	0x81	0xFC
Pattern Register 0 (PGEN0)	0x90	0x00
Pattern Register 1 (PGEN1)	0x91	0x00
Pattern Register 2 (PGEN2)	0x92	0x00
Pattern Register 3 (PGEN3)	0x93	0x00

General Purpose Register (GP)

The General Purpose register has four functions. It controls the on/off state of MAIN and SUB/FB, it selects between Unison or Non-Unison mode, provides for control over the rate of change of the LED current (see Brightness Rate of Change Description), and selects between White LED and OLED mode. Figure 41 and Table 2 describes each bit available within the General Purpose Register. Table 3 summarizes the output state of the LM3528 for the different combinations of General Purpose register settings.

General Purpose Register
Register Address 0x10

MSB							LSB
1 Bit 7	1 Bit 6	OLED Bit 5	RMP1 Bit 4	RMP0 Bit 3	UNI Bit 2	ENS Bit 1	ENM Bit 0

Figure 41. General Purpose Register Description

Table 2. General Purpose Register Bit Function

Bit	Name	Function	Power-On-Value
0	ENM	Enable MAIN. Writing a 1 to this bit enables the main current sink (MAIN). Writing a 0 to this bit disables the main current sink and forces MAIN high impedance.	0
1	ENS	Enable SUB/FB. Writing a 1 to this bit enables the secondary current sink (SUB/FB). Writing a 0 to this bit disables the secondary current sink and forces SUB/FB high impedance.	0
2	UNI	Unison Mode Select. Writing a 1 to this bit disables the BSUB register and causes the contents of BMAIN to set the current in both the MAIN and SUB/FB current sinks. Writing a 0 to this bit allows the current into MAIN and SUB/FB to be independently controlled via the BMAIN and BSUB registers respectively.	0
3	RMP0	Brightness Rate of Change. Bits RMP0 and RMP1 set the rate of change of the LED current into MAIN and SUB/FB in response to changes in the contents of registers BMAIN and BSUB (see Brightness Rate of Change Description).	0
4	RMP1		0
5	OLED	OLED = 0 places the LM3528 in White LED mode. In this mode both the MAIN and SUB/FB current sinks are active. The boost converter ensures there is at least 500mV at V_{MAIN} and $V_{SUB/FB}$. OLED = 1 places the LM3528 in OLED mode. In this mode the boost converter regulates $V_{SUB/FB}$ to 1.244V. V_{MAIN} is unregulated and must be > 400mV for the MAIN current sink to maintain current regulation.	0
6	Don't Care	These are non-functional read only bits. They will always read back as a 1.	1
7			

Table 3. Operational Truth Table

UNI	OLED	ENM	ENS	Result
X	0	0	0	LM3528 Disabled
1	0	1	X	MAIN and SUB/FB current sinks enabled. Current levels set by contents of BMAIN.
1	0	0	X	MAIN and SUB/FB Disabled
0	0	0	1	SUB/FB current sink enabled. Current level set by BSUB.
0	0	1	0	MAIN current sink enabled. Current level set by BMAIN.
0	0	1	1	MAIN and SUB/FB current sinks enabled. Current levels set by contents of BMAIN and BSUB respectively.
X	1	1	X	SUB/FB current sink disabled (SUB/FB configured as a feedback pin). MAIN current sink enabled current level set by BMAIN.
X	1	0	X	SUB/FB current sink disabled (SUB/FB configured as a feedback pin). MAIN current sink disabled.

* ENM ,ENS, or OLED high enables analog circuitry.

Brightness Registers (BMAIN and BSUB)

With the UNI bit (General Purpose register) set to 0 (Non-Unison mode) both brightness registers (BMAIN and BSUB) independently control the LED currents I_{MAIN} and $I_{SUB/FB}$ respectively. BMAIN and BSUB are both 8 bit, but with only the 7 LSB's controlling the current. The MSB's is a don't care. The LED current control is designed to approximate an exponentially increasing response of the LED current vs increasing code in either BMAIN or BSUB (see Figure 44). Program I_{LED_MAX} by connecting a resistor (RSET) from SET to GND, where:

$$I_{LED\_MAX} = 192 \times \frac{1.244V}{R_{SET}} \tag{2}$$

With the UNI bit (General Purpose register) set to 1 (Unison mode), BSUB is disabled and BMAIN sets both I_{MAIN} and $I_{SUB/FB}$. This prevents the independent control of I_{MAIN} and $I_{SUB/FB}$, however matching between current sinks goes from typically 1%(with UNI = 0) to typically 0.15% (with UNI = 1). Figure 42 and Figure 43 show the register descriptions for the Brightness MAIN and Brightness SUB registers. Table 4 and Figure 44 show I_{MAIN} and/or $I_{SUB/FB}$ vs. brightness data as a percentage of I_{LED_MAX}.

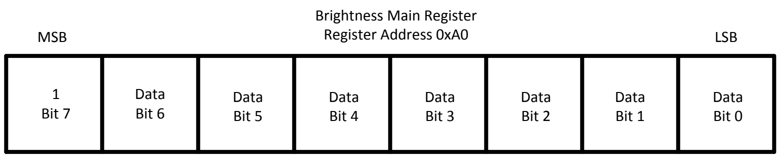


Figure 42. Brightness MAIN Register Description

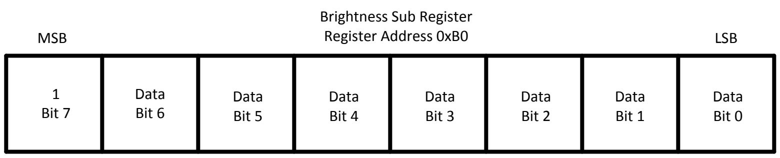


Figure 43. Brightness SUB Register Description

Table 4. I_{LED} vs. Brightness Register Data

BMAIN or BSUB Brightness Data	% of I_{LED_MAX}	BMAIN or BSUB Brightness Data	% of I_{LED_MAX}	BMAIN or BSUB Brightness Data	% of I_{LED_MAX}	BMAIN or BSUB Brightness Data	% of I_{LED_MAX}
0000000	0.000%	0100000	0.803%	1000000	4.078%	1100000	20.713%
0000001	0.166%	0100001	0.845%	1000001	4.290%	1100001	21.792%
0000010	0.175%	0100010	0.889%	1000010	4.514%	1100010	22.928%
0000011	0.184%	0100011	0.935%	1000011	4.749%	1100011	24.122%
0000100	0.194%	0100100	0.984%	1000100	4.996%	1100100	25.379%
0000101	0.204%	0100101	1.035%	1000101	5.257%	1100101	26.701%
0000110	0.214%	0100110	1.089%	1000110	5.531%	1100110	28.092%
0000111	0.226%	0100111	1.146%	1000111	5.819%	1100111	29.556%
0001000	0.237%	0101000	1.205%	1001000	6.122%	1101000	31.096%
0001001	0.250%	0101001	1.268%	1001001	6.441%	1101001	32.716%
0001010	0.263%	0101010	1.334%	1001010	6.776%	1101010	34.420%
0001011	0.276%	0101011	1.404%	1001011	7.129%	1101011	36.213%
0001100	0.291%	0101100	1.477%	1001100	7.501%	1101100	38.100%
0001101	0.306%	0101101	1.554%	1001101	7.892%	1101101	40.085%
0001110	0.322%	0101110	1.635%	1001110	8.303%	1101110	42.173%
0001111	0.339%	0101111	1.720%	1001111	8.735%	1101111	44.371%
0010000	0.356%	0110000	1.809%	1010000	9.191%	1110000	46.682%
0010001	0.375%	0110001	1.904%	1010001	9.669%	1110001	49.114%
0010010	0.394%	0110010	2.003%	1010010	10.173%	1110010	51.673%
0010011	0.415%	0110011	2.107%	1010011	10.703%	1110011	54.365%
0010100	0.436%	0110100	2.217%	1010100	11.261%	1110100	57.198%
0010101	0.459%	0110101	2.332%	1010101	11.847%	1110101	60.178%
0010110	0.483%	0110110	2.454%	1010110	12.465%	1110110	63.313%
0010111	0.508%	0111011	2.582%	1010111	13.114%	1110111	66.611%
0011000	0.535%	0110111	2.716%	1011000	13.797%	1111000	70.082%

Table 4. I_{LED} vs. Brightness Register Data (continued)

BMAIN or BSUB Brightness Data	% of I_{LED_MAX}	BMAIN or BSUB Brightness Data	% of I_{LED_MAX}	BMAIN or BSUB Brightness Data	% of I_{LED_MAX}	BMAIN or BSUB Brightness Data	% of I_{LED_MAX}
0011001	0.563%	0111000	2.858%	1011001	14.516%	1111001	73.733%
0011010	0.592%	0111001	3.007%	1011010	15.272%	1111010	77.574%
0011011	0.623%	0111010	3.163%	1011011	16.068%	1111011	81.616%
0011100	0.655%	0111011	3.328%	1011100	16.905%	1111100	85.868%
0011101	0.689%	0111100	3.502%	1011101	17.786%	1111101	90.341%
0011110	0.725%	0111101	3.684%	1011110	18.713%	1111110	95.048%
0011111	0.763%	0111111	3.876%	1011111	19.687%	1111111	100.000%

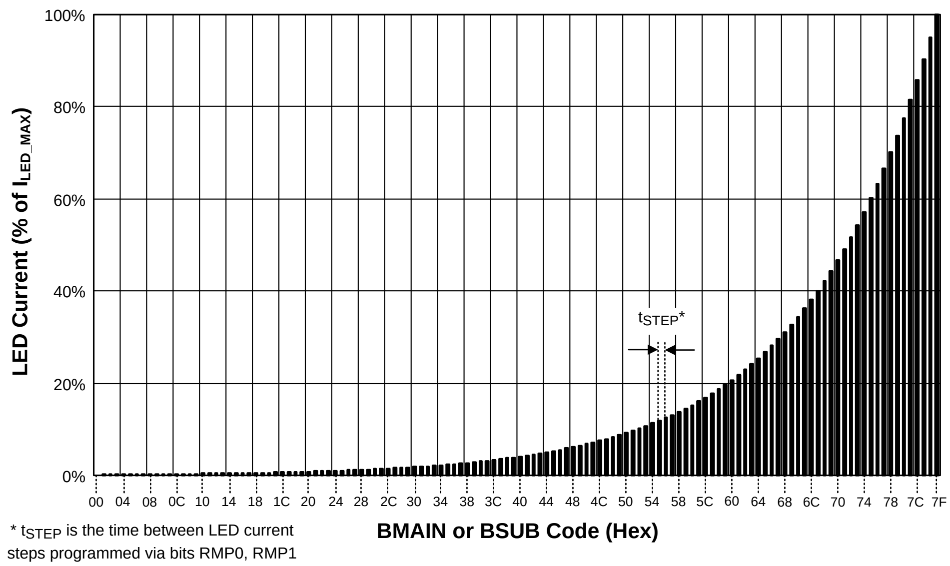


Figure 44. I_{MAIN} or I_{SUB} vs BMAIN or BSUB Data

Brightness Rate of Change Description

RMP0 and RMP1 control the rate of change of the LED current I_{MAIN} and $I_{SUB/FB}$ in response to changes in BMAIN and/or BSUB. There are 4 user programmable LED current rates of change settings for the LM3528 (see Table 5).

Table 5. Rate of Change Bits

RMP0	RMP1	Change Rate (t_{STEP})
0	0	12.75µs/step
0	1	3.25ms/step
1	0	6.5ms/step
1	1	13ms/step

For example, if R_{SET} = 12.1kΩ then I_{LED_MAX} = 20mA. With the contents of BMAIN set to 0x7F (I_{MAIN} = 20mA), suppose the contents of BMAIN are changed to 0x00 resulting in (I_{MAIN} = 0mA). With RMP0 =1 and RMP1 = 1 (13ms/step), I_{MAIN} will change from 20mA to 0mA in 127 steps with 13ms elapsing between steps, excluding the step from 0x7F to 0x7E, resulting in a full scale current change in 1638ms. The total time to transition from one brightness code to another is:

$$t_{transition} = (|\text{InitialCode} - \text{FinalCode}| - 1) \times t_{STEP} \quad (3)$$

The following 3 additional examples detail possible scenarios when using the brightness register in conjunction with the rate of change bits and the enable bits.

Example 1:

Step 1: Write to BMAIN a value corresponding to I_{MAIN} = 20mA.

Step 2: Write 1 to ENM (turning on MAIN)

Step 3: I_{MAIN} ramps to 20mA with a rate set by RMP0 and RMP1. (RMP0 and RMP1 bits set the duration spent at one brightness code before incrementing to the next).

Step 4: ENM is set to 0 before 20mA is reached, thus the LED current fades off at a rate given by RMP0 and RMP1 without I_{MAIN} going up to 20mA.

Example 2:

Step 1: ENM is 1, and BMAIN has been programmed with code 0x01. This results in a small current into MAIN.

Step 2: BMAIN is programmed with 0x7F (full scale current). This causes I_{MAIN} to ramp toward full-scale at the rate selected by RMP0 and RMP1.

Step 3: Before I_{MAIN} reaches full-scale BMAIN is programmed with 0x30. I_{MAIN} will continue to ramp to full scale.

Step 4: When I_{MAIN} has reached full-scale value it will ramp down to the current corresponding to 0x30 at a rate set by RMP0 and RMP1.

Example 3:

Step 1: Write to BMAIN a value corresponding to I_{MAIN} = 20mA.

Step 2: Write a 1 to both RMP0 and RMP1.

Step 3: Write 1 to ENM (turning on MAIN).

Step 4: I_{MAIN} ramps toward 20mA with a rate set by RMP0 and RMP1. (RMP0 and RMP1 bits set the duration spent at one brightness code before incrementing to the next).

Step 5: After 1.222s I_{MAIN} has ramped to 19.687% of I_{LED_MAX} (0.19687 × 20mA = 3.9374mA). Simultaneously, RMP0 and RMP1 are both programmed with 0.

Step 6: I_{MAIN} continues ramping from 3.9374mA to 20mA, but at a new ramp rate of 12.75µs/step.

Table 6. HPG Register Function

Bits 7 – 6 (PGEN Bit Period)	Bits 5 - 3 (PGEN Enable/Disable and Duty Cycle Selection)	Bit 2 (GPIO Data)	Bit 1 (GPIO Data Direction)	Bit 0 (HWEN Control)	Function
X	X	X	X	0	HWEN/PGEN/GPIO is configured as an active high Hardware Enable Input (HWEN)
00 = 1.6µs/bit (625kHz) 01 = 26ms/bit (38Hz) 10 = 52ms/bit (19Hz) 11 = 105ms/bit (9.5Hz) (1)	001 = 100% 010 = 1/2 011 = 1/3 100 = 1/4 101 = 1/6 110 = 1/12 111 = Latch Pattern Into Shift Register (2)	X	X	1	HWEN/PGEN/GPIO is configured as a Pattern Generator Output with the frequency set by bits <7:6> and the duty cycle set by bits <5:3>. (See Figure 46.)
X	000	GPIO Read Data	1	1	HWEN/PGEN/GPIO is configured as a GPIO Input. Read data from bit 2.
X	000	GPIO Write Data	0	1	HWEN/PGEN/GPIO is configured as a GPIO Output. A '1' written to bit 2 will force HWEN/PGEN/GPIO high; a 0 written to bit 2 will force HWEN/PGEN/GPIO low.

(1) This represents the amount of time each programmed bit will be present at HWEN/PGEN/GPIO. The entire pattern period will be 32 × Bit Period.

(2) This duty cycle indicates the fraction of time the pattern is being output at HWEN/PGEN/GPIO. For example the 1/2 duty cycle (bits <5:3> = 010) will have the 32 bit pattern output once followed by a dead time (HWEN/PGEN/GPIO high impedance) equal to 1×'s the pattern period (Deadtime = 32 × Bit_Period × (1/DutyCycle -1). For the 100% duty cycle setting the 32 bit pattern will repeat constantly with no deadtime.

HWEN/PGENGPIO Register
Register Address 0x80
Power On Reset = 0x01

MSB							LSB
Frequency Selection Bit 7	Frequency Selection Bit 6	Duty Cycle Selection Bit 5	Duty Cycle Selection Bit 4	Duty Cycle Selection Bit 3	GPIO Data Bit 2	GPIO Data Direction Bit 1	HWEN Enable/ Disable Bit 0

Figure 45. HPG Register Description

Table 7. GPIO Register Function

Bits 7 - 2	GPIO Data (Bit 1)	Data Direction (Bit 0)	Function
X	X	0	GPIO is configured as a GPIO input with the input data read back via bit [1]. This is the default power on state.
X	X	1	GPIO is configured as a logic output. The output logic voltage is written to bit [1].

GPIO Register
Register Address 0x81
Power On Reset = 0xFC

MSB							LSB
1 Bit 7	1 Bit 6	1 Bit 5	1 Bit 4	1 Bit 3	1 Bit 2	Data Bit 1	Data Direction Bit 0

Figure 46. GPIO Register Description

Figure 47 – Figure 50 detail the Pattern Generator Data Registers. These hold the 32 bit data that is output at HWEN/PGEN/GPIO in PGEN mode. The data is output LSB first (Bit 0 of PGEN0) and MSB last (Bit 7 of PGEN3).

PGEN0 Register
Register Address 0x90
Power On Reset = 0x00

MSB							LSB
PGEN DATA 7 Bit 7	PGEN DATA 6 Bit 6	PGEN DATA 5 Bit 5	PGEN DATA 4 Bit 4	PGEN DATA 3 Bit 3	PGEN DATA 2 Bit 2	PGEN DATA 1 Bit 1	PGEN DATA 0 Bit 0

Figure 47. PGEN0 Register Description

PGEN1 Register
Register Address 0x91
Power On Reset = 0x00

MSB							LSB
PGEN DATA 15 Bit 7	PGEN DATA 14 Bit 6	PGEN DATA 13 Bit 5	PGEN DATA 12 Bit 4	PGEN DATA 11 Bit 3	PGEN DATA 10 Bit 2	PGEN DATA 9 Bit 1	PGEN DATA 8 Bit 0

Figure 48. PGEN1 Register Description

PGEN2 Register
Register Address 0x92
Power On Reset = 0x00

MSB							LSB
PGEN DATA 23 Bit 7	PGEN DATA 22 Bit 6	PGEN DATA 21 Bit 5	PGEN DATA 20 Bit 4	PGEN DATA 19 Bit 3	PGEN DATA 18 Bit 2	PGEN DATA 17 Bit 1	PGEN DATA 16 Bit 0

Figure 49. PGEN2 Register Description

PGEN3 Register
Register Address 0x93
Power On Reset = 0x00

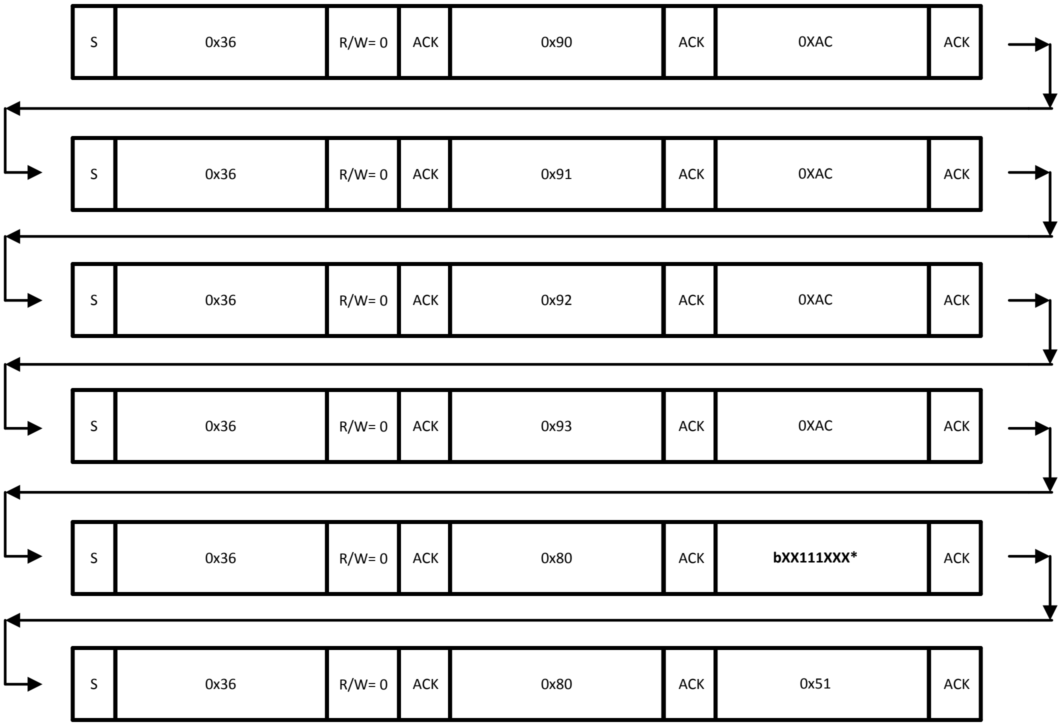
MSB							LSB
PGEN DATA 31 Bit 7	PGEN DATA 30 Bit 6	PGEN DATA 29 Bit 5	PGEN DATA 28 Bit 4	PGEN DATA 27 Bit 3	PGEN DATA 26 Bit 2	PGEN DATA 25 Bit 1	PGEN DATA 24 Bit 0

Figure 50. PGEN3 Register Description

Figure 51 shows a write sequence to the pattern generator programmed to output the waveform in Figure 52. In this example HPG register bits <7:6> = 01 (for 26ms/bit) and bits <5:3> = 010 (for 1/2 duty cycle). The pattern data in registers (PGEN0 – PGEN2) are all loaded with 0xAC. A '1' will force the HWEN/PGEN/GPIO output low while a '0' will force HWEN/PGEN/GPIO open drain. When set for a 26ms/bit period the pattern will be output LSB first (PGEN0, bit 0) and repeat every

$$t_{PERIOD} = \frac{26\ \text{ms/bit} \times 32\ \text{bits}}{1/2\ \text{Dutycycle}} = 1.664\text{s} \quad (4)$$

When set for ½ duty cycle there will be a dead time (HWEN/PGEN/GPIO high impedance) between each pattern and equal to the pattern period. In applications where HWEN/PGEN/GPIO is used to pull current through an indicator LED a '1' corresponds to the LED on and a '0' corresponds to the LED off.



*Only bits <5:3> are necessary in this byte the rest are don't cares. Bits <5:3> = '111' are necessary to latch the pattern generator data bits into the internal shift register.

Figure 51. Pattern Generation Write Sequence

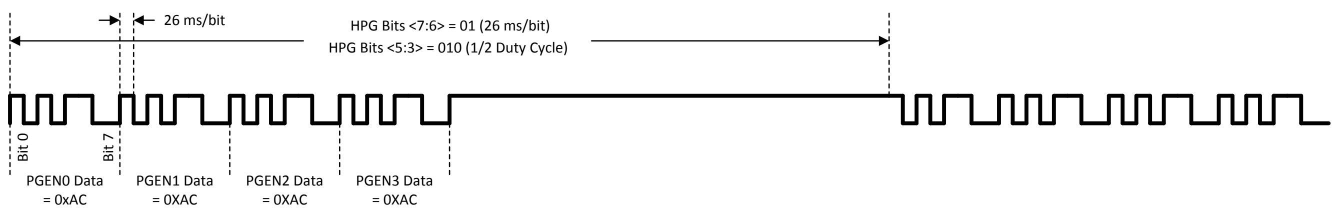


Figure 52. Pattern Generation Output

Shutdown and Output Isolation

The LM3528 provides a true shutdown for either MAIN or SUB/FB when configured as a White LED bias supply. Write a 0 to ENM (bit 1) of the General Purpose register to turn off the MAIN current sink and force MAIN high impedance. Write a 0 to ENS (bit 2) of the General Purpose register to turn off the SUB/FB current sink and force SUB/FB high impedance. Writing a 1 to ENM or ENS turns on the MAIN and SUB/FB current sinks respectively. When in shutdown the leakage current into MAIN or SUB/FB is typically 1.8µA. See Typical Performance Characteristics Plots for start-up responses of the LM3528 using the ENM and ENS bits in White LED and OLED modes.

Application Information

LED Current Setting/Maximum LED Current

Connect a resistor (R_{SET}) from SET to GND to program the maximum LED current (I_{LED_MAX}) into MAIN or SUB/FB. The R_{SET} to I_{LED_MAX} relationship is:

$$I_{LED\_MAX} = 192 \times \frac{1.244V}{R_{SET}} \tag{5}$$

where SET provides the constant 1.244V output.

Output Voltage Setting (OLED Mode)

Connect Feedback resistors from the converters output to SUB/FB to GND to set the output voltage in OLED mode (see R1 and R2 in the Figure 1 (OLED Panel Power Supply). First select R2 < 100kΩ then calculate R1 such that:

$$R1 = R2\left(\frac{V_{OUT}}{1.21V} - 1\right) \tag{6}$$

In OLED mode the MAIN current sink continues to regulate the current through MAIN, however, V_{MAIN} is no longer regulated. To avoid dropout and ensure proper current regulation the application must ensure that V_{MAIN} > 0.3V.

Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the input voltage ripple caused by the switching of the LM3528's boost converter. For continuous inductor current operation the input voltage ripple is composed of 2 primary components, the capacitor discharge (delta V_Q) and the capacitor's equivalent series resistance (delta V_{ESR}). These ripple components are found by:

$$\Delta V_Q = \frac{\Delta I_L \text{ x } D}{2 \text{ x } f_{SW} \text{ x } C_{IN}}$$

and

$$\Delta V_{ESR} = 2 \text{ x } \Delta I_L \text{ x } R_{ESR}$$

$$\text{where } \Delta I_L = \frac{V_{IN} \text{ x } (V_{OUT} - V_{IN})}{2 \text{ x } f_{SW} \text{ x } L \text{ x } V_{OUT}} \tag{7}$$

In the typical application circuit a 1µF ceramic input capacitor works well. Since the ESR in ceramic capacitors is typically less than 5mΩ and the capacitance value is usually small, the input voltage ripple is primarily due to the capacitive discharge. With larger value capacitors such as tantalum or aluminum electrolytic the ESR can be greater than 0.5Ω. In this case the input ripple will primarily be due to the ESR.

Output Capacitor Selection

The LM3528's output capacitor supplies the LED current during the boost converters on time. When the switch turns off the inductor energy is discharged through the diode supplying power to the LED's and restoring charge to the output capacitor. This causes a sag in the output voltage during the on time and a rise in the output voltage during the off time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on LED or OLED panel current requirements and input/output voltage differentials. For proper operation ceramic output capacitors ranging from 1µF to 2.2µF are required.

As with the input capacitor, the output voltage ripple is composed of two parts, the ripple due to capacitor discharge (delta V_Q) and the ripple due to the capacitors ESR (delta V_{ESR}). For continuous conduction mode, the ripple components are found by:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \quad \text{and}$$

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} + \Delta I_L\right)$$

$$\text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{8}$$

Table 8 lists different manufacturers for various capacitors and their case sizes that are suitable for use with the LM3528. When configured as a dual output LED driver a 1µF output capacitor is adequate. In OLED mode for output voltages above 12V a 2.2µF output capacitor is required (see Low Output Voltage Operation (OLED) Section).

Table 8. Recommended Output Capacitors

Manufacturer	Part Number	Value	Case Size	Voltage Rating
TDK	C1608X5R1E105M	1µF	0603	25V
Murata	GRM39X5R105K25D539	1µF	0603	25V
TDK	C2012X5R1E225M	2.2µF	0805	25V
Murata	GRM219R61E225KA12	2.2µF	0805	25V

Inductor Selection

The LM3528 is designed for use with a 10µH inductor, however 22µH are suitable providing the output capacitor is increased 2×. When selecting the inductor ensure that the saturation current rating (I_{SAT}) for the chosen inductor is high enough and the inductor is large enough such that at the maximum LED current the peak inductor current is less than the LM3528's peak switch current limit. This is done by choosing:

$$I_{SAT} > \frac{I_{LED}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where}$$

$$\Delta I_L = \frac{V_{IN} \text{ x } (V_{OUT} - V_{IN})}{2 \text{ x } f_{SW} \text{ x } L \text{ x } V_{OUT}}, \text{ and}$$

$$L > \frac{V_{IN} \text{ x } (V_{OUT} - V_{IN})}{2 \text{ x } f_{SW} \text{ x } V_{OUT} \text{ x } \left(I_{PEAK} - \frac{I_{LED\_MAX} \text{ x } V_{OUT}}{\eta \text{ x } V_{IN}} \right)} \quad (9)$$

Values for I_{PEAK} can be found in the plot of peak current limit vs. V_{IN} in the Typical Performance Characteristics graphs. Table 9 shows possible inductors, as well as their corresponding case size and their saturation current ratings.

Table 9. Recommended Inductors

Manufacturer	Part Number	Value	Dimensions	I_{SAT}	DC Resistance
TDK	VLF3012AT-100MR49	10µH	2.6mm×2.8mm×1mm	490mA	0.36Ω
Coilcraft	LPS3008-103ML	10µH	2.95mm×2.95mm×0.8mm	490mA	0.65Ω
TDK	VLF4012AT-100MR79	10µH	3.5mm×3.7mm×1.2mm	800mA	0.3Ω
Coilcraft	LPS4012-103ML	10µH	3.9mm×3.9mm×1.1mm	700mA	0.35Ω
TOKO	A997AS-100M	10µH	3.8mm×3.8mm×1.8mm	580mA	0.18Ω

Diode Selection

The output diode must have a reverse breakdown voltage greater than the maximum output voltage. The diodes average current rating should be high enough to handle the LM3528's output current. Additionally, the diodes peak current rating must be high enough to handle the peak inductor current. Schottky diodes are recommended due to their lower forward voltage drop (0.3V to 0.5V) compared to (0.6V to 0.8V) for PN junction diodes. If a PN junction diode is used, ensure it is the ultra-fast type (trr < 50ns) to prevent excessive loss in the rectifier. For Schottky diodes the B05030WS (or equivalent) work well for most designs. See Table 10 for a list of other Schottky Diodes with similar performance.

Table 10. Recommended Schottky Diodes

Manufacturer	Part Number	Package	Reverse Breakdown Voltage	Average Current Rating
On Semiconductor	NSR0230P2T5G	SOD-923 (0.8mm×0.6mm×0.4mm)	30V	200mA
On Semicondcuctor	NSR0230M2T5G	SOD-723 (1mm×0.6mm×0.52mm)	30V	200mA
On Semiconductor	RB521S30T1	SOD-523 (1.2mm×0.8mm×0.6mm)	30V	200mA
Diodes Inc.	SDM20U30	SOD-523 (1.2mm×0.8mm×0.6mm)	30V	200mA
Diodes Inc.	B05030WS	SOD-323 (1.6mm×1.2mm×1mm)	30V	0.5A
Philips	BAT760	SOD-323 (1.6mm×1.2mm×1mm)	20V	1A

Output Current Range (OLED Mode)

The maximum output current the LM3528 can deliver in OLED mode is limited by 4 factors (assuming continuous conduction); the peak current limit of 770mA (typical), the inductor value, the input voltage, and the output voltage. Calculate the maximum output current (I_{OUT_MAX}) using the following equation:

$$I_{OUT\_MAX} = \frac{(I_{PEAK} - \Delta I_L) \times \eta \times V_{IN}}{V_{OUT}}$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (10)$$

For the typical application circuit with V_{OUT} = 18V and assuming 70% efficiency, the maximum output current at V_{IN} = 2.7V will be approximately 70mA. At 4.2V due to the shorter on times and lower average input currents the maximum output current (at 70% efficiency) jumps to approximately 105mA. Figure 53 shows a plot of I_{OUT_MAX} vs. V_{IN} using the above equation, assuming 80% efficiency. In reality, factors such as current limit and efficiency will vary over V_{IN}, temperature, and component selection. This can cause the actual I_{OUT_MAX} to be higher or lower.

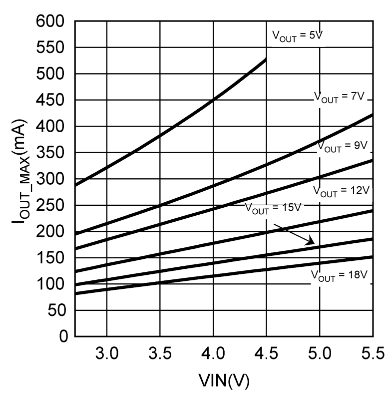


Figure 53. Typical Maximum Output Current in OLED Mode (assumed 80% efficiency)

Output Voltage Range (OLED Mode)

The LM3528's output voltage is constrained by 2 factors. On the low end it is limited by the minimum duty cycle of 10% (assuming continuous conduction) and on the high end it is limited by the over voltage protection threshold (V_{OVP}) of 22V (typical). In order to maintain stability when operating at different output voltages the output capacitor and inductor must be changed. Refer to Table 10 for different V_{OUT}, C_{OUT}, and L combinations.

Table 11. Component Values for Output Voltage Selection

V_{OUT}	C_{OUT}	L	V_{IN} Range
18V	2.2µF	10µH	2.7V to 5.5V
15V	2.2µF	10µH	2.7V to 5.5V
12V	4.7µF	10µH	2.7V to 5.5V
9V	10µF	10µH	2.7V to 5.5V
7V	10µF	4.7µH	2.7V to 5.5V
5V	22µF	4.7µH	2.7V to 4.5V

Application Circuits

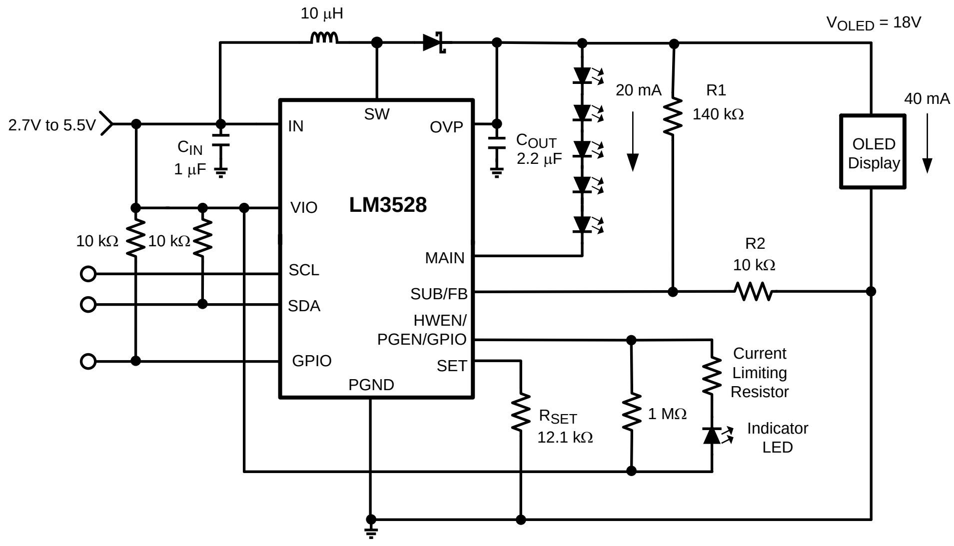


Figure 54. LED Backlight + OLED Power Supply

Layout Considerations

Refer to AN-1112 SNVA009 for DSBGA package soldering

The high switching frequencies and large peak currents in the LM3528 make the PCB layout a critical part of the design. The proceeding steps should be followed to ensure stable operation and proper current source regulation.

1. C_{IN} should be located on the top layer and as close to the device as possible. The input capacitor supplies the driver currents during MOSFET switching and can have relatively large spikes. Connecting the capacitor close to the device will reduce the inductance between CIN and the LM3528 and eliminate much of the noise that can disturb the internal analog circuitry.

2. Connect the anode of the Schottky diode as close to the SW pin as possible. This reduces the inductance between the internal MOSFET and the diode and minimizes the noise generated from the discontinuous diode current and the PCB trace inductance that will add ringing at the SW node and filter through to VOUT. This is especially important in VOUT mode when designing for a stable output voltage.

3. C_{OUT} should be located on the top layer to minimize the trace lengths between the diode and PGND. Connect the positive terminal of the output capacitor (COUT+) as close as possible to the cathode of the diode. Connect the negative terminal of the output capacitor (COUT-) as close as possible to the PGND pin on the LM3528. This minimizes the inductance in series with the output capacitor and reduces the noise present at VOUT and at the PGND connection. This is important due to the large di/dt into and out of COUT. The returns for both CIN and COUT should terminate directly to the PGND pin.

4. Connect the inductor on the top layer close to the SW pin. There should be a low impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the high dV/dt present at SW that can couple into nearby traces.

5. , Route the traces for R_{SET} and the feedback divider away from the SW node to minimize the capacitance between these nodes that can couple the high dV/dt present at SW into them. Furthermore, the feedback divider and R_{SET}should have dedicated returns that terminate directly to the PGND pin of the device. This will minimize any shared current with COUT or CIN that can lead to instability. Avoide routing the SUB/FB node close to other traces that can see high dV/dt such as the I2C pins. The capacitive coupling on the PCB between FB and these nodes can disturb the output voltage and cause large voltage spikes at VOUT.

6. Do not connect any external capacitance to the SET pin.

7. Refer to the LM3528 Evaluation Board as a guide for proper layout.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3528TME/NOPB	ACTIVE	DSBGA	YFQ	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SE	Samples
LM3528TMX/NOPB	ACTIVE	DSBGA	YFQ	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

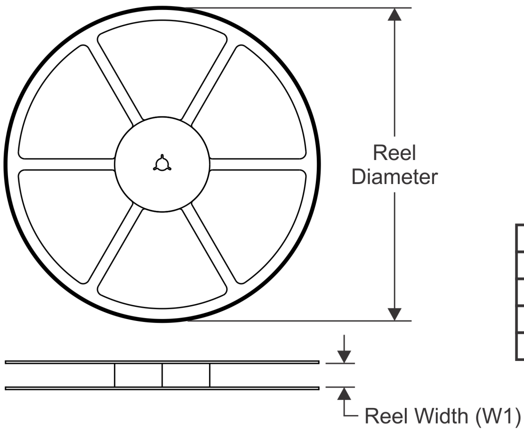
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

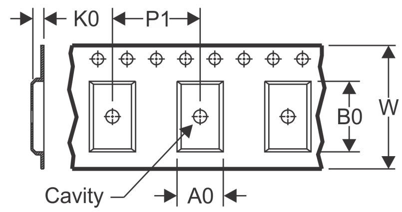
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

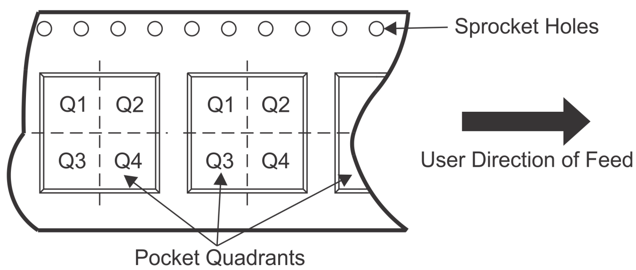


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

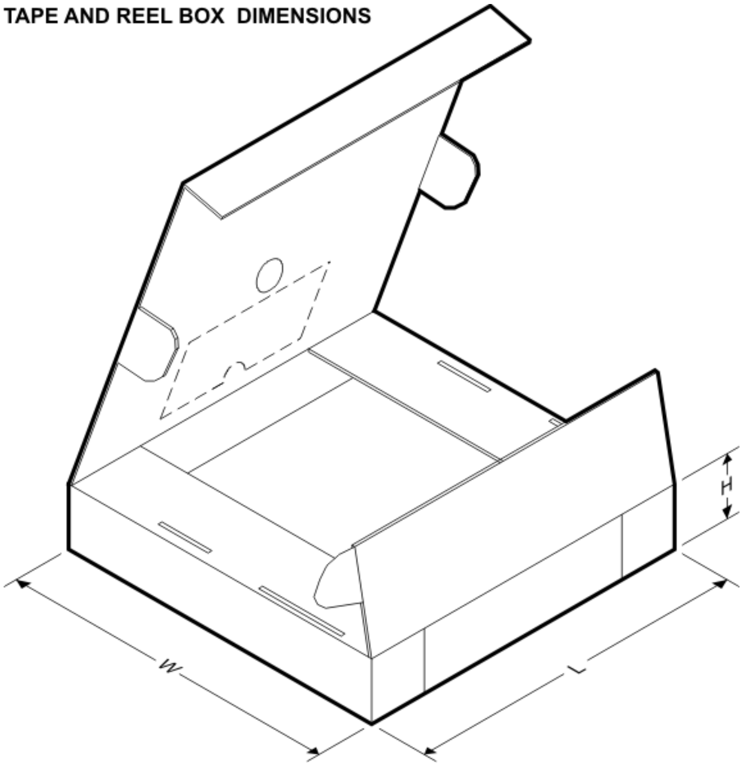
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3528TME/NOPB	DSBGA	YFQ	12	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3528TMX/NOPB	DSBGA	YFQ	12	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1

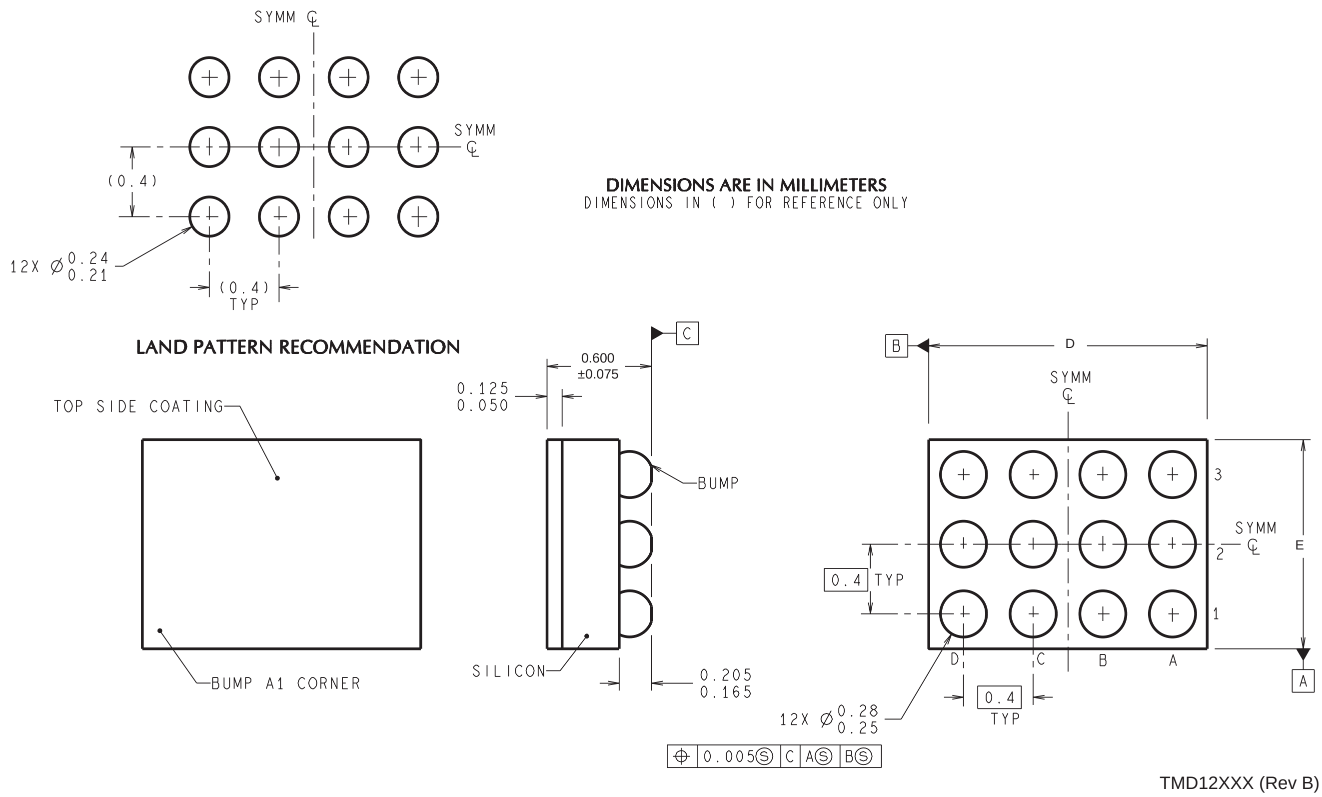
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3528TME/NOPB	DSBGA	YFQ	12	250	208.0	191.0	35.0
LM3528TMX/NOPB	DSBGA	YFQ	12	3000	208.0	191.0	35.0

YFQ0012



D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.24 mm, Min = 1.18 mm

4215079/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.