# RAD-TOLERANT CLASS-V, SWITCHED MODE CONTROLLER FOR DC MOTOR DRIVE

**Check for Samples: UC1637-SP**

## FEATURES

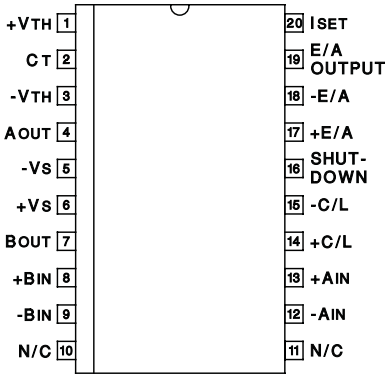
- **QML-V Qualified, SMD 5962-89957**
- **Rad Tolerant: 30 kRad(Si) TID** (1)
  - **TID Dose Rate = 10 mRad/sec**
- **Single or Dual Supply Operation**
- **±2.5-V to ±20-V Input Supply Range**
- **±5% Initial Oscillator Accuracy; ±10% Over Temperature**
- **Pulse-by-Pulse Current Limiting**
- **Under-Voltage Lockout**
- **Shutdown Input with Temperature Compensated 2.5-V Threshold**
- **Uncommitted PWM Comparators for Design**

(1) Radiation tolerance is a typical value based upon initial device qualification. Radiation Lot Acceptance Testing is available - contact factory for details.

**Flexibility**

- **Dual 100-mA Source/Sink Output Drivers**

W PACKAGE
(TOP VIEW)




## DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

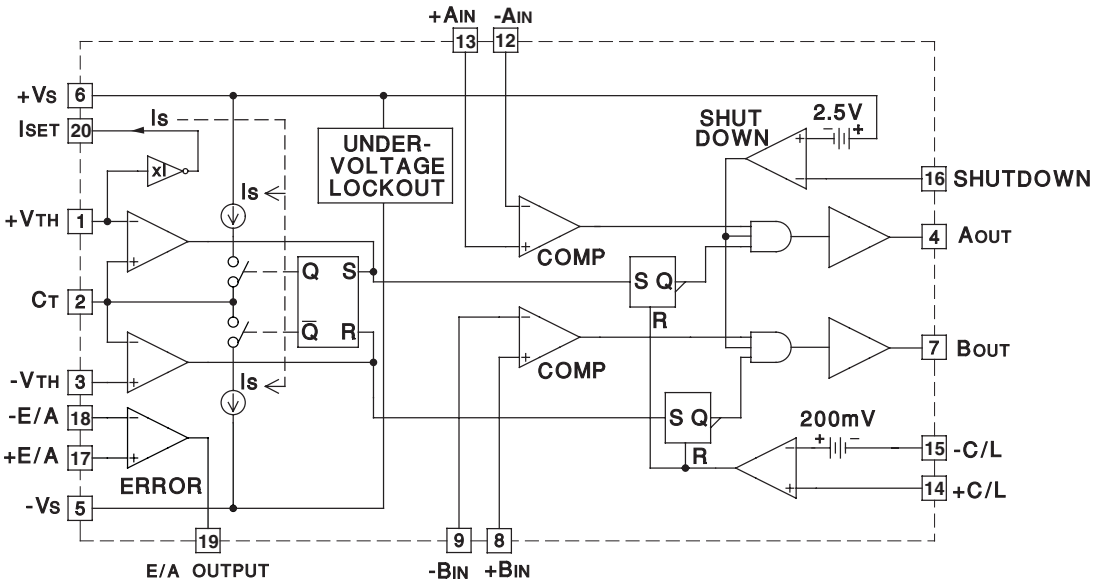
This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ±100-mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5-V temperature compensated threshold.

The UC1637 is characterized for operation over the full space temperature range of –55°C to 125°C.

### ORDERING INFORMATION

| $T_A$ | PACKAGE | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| –55°C to 125°C | CFP-20 | 5962-8995701VSA | UC1637W-SP |

## FUNCTIONAL BLOCK DIAGRAM




Note: Fault latches are reset dominant.

## ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage | | ±20 | V |
| $I_O$ | Output current, source/sink ($A_{OUT}$, $B_{OUT}$) | Peak | 500 | mA |
| | | Steady-state | 100 | |
| | Analog inputs ($+V_{TH}$, $C_T$, $-V_{TH}$, $+B_{IN}$, $-B_{IN}$, $-A_{IN}$, $+A_{IN}$, +C/L, -C/L, SHUTDOWN, +E/A, -E/A ) | | $\pm V_S$ | V |
| | Error amplifier output current ($E/A_{OUTPUT}$) | | ±20 | mA |
| | Oscillator charging current ($I_{SET}$) | | –2 | mA |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |
| | Lead temperature (soldering, 10 seconds) | | 300 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into, negative out of the specified terminal.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_S$ = 15 V, $-V_S$ = –15 V, $+V_{TH}$ = 5 V, $-V_{TH}$ = –5 V, $R_T$ = 16.7 kΩ, $C_T$ = 1500 pF, $T_A$ = –55°C to 125°C = $T_J$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| Initial accuracy(1) | | $T_J$ = 25°C | 9.4 | 10 | 10.6 | kHz |
| | | $T_J$ = –55°C to 125°C | 9.2 | | 10.8 | |
| Voltage stability | | $V_S$ = ±5 V to ±20 V, $+V_{TH}$ = 3 V, $-V_{TH}$ = –3 V | | 5 | 7 | % |
| Temperature stability | | Over operating range | | 0.5 | | % |
| Input bias current | $+V_{TH}$ | $C_T$ = 6 V | –10 | 0.1 | 10 | µA |
| | $-V_{TH}$ | $C_T$ = 0 V | –10 | –0.5 | | |
| Input range ($+V_{TH}$, $-V_{TH}$) | | | $-V_S$+2 | | $+V_S$-2 | V |
| **ERROR AMPLIFIER** | | | | | | |
| Input offset voltage | | $V_{CM}$ = 0 V | | 1.5 | ±5 | mV |
| Input bias current | | $V_{CM}$ = 0 V | | 0.5 | 5 | µA |
| Input offset current | | $V_{CM}$ = 0 V | | 0.1 | ±1 | µA |
| Common mode range | | $V_S$ = ±2.5 V to ±20 V | $-V_S$+2 | | $+V_S$ | V |
| Open loop volage gain | | $R_L$ = 10k | 75 | 100 | | dB |
| Slew rate | | | | 15 | | V/µs |
| Unity gain bandwidth | | | | 1 | | MHz |
| CMRR | | Over common mode range | 75 | 100 | | dB |
| PSRR | | $V_S$ = ±2.5 V to ±20 V | 75 | 110 | | dB |
| Output sink current | | $E/A_{OUTPUT}$ = 0 V | 20 | 50 | | mA |
| Output source current | | $E/A_{OUTPUT}$ = 0 V | | –11 | –5 | mA |
| High level output voltage | | | 13 | 13.6 | | V |
| Low level output voltage | | | | –14.8 | –13 | V |
| **PWM COMPARATORS** | | | | | | |
| Input offset voltage | | $V_{CM}$ = 0 V | –10 | 20 | 50 | mV |
| Input bias current | | $V_{CM}$ = 0 V | | 2 | 10 | µA |
| Input Hysteresis | | $V_{CM}$ = 0 V | | 10 | 30 | mV |
| Common mode range | | $V_S$ = ±5 V to ±20 V | $-V_S$+1 | | $+V_S$-2 | V |
| **CURRENT LIMIT** | | | | | | |
| Input offset voltage | | $V_{CM}$ = 0 V, $T_J$ = 25°C | 190 | 200 | 210 | mV |
| | | $V_{CM}$ = 0 V, $T_J$ = –55°C to 125°C | 160 | | 370 | |
| Input offset voltage T.C. | | | | –0.2 | | mV/°C |
| Input bias current | | | –10 | –1.5 | | µA |
| Common mode range | | $V_S$ = ±2.5 V to ±20 V | $-V_S$ | | $+V_S$-3 | V |
| **SHUTDOWN** | | | | | | |
| Shutdown threshold(2) | | | –2.7 | –2.5 | –2.3 | V |
| Hysteresis | | | | 40 | | mV |
| Input bias current | | SHUTDOWN = $+V_S$ to $-V_S$ | –10 | –0.5 | | µA |
| **UNDER-VOLTAGE LOCKOUT** | | | | | | |
| Start threshold(3) | | | | 4.15 | 5 | V |
| Hysteresis | | | 75 | 250 | 500 | mV |
| **TOTAL STANDBY CURRENT** | | | | | | |
| Supply current | | | | 8.5 | 15 | mA |

(1) $R_T$ and $C_T$ referenced to ground.
(2) Parameter measured with respect to $+V_S$ (Pin 6).
(3) Parameter measured at $+V_S$ (Pin 6) with respect to $-V_S$ (Pin 5).

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_S$ = 15 V, $-V_S$ = –15 V, $+V_{TH}$ = 5 V, $-V_{TH}$ = –5 V, $R_T$ = 16.7 kΩ, $C_T$ = 1500 pF, $T_A$ = –55°C to 125°C = $T_J$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **OUTPUT SECTION** | | | | | |
| Output low level | $I_{SINK}$ = 20 mA | | –14.9 | –13 | V |
| | $I_{SINK}$ = 100 mA | | –14.5 | –13 | |
| Output high level | $I_{SOURCE}$ = 20 mA | 13 | 13.5 | | V |
| | $I_{SOURCE}$ = 100 mA | 12 | 13.5 | | |
| Rise time | $C_L$ = 1 nF, $T_J$ = 25°C(4) | | 100 | 600 | ns |
| Fall time | $C_L$ = 1 nF, $T_J$ = 25°C(4) | | 100 | 300 | ns |

(4) Parameters ensured by design and/or characterization, if not production tested.

## FUNCTIONAL DESCRIPTION

The following is a description of each of the functional blocks shown in the Functional Block Diagram.

### Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, $I_{SET}$, and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the ISET terminal to develop the capacitor charging current through $R_T$. If $R_T$ is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillator's frequency and voltage amplitude are determined by the exernal components using the formulas given in Figure 1.

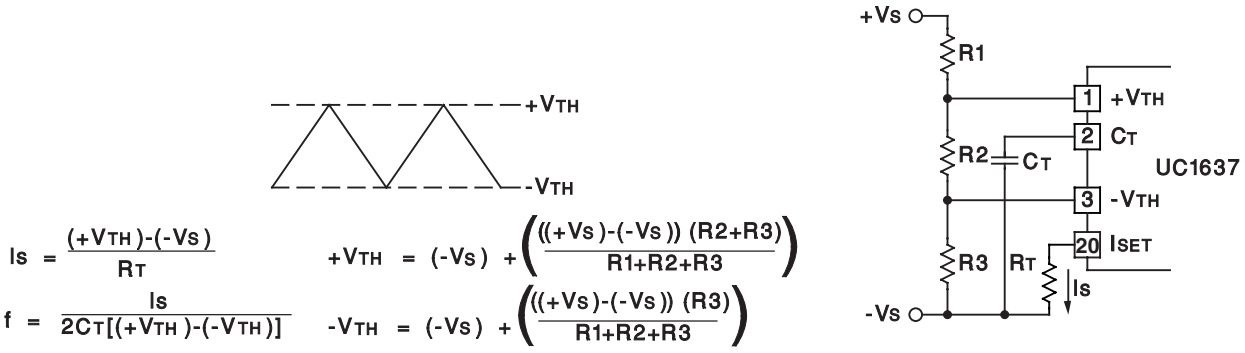



**Figure 1. Oscillator Setup**

### PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at -AIN and +BIN will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on -BIN and +AIN.

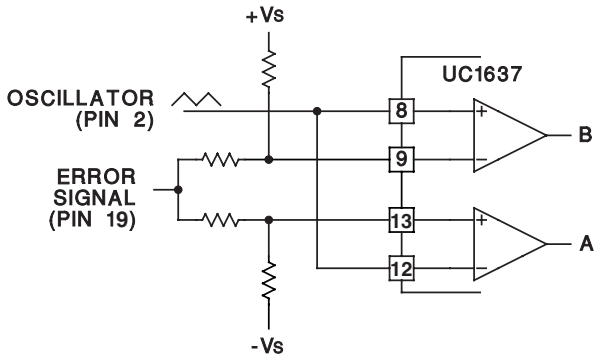



**Figure 2. Comparator Biasing**

## MODULATION SCHEMES

### Case A Zero Deadtime (Equal voltage on -BIN and +AIN)

In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3 (A) shows this configuration.

### Case B Small Deadtime (Voltage on -BIN > +AIN)

A small differential voltage between -BIN and +AIN provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3 (B).

### Case C Increased Deadtime and Deadband Mode (Voltage on -BIN > +AIN)

With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical siffness is unimportant, deadband operation can be used. This is shown in Figure 3 (C).

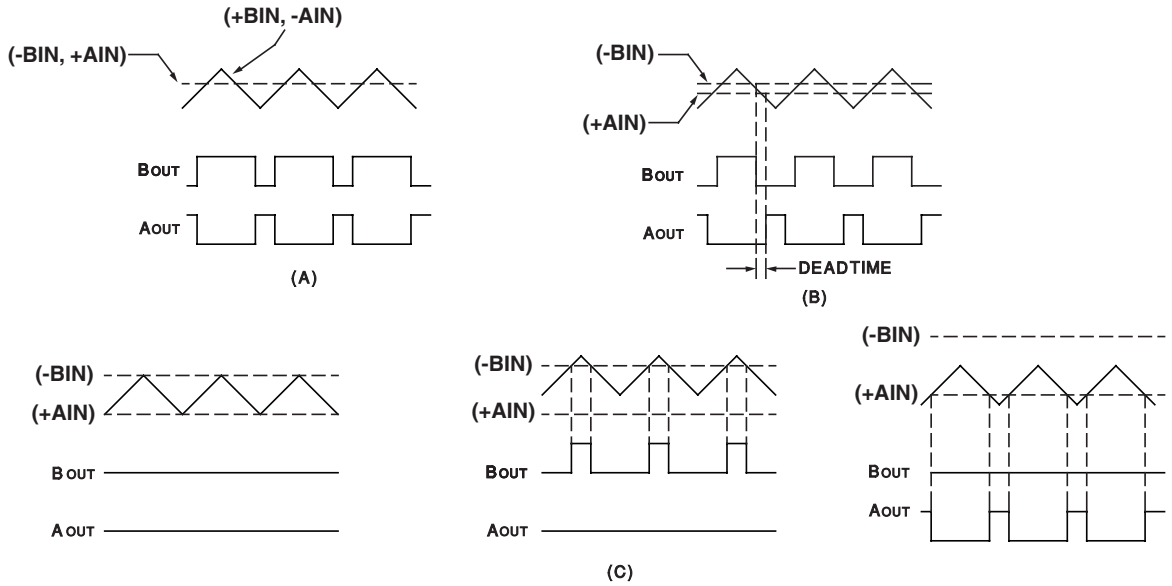



**Figure 3. Modulation Schemes Showing (A) Zero Deadtime, (B) Deadtime and (C) Deadband Configurations**

### Ouput Drivers

Each output driver is capable of both sourcing and sinking 100 mA steady state and up to 500 mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically $-V_S$+0.2 V at 50 mA low level and $+V_S$-2 V at 50 mA high level.

### Error Amplifier

The error amplifier consists of a high slew rate (15 V/μs) op-amp with a typical 1-MHz bandwidth and low output impedance. Depending on the $\pm V_S$ supply voltage, the common mode range and the voltage output swing is within 2 V of the $V_S$ supply.

### Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4 V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

### Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5 V below VIN, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

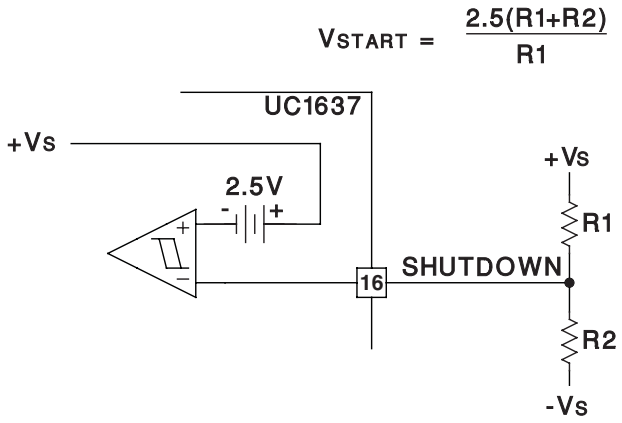



**Figure 4. External Under-Voltage Lockout**

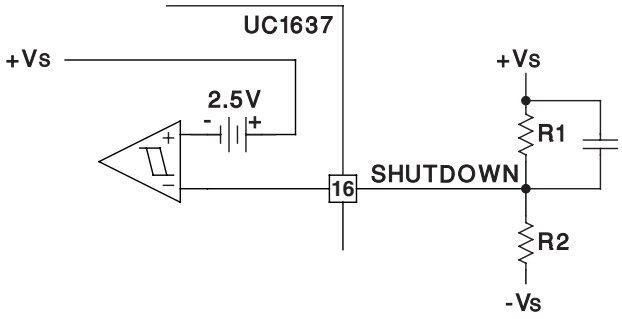



**Figure 5. Delayed Start-up**

### Current Limit

A latched current limit amplifier with an internal 200-mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from $-V_S$ to within 3 V of the $+V_S$ supply while providing excelent noise rejection. Figure 6 shows a typical current sense circuit.

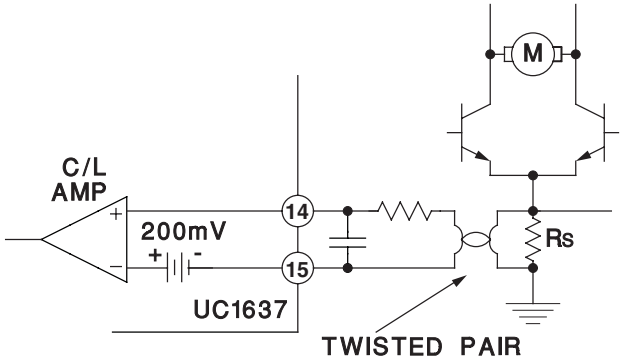



**Figure 6. Current Limit Sensing**

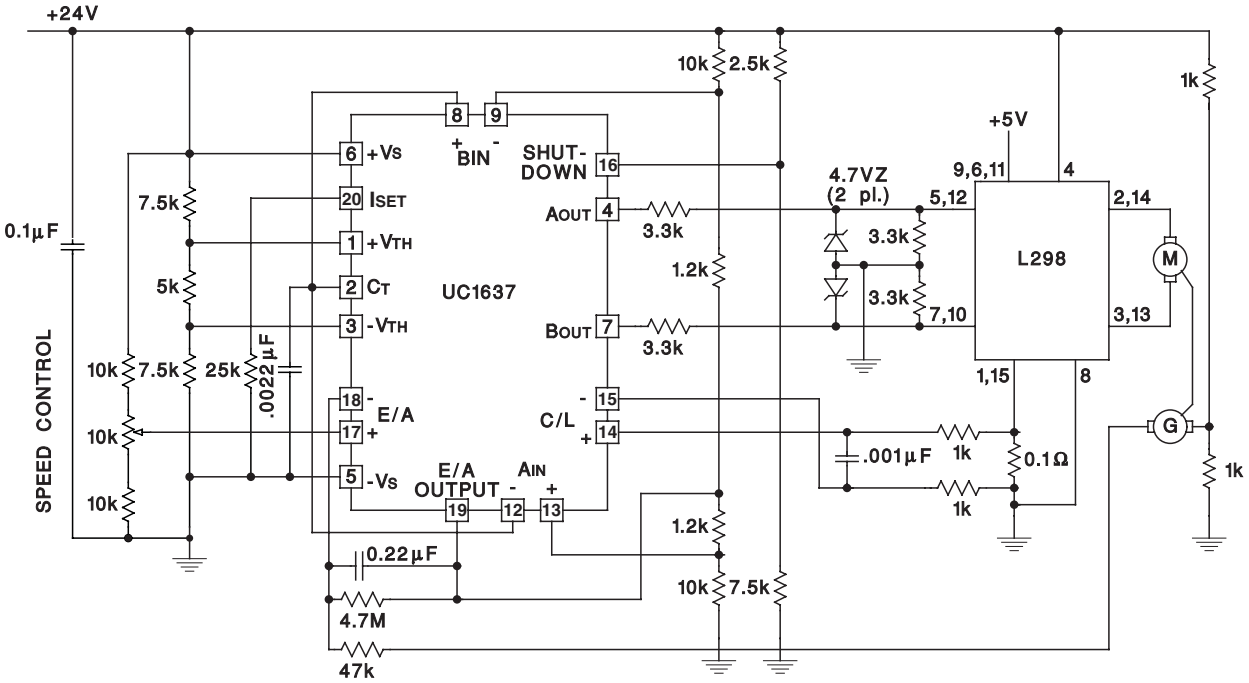



**Figure 7. Bi-Directional Motor Drive With Speed Control Power-Amplifier**

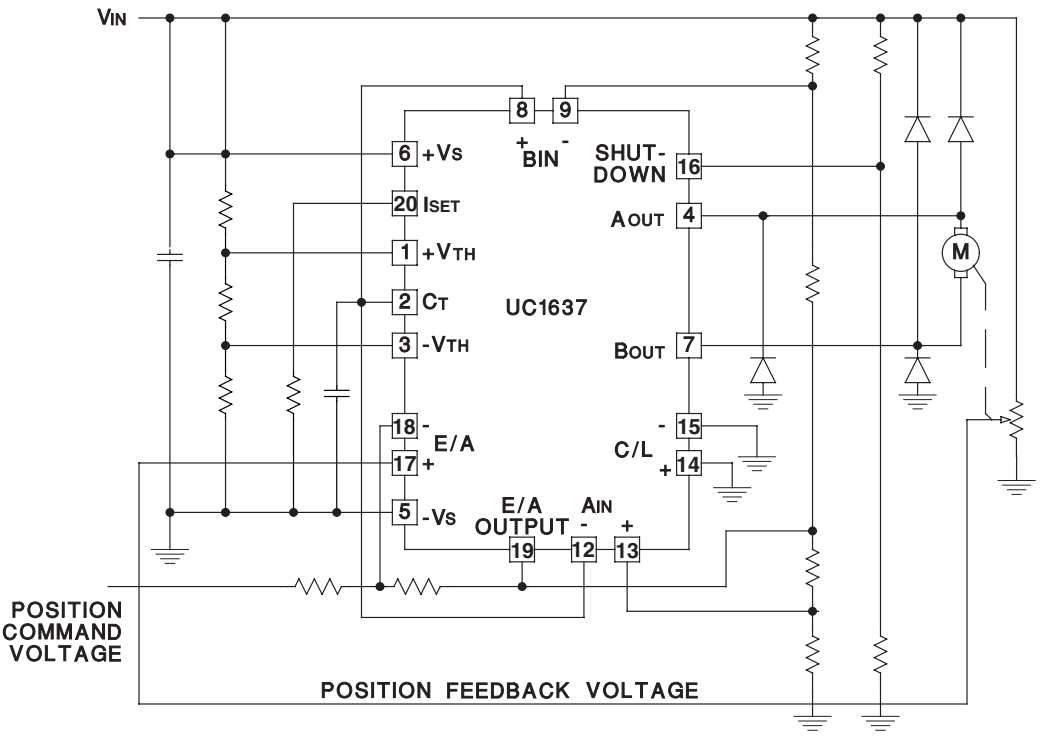



**Figure 8. Single Supply Position Servo Motor Drive**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8995701VSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8995701VSA UC1637W-SP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

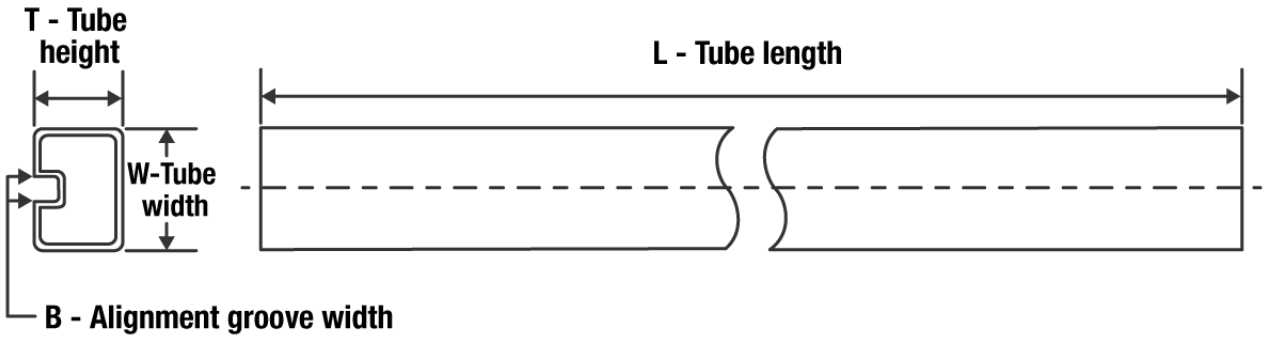
**OTHER QUALIFIED VERSIONS OF UC1637-SP :**

- Catalog: UC1637

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

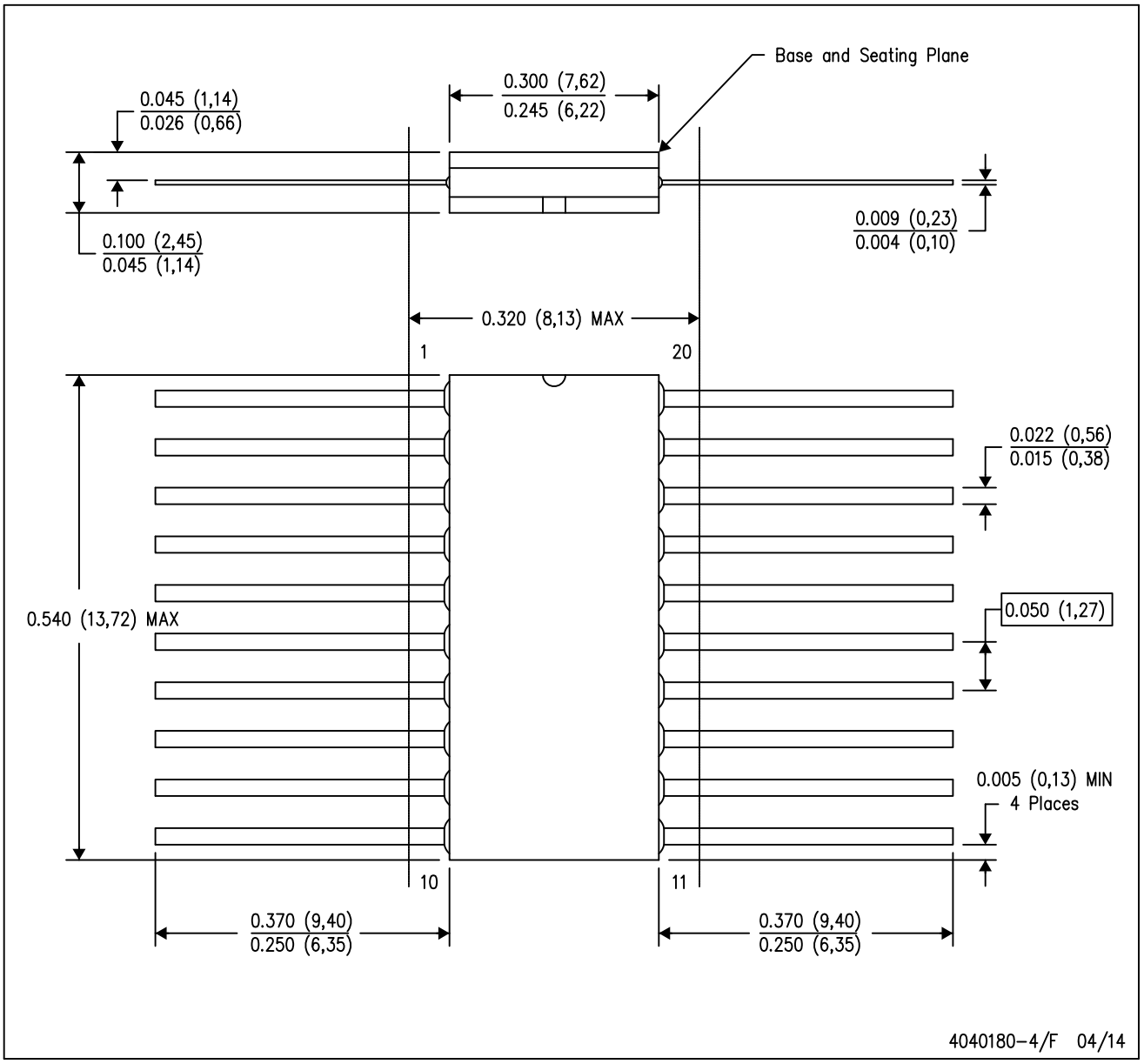
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-8995701VSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F20) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

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