

Evaluating the **ADG5401F** Fault Protection, $6\ \Omega$ R_{ON} , SPST Switch with $0.6\ \text{k}\Omega$ Feedback Channel

FEATURES

Supply voltages

Dual-supply: $\pm 5\ \text{V}$ to $\pm 22\ \text{V}$

Single-supply: $8\ \text{V}$ to $44\ \text{V}$

Protected against overvoltage on the device source pins (S and SFB) on Terminal J2

Protected against signal voltages up to $\pm 60\ \text{V}$

LEDs for visual overvoltage indication

Parallel interface compatible with $1.8\ \text{V}$ logic

On-board LDO regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

EVAL-ADG5401FEBZ

DOCUMENTS NEEDED

[ADG5401F](#) data sheet

EQUIPMENT NEEDED

DC voltage source

$\pm 5\ \text{V}$ to $\pm 22\ \text{V}$ for dual supply

$8\ \text{V}$ to $44\ \text{V}$ for single supply

Optional digital voltage source: $1.8\ \text{V}$ to $5\ \text{V}$

Analog signal source (signal generator)

GENERAL DESCRIPTION

The EVAL-ADG5401FEBZ evaluation board for the [ADG5401F](#) features one SPST switch channel and one feedback switch channel. The [ADG5401F](#) SPST switch has overvoltage detection and protection circuitry on the source pins (S and SFB) on Terminal J2 and is protected against signals up to $\pm 60\ \text{V}$ in the powered state and unpowered state.

Figure 1 shows the EVAL-ADG5401FEBZ in a typical evaluation setup. The [ADG5401F](#) is soldered to the center of the EVAL-ADG5401FEBZ, and two wire screw terminals (J2 and J3) are provided to connect to each device source pin (S and SFB) and drain pin (D and DFB). The J1 screw terminal powers the device through three EVAL-ADG5401FEBZ supply pins (VDD, GND and VSS), and a fourth pin (EXT_VL) provides a user defined digital voltage of $1.8\ \text{V}$ to $5\ \text{V}$, if required. Alternatively, a low dropout (LDO) regulator ([ADP7142](#)) is provided for $5\ \text{V}$ digital voltage control and to supply both light emitting diodes (LEDs) LED1 and LED2, which are mounted to provide visual indication of the fault status of the switch.

For full specifications on the [ADG5401F](#), see the [ADG5401F](#) data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADG5401FEBZ.

EVALUATION BOARD CONNECTION DIAGRAM

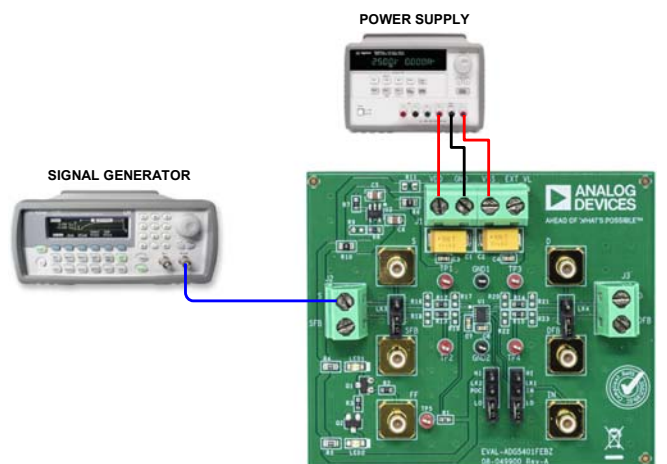


Figure 1.

TABLE OF CONTENTS

Features.....	1	Power Supply.....	4
Evaluation Kit Contents.....	1	Input Signals.....	4
Documents Needed.....	1	Output Signals.....	4
Equipment Needed.....	1	Jumper Settings.....	5
General Description.....	1	Link Headers and 0 Ω Resistors.....	5
Evaluation Board Connection Diagram.....	1	SMB Connectors.....	5
Revision History.....	2	Evaluation Board Schematics and Artwork.....	6
Getting Started.....	3	Ordering Information.....	8
Evaluation Board Setup Procedure.....	3	Bill of Materials.....	8
Evaluation Board Hardware.....	4		

REVISION HISTORY

9/2020—Rev. 0 to Rev. A

Changes to User Guide Title.....	1
Changes to Table 2.....	8

8/2020—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5401FEBZ operates independently and does not require any additional evaluation boards or software to operate. An on-board ADP7142 LDO regulator is provided as the digital power supply for the LEDs and to manually control the ADG5401F.

To supply the EVAL-ADG5401FEBZ with a dual power supply of $\pm 5\text{ V}$ to $\pm 22\text{ V}$ or a single supply of $+8\text{ V}$ to $+44\text{ V}$, connect the EVAL-ADG5401FEBZ VSS pin and GND pin together on J1. If the VDD pin voltage is greater than 40 V , remove the R6 resistor to protect the on-board ADP7142 LDO regulator and move the R10 resistor to the R11 pad (where the R11 resistor can be populated, if required) to use an alternative digital voltage supply connected to the EXT_VL pin on J1.

To set up the EVAL-ADG5401FEBZ to perform a functionality test, take the following steps:

1. Connect a power supply to the J1 connector. If a single supply is required, connect the EVAL-ADG5401FEBZ VSS pin and GND pin together on J1.
2. Use the LK1 link header to control the digital signals of the switch channel on the ADG5401F as follows:
 1. To open the switch and present it as an open circuit, place LK1 in Position LO.
 2. To close the switch and present it with a resistance of approximately $6\ \Omega$, place LK1 in Position HI.

The green LED1 then illuminates to indicate that the switch is operating normally.

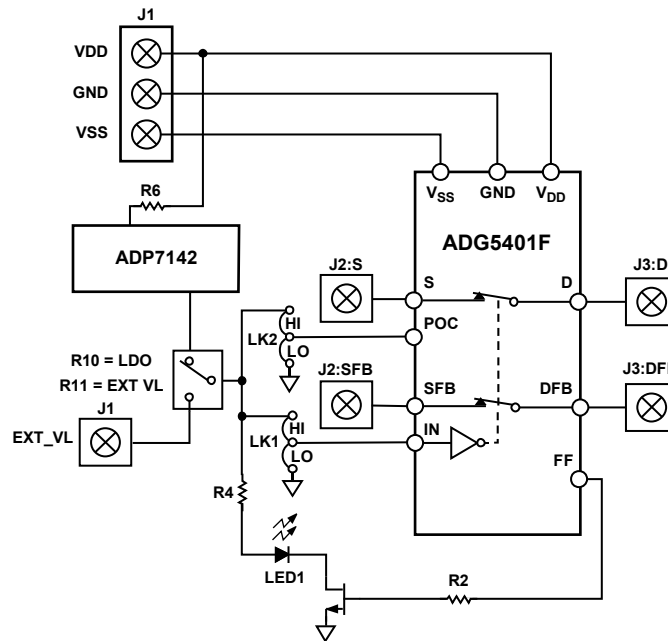


Figure 2. EVAL-ADG5401FEBZ Functional Block Diagram

23124-002

EVALUATION BOARD HARDWARE

Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the functional block diagram of the EVAL-ADG5401FEBZ main components.

The [ADG5401F](#) on the EVAL-ADG5401FEBZ passes signals from either the source connectors or drain connectors. The [ADG5401F](#) source pins (S and SFB) have fault detection circuitry that reacts to an overvoltage event. During an overvoltage event, the switch turns off, and the [ADG5401F](#) FF pin pulls low. See the [ADG5401F](#) data sheet for more details.

POWER SUPPLY

Connector J1 provides access to the [ADG5401F](#) supply pins (V_{DD} , GND, and V_{SS}). The EVAL-ADG5401FEBZ VDD, GND, and VSS terminals on J1 link to the corresponding pins on the [ADG5401F](#). For dual supply voltages, power the EVAL-ADG5401FEBZ with a supply from ± 5 V to ± 22 V. For single-supply voltages, connect the GND and VSS terminals together and power the EVAL-ADG5401FEBZ with a supply from 8 V to 44 V. The on-board [ADP7142](#) LDO regulator is provided for the digital control voltage. A secondary voltage source can be connected to the EVAL-ADG5401FEBZ EXT_VL terminal and used as the digital control voltage. To use the EVAL-ADG5401FEBZ EXT_VL terminal, move the R10 resistor to the R11 pad. Do not expose the on-board [ADP7142](#) LDO regulator to voltages greater than 40 V. Remove the R6 resistor and supply an alternative digital voltage via the EVAL-ADG5401FEBZ EXT_VL terminal, if required.

INPUT SIGNALS

Two 2-pin screw connectors, J2 and J3, are provided on the EVAL-ADG5401FEBZ to connect to the [ADG5401F](#) source pins (S and SFB) and drain pins (D and DFB), respectively. Use additional Subminiature Version B (SMB) connectors if extra connections are required. The [ADG5401F](#) is overvoltage protected on the source side, and both EVAL-ADG5401FEBZ source terminals (S and SFB) can handle a voltage of up to ± 60 V. See the [ADG5401F](#) data sheet for more details.

Each trace on the source and drain side includes two sets of 0603 pads (where the R16 to R23 resistors can be populated, if required) that can place a load on the signal path to ground. The R12 and R14 0 Ω resistors are placed in the signal path and can be replaced with a user defined value. These resistors combined with the capacitor 0603 pads create an RC filter.

The [ADG5401F](#) uses a parallel interface to control the operation of the switch channel. The switch operation can be manually controlled using the headers on the LK1 link header. Or, remove the link headers on LK1 and use the IN SMB connector to interface an external controller directly to the device control pin, IN. The LK2 link header can control the operation of the power-on condition (POC) feature.

OUTPUT SIGNALS

The [ADG5401F](#) FF pin is an open-drain output. This output indicates when the device is operating normally or if there is an overvoltage fault on one of the source pins. For visual indication, LED1 and LED2 are mounted on the EVAL-ADG5401FEBZ. When the device operates normally, the FF pin remains high (pull-up resistor required), and LED1 illuminates green. If an overvoltage occurs at any of the source pins, the FF pin pulls low, and LED2 illuminates red.

JUMPER SETTINGS

LINK HEADERS AND 0 Ω RESISTORS

The on-board link headers (LK1 to LK4) can control the [ADG5401F](#) manually and short the main switch channel to the feedback channel, if required. On-board 0 Ω, 300 Ω, and 1 kΩ resistors configure the digital control voltage and isolate the LEDs from the rest of the system. Table 1 lists the link headers and resistors and explains how each is used on the EVAL-ADG5401FEBZ.

The LK1 link header controls the [ADG5401F](#) switch channel. Place the link header in Position LO to open the switch and place the link header in Position HI to close the switch.

The LK2 link header controls the user selectable POC feature of the [ADG5401F](#). Place the link header in Position HI to disable the POC feature and place the link header in Position LO to enable the POC feature.

The LK3 and LK4 link headers short both the S and SFB nodes and the D and DFB nodes on the EVAL-ADG5401FEBZ. When using the device as a single-channel switch without the feedback channel, insert the LK3 and LK4 link headers to short the nodes.

The R6 resistor connects the VIN pin of the on-board [ADP7142](#) LDO regulator to the EVAL-ADG5401FEBZ VDD terminal supply. Remove the R6 resistor to protect the LDO regulator from voltages higher than 40 V. Move the 0 Ω R10 resistor to the R11 pad to use an alternative digital voltage connected to the EVAL-ADG5401FEBZ EXT_VL terminal.

The R4 and R5 resistors connect the LEDs to the digital power supply pin, VL, and the R2 and R3 resistors connect the [ADG5401F](#) FF pin to the LED control.

Table 1. Link Header Descriptions

Label	Position	Description
LK1	LO	S/D switch open, SFB/DFB switch open
	HI	S/D switch closed, SFB/DFB switch closed
LK2	HI	POC feature disabled
	LO	POC feature enabled
LK3	Inserted	S shorted to SFB
	Removed	S disconnected from SFB
LK4	Inserted	D shorted to DFB
	Removed	D disconnected from DFB
R6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
R2, R3	Inserted	FF pin connected to LED
	Removed	FF pin disconnected from LED
R4, R5	Inserted	LED1 and LED2 connected to the VL node
	Removed	LED1 and LED2 disconnected from VL node
R1	Inserted	1 kΩ pull-up resistor at the FF pin
	Removed	No external pull-up resistor at the FF pin
R10	Inserted	On-board LDO regulator digital voltage
R11	Inserted	EXT_VL digital voltage

SMB CONNECTORS

The parallel interface of the [ADG5401F](#) can either be controlled manually using the LK1 link header or accessed by using the IN SMB connector. To use the SMB connectors, remove the LK1 link header. Use the FF SMB connector to access the [ADG5401F](#) FF digital output.

EVALUATION BOARD SCHEMATICS AND ARTWORK

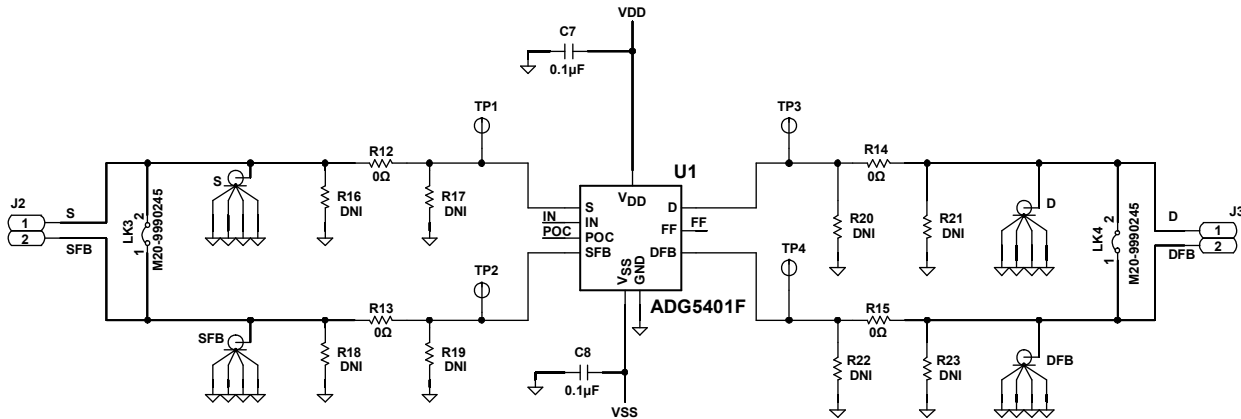


Figure 3. EVAL-ADG5401FEBZ Schematic, Page 1

23124-003

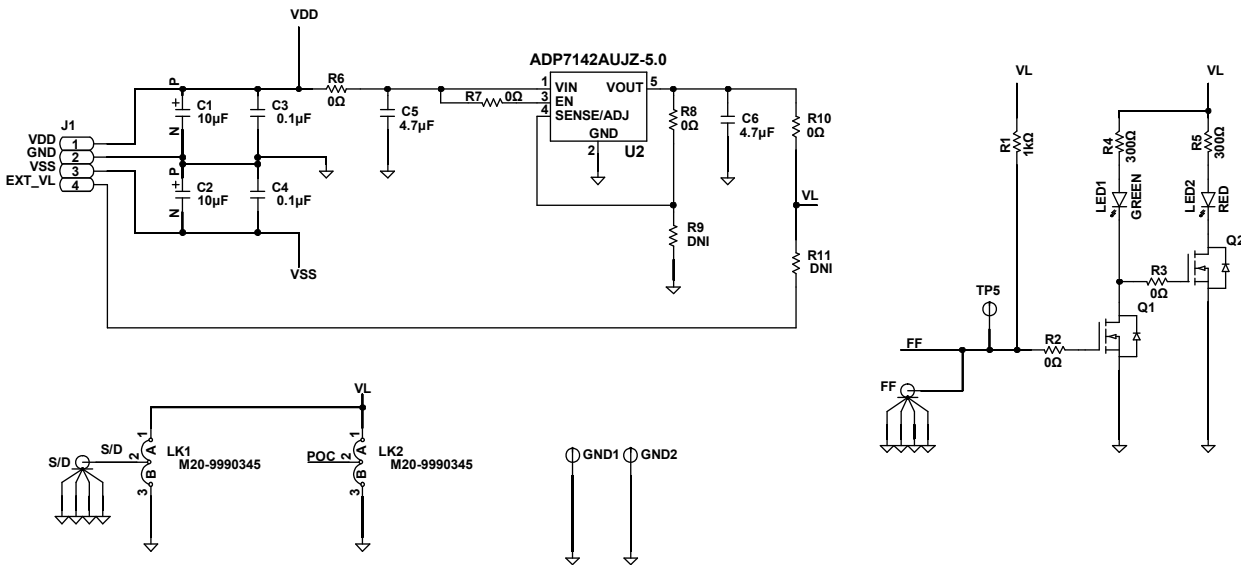


Figure 4. EVAL-ADG5401FEBZ Schematic, Page 2

23124-004

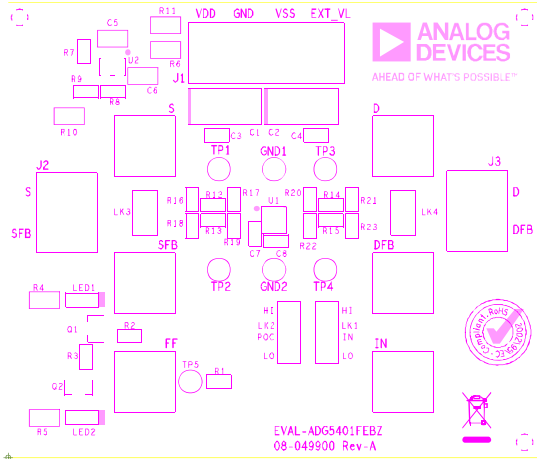


Figure 5. EVAL-ADG5401FEBZ, Silkscreen

23124-005

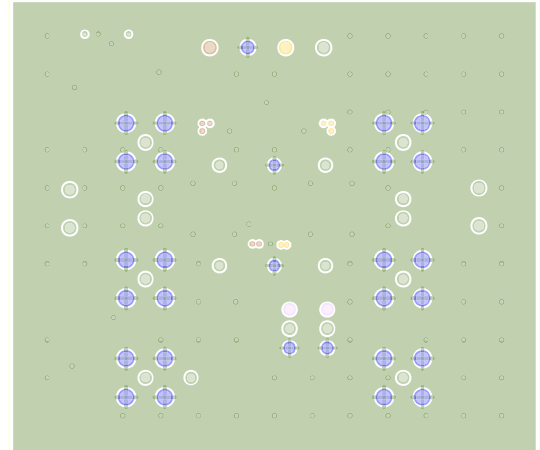


Figure 8. EVAL-ADG5401FEBZ, Layer 3

23124-008

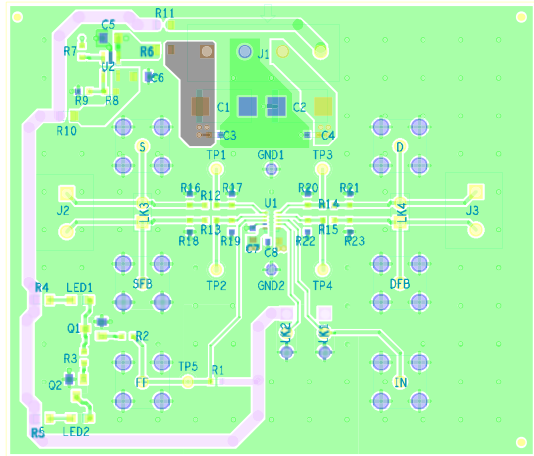


Figure 6. EVAL-ADG5401FEBZ, Top Layer

23124-006

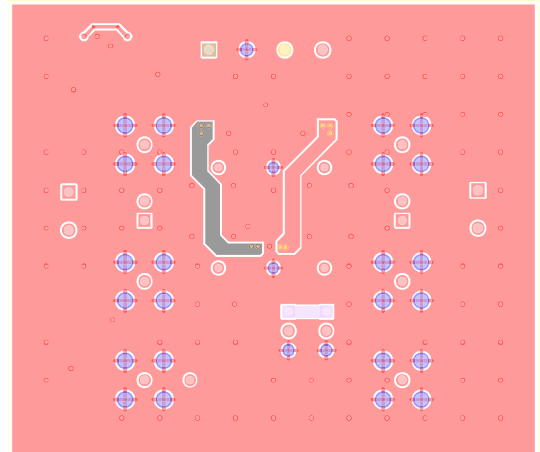


Figure 9. EVAL-ADG5401FEBZ, Bottom Layer

23124-009

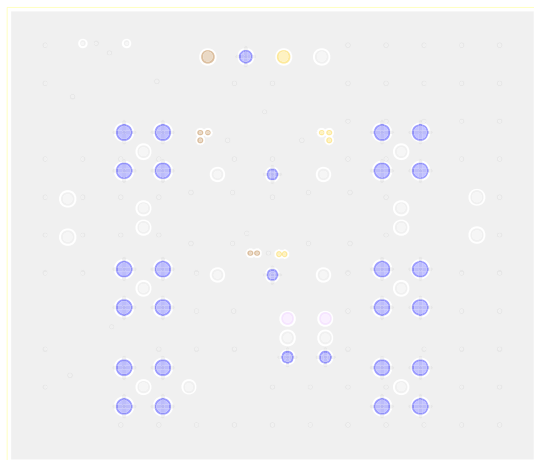


Figure 7. EVAL-ADG5401FEBZ, Layer 2

23124-007

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer	Part Number
C1, C2	10 μ F tantalum capacitors, 50 V, Size D	AVX	TAJD106K050RNJ
C3, C4, C7, C8	0.1 μ F, multilayer, ceramic capacitors, 50 V	Murata	GRM188R71H104KA93D
C5, C6	4.7 μ F, multilayer, ceramic capacitors	TDK	C2012X5R1H475K125AB
D, DFB, FF, IN, S, SFB	50 Ω , SMB sockets	Amphenol	SMB1251B1-3GT30G-50
GND1, GND2	Test points, black	Vero Technologies	20-2137
J1	4-pin terminal block, 5 mm pitch	Camdenboss LTD	CTB5000/4
J2, J3	2-pin terminal blocks, 5 mm pitch	Camdenboss LTD	CTB5000/2
LED1	LED, surface-mount diode (SMD), green	Kingbright	KP-2012SGC
LED2	LED, SMD, red	Kingbright	KP-2012EC
LK1, LK2	3-pin headers and shorting links	Harwin	M20-9990345
LK3, LK4	2-pin, 0.1 inch pitch, headers and shorting shunts	Harwin	M20-9990245
Q1, Q2	Transistors, N-channel enhancement mode field effect transistor (MOSFET), 60 V, 0.23 A, SOT-23	ONSEMI	NDS7002A
R1	Resistor, 1 k Ω , 0.063 W	Multicomp (SPC)	MC0063W060311K
R6, R10	0 Ω resistors	Panasonic	ERJ-6GEY0R00V
R2, R3, R7, R8, R12 to R15	0 Ω resistors	Multicomp (SPC)	MC0603WG00000T5E-TC
R4, R5	Resistors, 300 Ω , 0.1 W	Yageo	RC0805JR-07300RL
TP1 to TP5	Test points, red	Vero Technologies	20-313137
U1	Fault protection, 6 Ω R _{ON} , SPST switch with 0.6 k Ω feedback channel	Analog Devices, Inc.	ADG5401F
U2	40 V, 200 mA, low noise, CMOS LDO linear regulator	Analog Devices	ADP7142AUJZ-5.0

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.